Non-destructive Micro to Nanoscale Metal Patterning for Probing Thermal Anisotropy

A report discussing the use of stencil lithography in the fabrication of nanoscale grating structures, submitted to the Stanford Nanofabrication Facilities in partial fulfillment of course requirements for ENGR 241.

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Christopher Perez & Heungdong Kwon
Department of Mechanical Engineering
Stanford University
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Executive Summary

In this report, a process flow is referenced that sought the creation of periodic metallic gratings on the order of 150 nanometers using a stencil lithography technique. To summarize the associated standard operating procedure (SOP), the stencil is comprised of a patterned, 200 nm thick, suspended low-stress silicon nitride membrane with silicon as the structural handle material. The following renderings, taken from the SOP, demonstrate the high-level structure of a single silicon nitride stencil with silicon handle wafer.

A thin (25 nm) film of aluminum was then deposited through the stencils, imparting their grating features on a target substrate (silicon), resulting in metallic grating structures on the substrate. This was performed with the intent of the grating widths to reach the wavelength scales of the lasers used in thermal metrology (i.e. Ti:Sapphire, $NdYVO_4$, etc.).

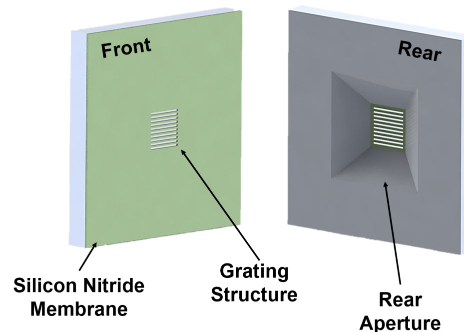

Figure 1: A rendering of the front and rear views of the silicon nitride stencils.

Key findings include that the grating structures created, on the order of 150 nm width with a pitch of 300 nm, were comfortably achieved using the JEOL JBX-6300FS Electron Beam Lithography System (the JEOL). Due to the small device footprints, the maskless lithography tool's resolution (the Heidelberg MLA150, or the Heidelberg), was deemed much too coarse due to its 1-2 μm wafer alignment uncertainty. This wafer alignment was crucial to pattern front-to-backside alignment marks that would provide the device orientation when moving on to the e-beam lithography using the JEOL.

Additionally, a SiN etch using the Oxford RIE tool recipe was used to "free" the grating structures by etching through the backside of the device. This etch however, was characterized as being highly variable, with the SiN membrane still adhered to the grating structure through the rear aperture. Regardless, scanning electron microscopy (SEM) images are taken of these devices at various points in the etch, qualitatively demonstrating how the SiN etches as a function of time.

The grating quality is investigated through SEM images that were often misleading due to the insulating nature of SiN. Often times, the SiN backside etch to free the gratings was deemed complete, but was seen to be premature after metallization. This caused the beam widths to be under-estimated before metallization, with an estimated duty cycle (ratio of "on", or grating beam width, versus "off", or grating void) of 30-70. Post-metallization however, the duty cycle was confirmed to be 55-45 through SEM images, much more representative of the intended design.

The location of "chip trenches", or square frames that enclose a single device, was found to play a major role in the success of the process flow. This gave rise to a "initial" flow, where the chip trenches were patterned on the same plane as the grating structures. This had a negative impact on the e-beam resist uniformity and subsequently made for an unreliable exposure, with many devices not exposed at all. The "final" flow offered a correction to this and the resulting devices were deemed successful as a proof of concept.

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1 Brief Process Flow (adapted from the associated SOP)

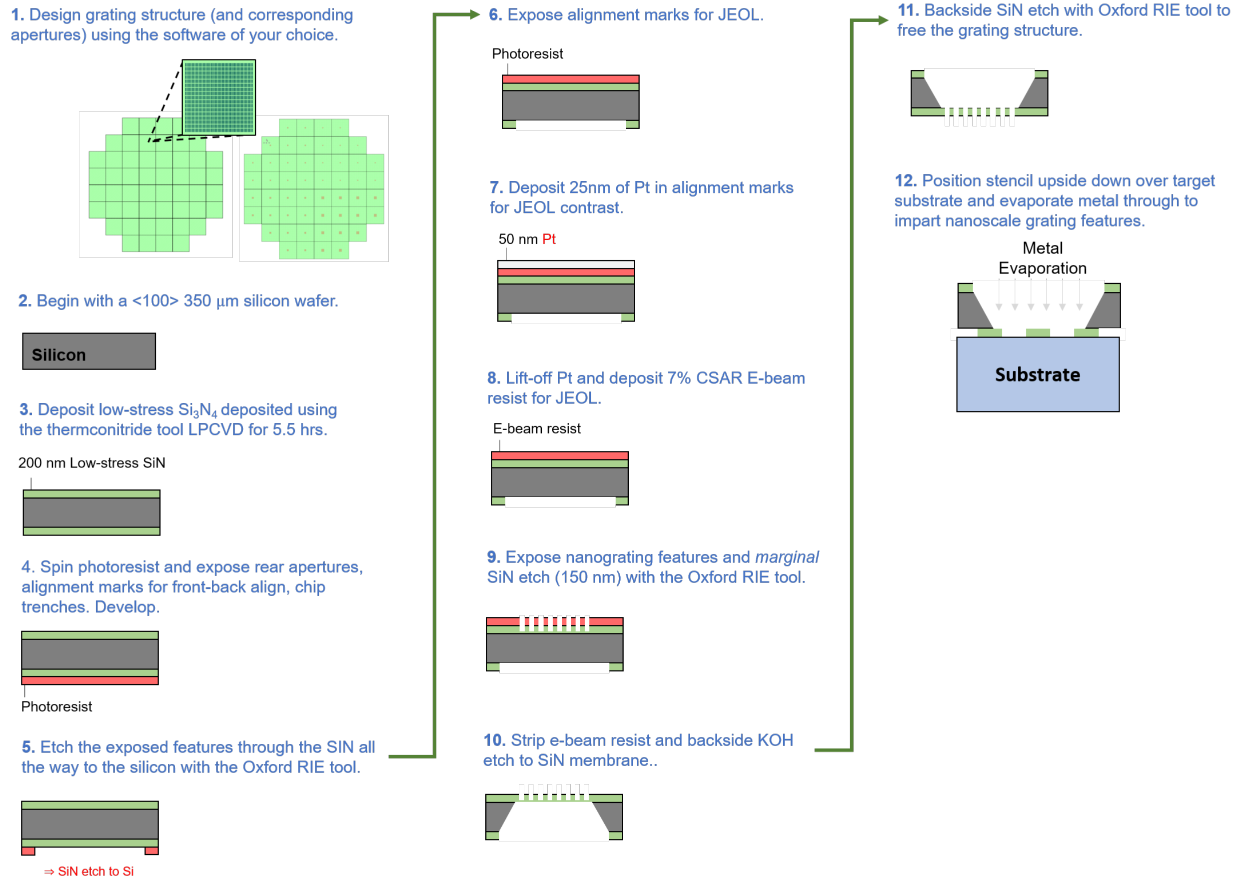

Figure 2: The above figure succinctly describes the high-level process flow that will be referred to in later portions of the report.

2 Project Background

2.1 Optical Polarization

Controlling the polarization of light through periodic gratings is a technique that has seen extensive use throughout the past half century, giving rise to optical components that essentially act as waveplates, absorption filters, and other birefringent materials that have a refractive index dependent on the polarization and propagation direction of the incident light. All of these components are based on aligning a coherent source, or laser, along a portion of the material that will either slow, steer, or absorb/reflect the polarization components of the source. With the ever-increasing fidelity of semiconductor fabrication however, periodic grating schemes have been made exceedingly small, thus allowing the control of electromagnetic radiation fields with nanometer-scale wavelengths once limited by diffraction.

2.2 Optical Methods to Probe Thermal Properties

One of the major applications that require such precise control of radiative fields is thermal metrology. One such technique is time-domain thermoreflectance (TDTR), a method that uses picosecond laser pulses to excite a sample (the "pump" laser) and a continuous laser to monitor its surface temperature response in time (the "probe" laser). These systems use a reflective transducer blanket layer of aluminum deposited on top of the sample to probe the surface temperature response as a proportional change in surface reflectively. The data from the heat input and temperature response signals are translated to physical material properties through a least-square fit to a multi-layer thermal model.

3 Motivation & Project Goals

The measurement difficulties in these optical thermal metrology methods, especially involving materials with anisotropic and excessively low thermal conductivity (κ_r) values (e.g. organics, polymers, etc.), is of great fundamental and applied value. For example, TDTR is a non-contact technique and thus ideally suited for high-throughput measurements. However, it suffers from diffraction-limited beam diameters when attempting to invoke a two-dimensional heating geometry (i.e. a scenario where the pump beam diameter is smaller than the in-plane heat diffusion length).

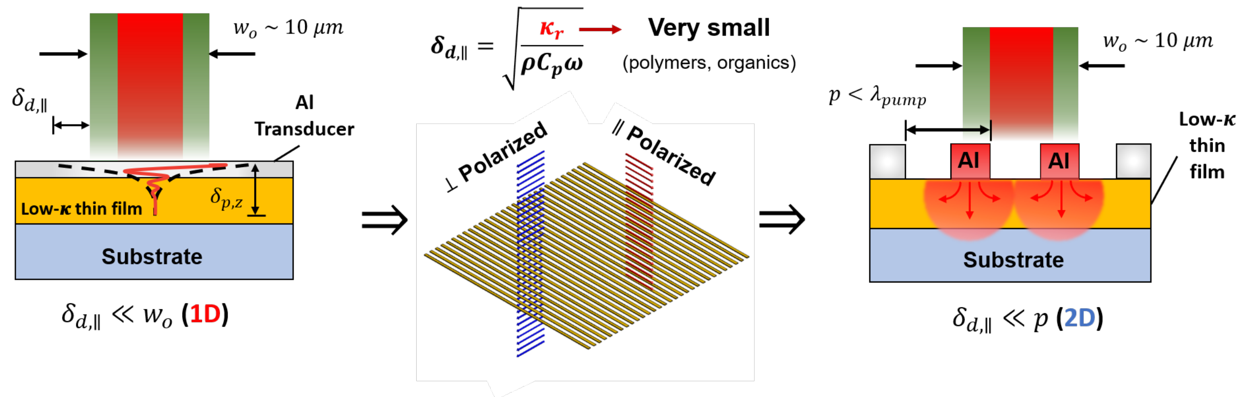

Figure 3: (Left) The traditional TDTR heating geometry, consisting of the "in-plane" diffusion length, $\delta_{d,||}$, being much smaller than the characteristic heating length, or the beam diameter, on the order of $10\mu m$. (Center) A sub-wavelength grating could effectively reflect/absorb the incident laser beam given that its polarization is aligned with the long-side of the grating structure, while perpendicular components are not met with a local electric field and are thus allowed to pass through, not heating the substrate beneath. (Right) The desired heating geometry that is expected to confine incident laser heating to the feature sizes of the nanometer grating itself, invoking a two-dimensional scenario that can be probed to reveal anisotropic thermal properties.

The low-κ_r thin-films of interest are likely to be sensitive to chemical resists and high process temperatures given their organic/polymeric nature. Our goal then is to eventually directly deposit *nanoscale* grating features, or features smaller than the wavelength of the pump beam, on top of the thin-films using stencil lithography described in the proceeding "Introduction" section,(page 4). The grating would essentially act as a wire-grid polarizer, thus avoiding direct substrate laser heating while confining the incident heat input to the sub-laser wavelength length-scales of grating itself, as seen in Figure 3. In this fashion, two-dimensional information can be captured and in-plane thermal properties can be extracted.

The goals for this project are as follows:

◦ Confirm the success of the stencil lithography approach for imparting metallic grating features.

◦ Reveal the structural parameters that effect the survival rates of the grating structures.

◦ Characterize the SiN etching based on the freeing of the gratings.

◦ Assess the resulting line quality of the grating structures.

In this study, we analyze fabricated periodic metallic gratings on the order of 150 nm using a stencil made of SiN with a handle wafer of silicon. This was is intended to be read alongside the associated SOP for creating these grating structures. This represents a first step in the further development for the eventual goal of nanometer-scale patterns suitable for the wavelength scales of the lasers used in thermal metrology (i.e. Ti:Sapphire, Nd:YVO_4, etc.).

4 Introduction - What is Stencil Lithography?

Stencil Lithography is a technique based on the principle of shadow masking a flux of atoms, molecules, or particles to locally modify a the surface of a substrate. This process can accommodate a variety of methods such as deposition, etching, or ion implantation[1].

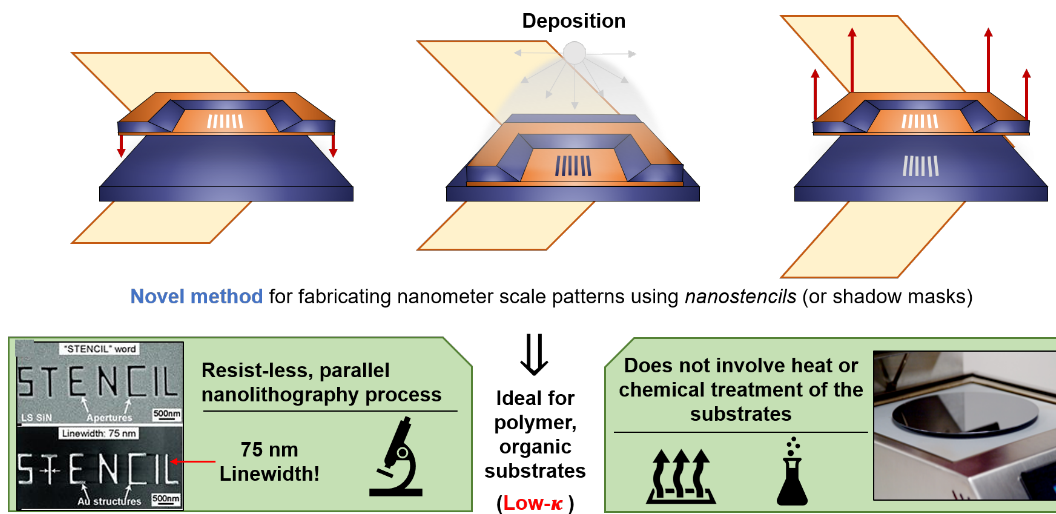

Figure 4: The specific stencil lithography process implemented in this work. A stencil with aperture features is placed on a target substrate while material is deposited on the stencil. The substrate thus gains the features defined by the apertures of the stencil in the form of deposited structures.

This particular project involved material deposition, namely aluminum evaporation, where the stencil is positioned between a target substrate and the evaporation source to mask the deposition of the incident material flux. It is important to note that this process is performed without any resist processing and the features on the stencil are imparted onto the substrate as deposited structures. This resist-less, low-temperature processing was attractive given the highly sensitive organic/polymeric materials under study, as explained in Figure 4. There are however, advantages and disadvantages to this processing scheme, summarized in the table below.

Table 1: The high-level advantages and disadvantages of stencil lithography.

Advantages	Disadvantages
No resist processing, avoiding organic materials, solvents, energy radiation, and mechanical pressure	Blurring due to inherent gap
Easy implementation and applicable with access to physical vapor deposition tools	Clogging if the deposited thickness of the material is on the same order as the stencil aperture size
Allows for reusability being mindful of the clogging effect	Membrane stability can limit aspect ratios that can be achieved using dry etching techniques

5 Depositing Grating Patterns via Stencil Lithography

5.1 Process Flow

The process flow for these nanoscale grating structures is detailed in the associated SOP. To facilitate following along in the various points along the process flow, we include the high-level flow in Figure 2 for convenience. It is important to note that all the gratings considered in this study were on an initially 200 nm thick SiN membrane.

The grating dimensions referred to throughout this report, especially with regard to how the "aspect ratio" (L:w) and "pitch" (p) were defined, are introduced in the following Figure 5:

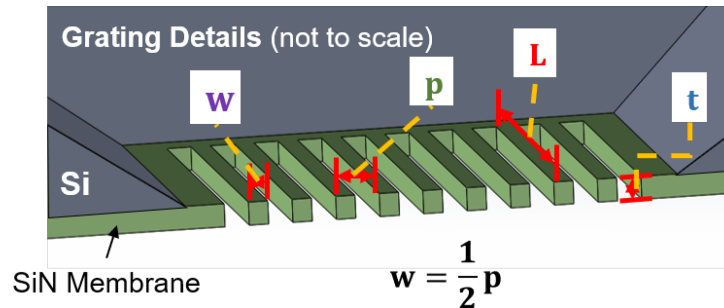

Figure 5: The variables corresponding to the dimensions of the grating structure. NOTE: We define the "aspect ratio" as the length-to-width of a grating beam, or L:w.

Another piece of terminology is the "duty cycle", defined as:

$$DutyCycle = \frac{''on''}{''off''} = \frac{w}{p-w}$$

A duty cycle of 1/2 is sought after in this project, and referred to as "50-50".

6 Stencil Lithography Grating Analysis

6.1 Wafer Breakdown

The grating structures that successfully made it throughout the process was initially dependent on the backside SiN etch that "freed" them, or step #11. After this step was optimized, the main bottlneck for grating survival was front-to-back wafer alignment, touched upon in detail in the section "Frontside SiN Etch Characterization".

6.1.1 Design of Experiment

Upon completion of the lithographic steps in the process flow, as well as the marginal etching of the SiN, the remaining task was to "free" the grating structure. This was performed via a backside SiN etch using the Oxford RIE tool to mitigate the capillary effects of a wet etch that would otherwise make the grating beams "stick". The main structural elements, namely length-to-width (L:w) aspect ratio, the critical beam width dimensions, and what we deemed to be "free" or "confined" configurations, were varied for to provide insight on the kinds of structures that would survive the process flow. Figure 6 below summarizes the experimentation matrix implemented, as well as defining these "free" and "confined" layouts.

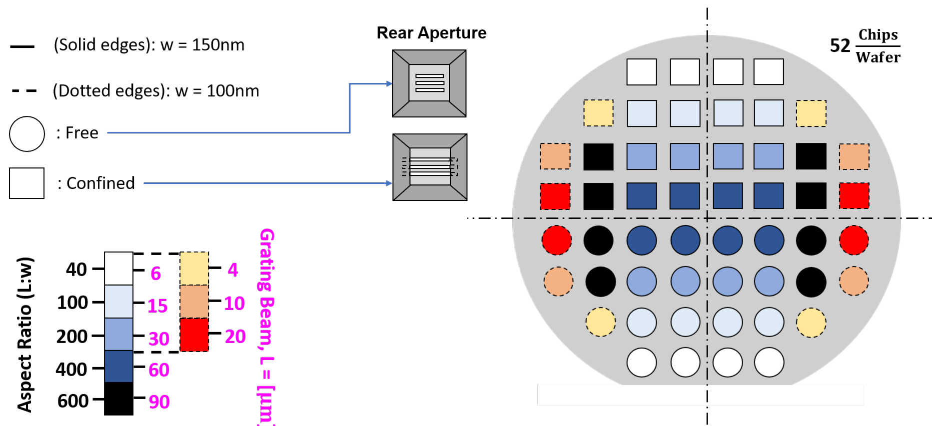

Figure 6: The implemented wafer layout that varied the aspect ratio, free/confined configurations, as well as critical beam width dimensions.

With this experimentation matrix in mind, various scanning electron microscopy (SEM) images were analyzed after **steps #9, #10, #11, and #12** to assess the viability of the process flow described on page 1.

6.1.2 Surviving Structures

As mentioned previously, the main factor for grating survival was front-to-back wafer alignment, which for lower aspect ratios can be extremely detrimental. This was expected given the tool used for front-to-back wafer alignment (the Hiedelberg ML150A), which has an alignment uncertainty of about 1-2 μm. This is discussed in more detail in the section "Frontside SiN Etch Characterization". The survival locations can be seen in the subsequent Figure 7:

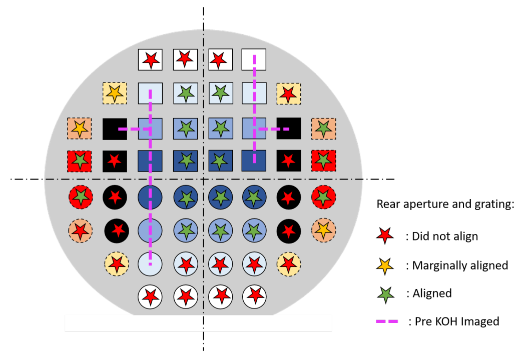

Figure 7: The surviving grating structures as laid out on the wafer. Red, yellow, and green stars indicate the structures that did not align, marginally aligned, and did align with the rear aperture window, respectively. The pink dotted line indicates devices that were removed and SEM imaged before the KOH etch (step # 10).

6.2 Frontside SiN Etch Characterization

The frontside SiN etch provided a means with which to assess the quality of the e-beam exposure since it defined the grating structure within the silicon nitride membrane. It was a timed etch, and the marginal etch target was 150 nm, leaving 50 nm of SiN membrane left. As a reminder, this comprises step #9 in the process flow. By measuring the SiN thickness using the NanoSpec tool, we calculated an RIE etch rate (using the Oxford RIE tool at 200V accelerating voltage) to be around 1.2 nm/s.

Following the process flow outlined on page 1, the KOH etch in step #10 was also performed. As mentioned in the SOP, there were two process flows implemented that varied very little. The only difference between them was the placement of what we call "chip trenches", or rectangular frames surrounding each individual device that are etch down into the Silicon. Their widths are adjusted such that after the KOH step (step #10), they only etch about 80% through the wafer. The individual devices can then be "popped" out using tweezers.

The initial process flow had these chip trenches on the front of the wafer (same plane as the grating structure), while the final flow had them on the rear of the device (same plane as the aperture). Using SEM, we acquired images of the grating structure at steps #9 and #10, seen in Figure 8:

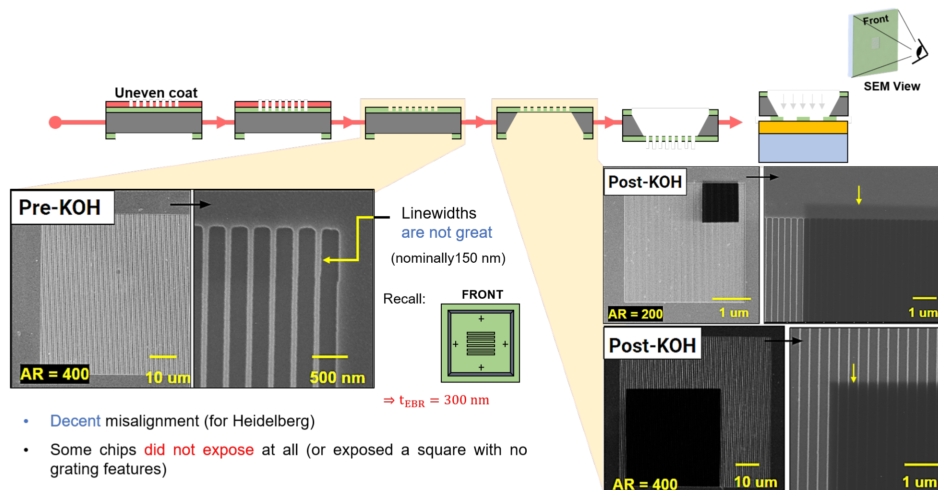

Figure 8: SEM images after the frontside SiN etch, pre/post the KOH etch, as well as which steps in the initial process flow they correspond to. A small illustration is also included of where the "chip trenches" were located as visualized on the front of the device.

As seen in Figure 8, the linewidths achieved are not representative of what we had nominally designed for (150 nm). The linewidths seem to be much thinner, on the order of 80-100 nm. Additionally, we also observed that some of the devices or "chips" did not expose at all in some regions. These issues were attributed to the uneven spinning of the e-beam resist caused by the existence of the chip trenches in the same plane as the devices: a realization that was corrected with the "final" flow. The results for the same kind of SiN etch, post KOH, for the final flow are shown in Figure 9:

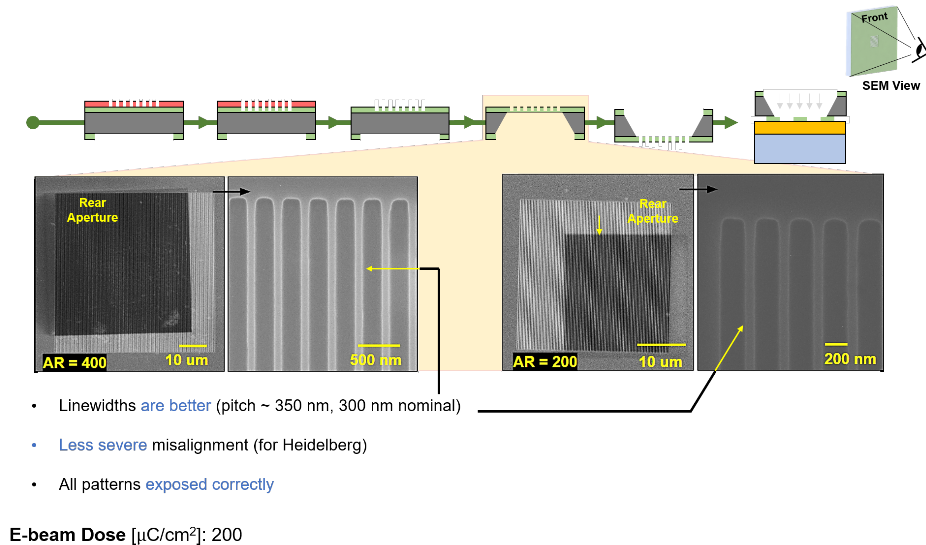

Figure 9: SEM images after the frontside SiN etch, post the KOH etch, as well as the step in the final process flow they correspond to. A small illustration is also included of where the "chip trenches" were located as visualized on the front of the device.

As seen in Figure 9, the linewidths achieved looking more like what we had nominally designed for (150 nm). The final process flow showed more promise in that the pitch seem to be slightly larger, on the order of about

350 nm where it should be 300 nm. It is also important to note that all the devices or "chips" exposed correctly on the wafer processed with the final flow. The e-beam dosage was also deemed slightly too much since for both the initial and final flows were subjected to a 200 $\mu C/cm^2$ dose.

After KOH etching for both initial and final flows however, we see a much darker contrast signifying how the rear aperture has made its way to the bottom of the membrane. There is some degree of misalignment, but it was expected given the tool used for front-to-back wafer alignment (the Hiedelberg ML150A), which has an alignment uncertainty of about 1-2 μm. This misalignment is not as significant for higher aspect ratio gratings, such as those in Figure 8. Since the aspect ratio is defined as the length to width ratio of the grating beams, the lower aspect ratio devices possess a much smaller footprint, on the order of 6 μm x 6 μm for an aspect ratio of 40 (as seen in Figure 6). The use of more precise front-to-back alignment tools is necessary in these instances, where the misalignment actually causes the aperture to miss completely: never reaching the device.

6.3 Backside SiN Etch Characterization

The backside SiN etch was a pivotal step in the process flow that served to free the grating structure within the silicon nitride membrane. It was a timed etch, and insightful conclusions were drawn based on SEM images taken at various different etch times and accelerating voltages. This was an iterative procedure since the SiN thickness possessed the same thickness uncertainty as the wafer itself, measured to be about $\pm 30 - 50$ nm by testing various spots with the NanoSpec tool. The following Figure 10 shows this iterative procedure with the initial process flow via SEM images of the backside of the stencil as a function of time:

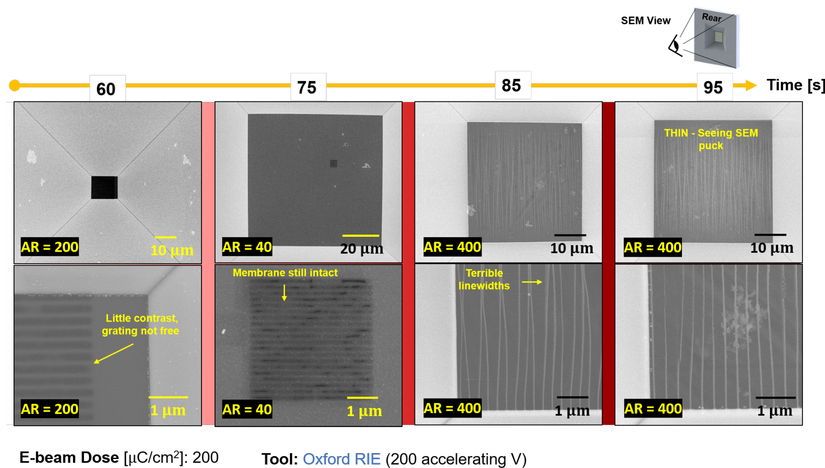

Figure 10: The SiN backside etch for the initial flow. We see how individual the backside SiN etch can be across devices, as well as the negative effect of the e-beam exposure in the initial flow since when the gratings are finally free (the 85 and 95 second cases), the linewidths are severely below the 150 nm wide designed value.

From the above figure, we see little contrast after 60 seconds, indicating the SiN membrane is still intact. This indicates the nominal SiN thickness after the frontside SiN etch was overestimated (nominally 150 nm). On the image corresponding to the 75 second case, we see small holes that provide even more contrast with the rest of the SiN structure. Based on the image corresponding this case, we can conclude that the SiN thickness uncertainty is an issue that can vary the SiN etch time significantly. As seen in the 85 and 95 second cases, the e-beam exposure was also confirmed to be a problem. The beam thicknesses are well below the nominal 150 nm designed for, and although they are free, they are so thin that they bow uncontrollably.

These results prompted us to carry out the same study, but for the final process flow. Figure 11 summarizes the results for this study:

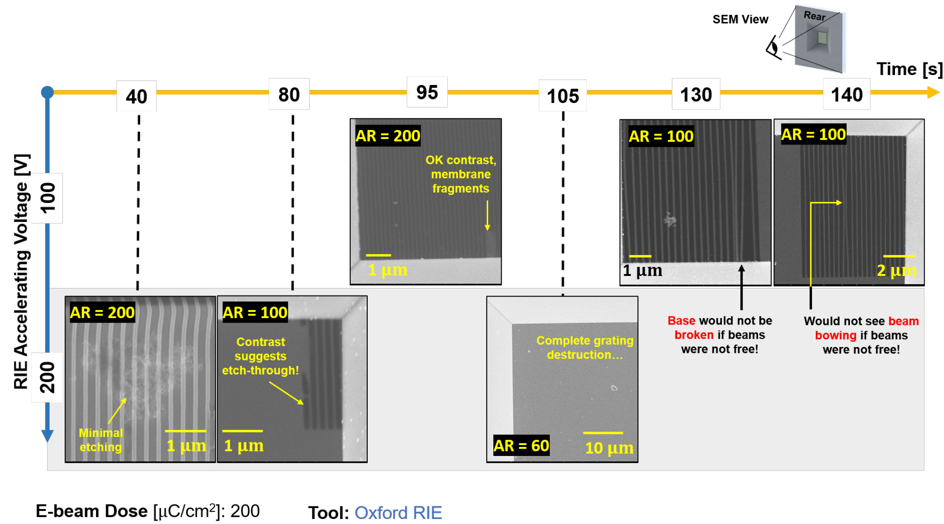

Figure 11: The SiN backside etch for the final flow. We see a much better result for the backside SiN etch across devices as compared to the initial flow. The three most promising devices (1) 200V 80 seconds, (2) 100V 130 seconds, and (3) 100V 140 seconds were deemed the best candidates for metal deposition.

For the final flow backside SiN etch study, three different RIE accelerating voltages were experimented with (although only two were SEM imaged) to notice a difference in the etch quality. No such difference was observed, although this exercise served to enabled the quantification of the SiN etch rates at these varying voltages, seen in the table below:

Table 2: A summary of the silicon nitride etch times using the Oxford RIE tool at varying accelerating voltages.

Accelerating Voltage [V]	Etch Rate [nm/s]	Uncertainty[nm/s]
50	0.54	± 0.02
100	0.70	± 0.05
200	1.25	± 0.08

As seen in Figure 11, the contrast for the grating structure is much more pronounced as it was for the initial flow. In particular, the trials at 100V for 130 and 140 seconds clearly demonstrate free grating structures. The grating at 130 seconds shows two beams breaking at the base, something that would not be possible had they not been free. Additionally, the grating at 140 seconds demonstrates beam bowing at the center of the device. Again, this would not happen had their been a underlying SiN membrane.

6.4 Linewidth Quality Analysis

To assess the linewidth quality of the stencil, the stencil was used as intended by evaporating 25 nm of aluminum through it onto a silicon substrate. Both the stencil and the deposited metal on the silicon target substrate were characterized via SEM imaging. It is important to note that the aluminum deposition thickness was chosen to be thin since we did not want to destroy the grating structure by depositing a metal thickness on the same order as the thickness of the grating beams. Figure 12 shows the importance of this phenomenon.

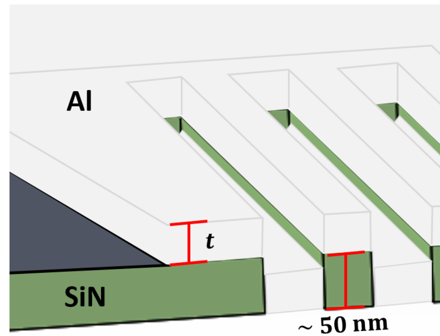

Figure 12: A demonstration of the relative grating beam-metal deposition thickness issue. Note that when the thickness of the metal layer is around the same order as the expected SiN beam thickness, the grating structure can be destroyed.

When "t" (the thickness of the metal layer) in the above figure is around the same order of our expected SiN beam thickness, the grating structure can be destroyed when the stencil is removed from the target substrate due to significant sidewall "sticking" between the grating beams. This was the main motivation driving both the future increase of SiN membrane thickness, as well as thinner metal depositions.

6.4.1 Stencil Post-Metallization

The stencil was SEM imaged after metallization to assess whether the SEM contrast observed was indicative of the degree of grating beam "freeing". Since SiN is a naturally insulating material, it does not always provide the best imaging results when inspected through an SEM. After metal deposition however, the introduction of a fairly thin layer of metal served to better resolve many of the critical grating features such as the grating beam edges and voids. Figure 13 shows the post-metallization SEM images of the three most promising stencils mentioned in the preceding section:

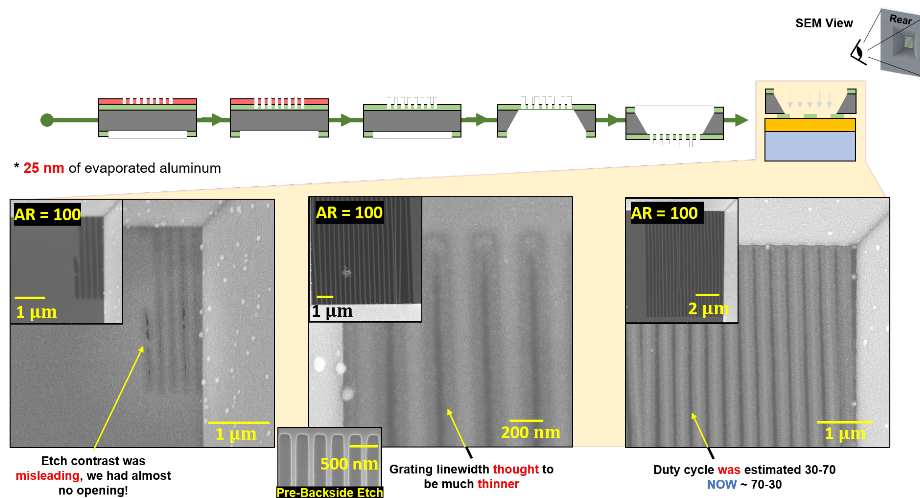

Figure 13: (Left) The stencils at 200V 80 second SiN etch, (center) 100V 130 second SiN etch, and (right) 100V 140 second SiN etch after metal deposition. The corresponding pre-metallization stencil is shown for each on their top left corners. The stencil on the left indicated that the SEM images taken before were misleading, showing contrast but failing to image the hidden etches of the grating beam.

As seen in the above figure, misleading conclusions were drawn when SEM imaging the stencils prior to metallization. By comparison, the void spaces between the grating beams seemed much larger. In contrast, the metallization images demonstrate the existence of what seem to be rounded edges where the SEM could not focus and where we subsequently deemed it void space. The metal deposition showed us the "true" grating in a sense, with the duty cycle being vastly underestimated from previous SEM images. Before, we had calculated it to be around 30-70, with void spaces comprising the larger part. However, we see that the duty cycle is actually around 70-30 according to the images in 13.

6.4.2 Substrate Deposition

The next step in the assessment of the nanoscale gratings was to note the quality of the structures they imparted on the target substrate. The substrate was chosen to be silicon and, as mentioned previously, 25 nm of aluminum was deposited through the three most promising stencils described in the preceding section. The stencil processed with a 200V 80 second SiN etch yielded no discernable deposited features with SEM imaging. This was expected due to the exceedingly small void spaces in the stencil, seen on the left in Figure 13. The other two stencils however, yielded successful gratings feature the exact negative of the stencil. Figure 14 displays these gratings imaged with SEM and a focused ion beam (FIB), along with their pre-metal deposition stencils:

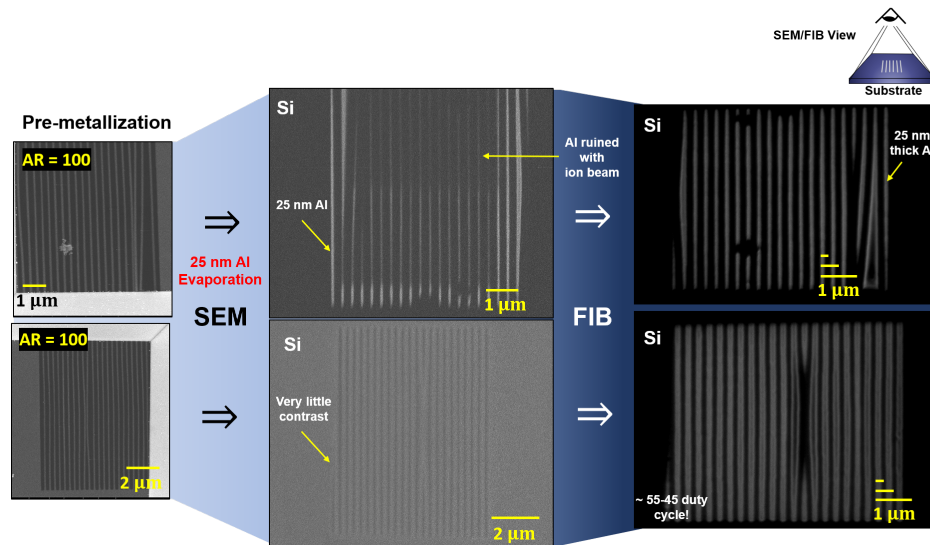

Figure 14: (Left) The stencils and corresponding (center) SEM images, and (right) FIB images when using them to deposit metal.

The deposited gratings were extremely difficult to discern via SEM, due to their small features and overall footprint on the silicon substrate. This warranted the use of the FIB, which could distinguish the structure from the substrate based on their elemental mismatch via their atomic number. The grating structures featured grating widths of around 200 nm, very much on the order of our nominal value of 150 nm. This is in contrast to both the pre and post metallization SEM images of the stencil, which are now deemed to yield underestimations in the grating beam widths. From the images, a duty cycle of around 55-45 was observed, very close to our intended 50-50. The imperfections in both structures are also seen to be successfully transferred, with the top row device imparting its broken beam shape and the bottom row device imparting its beam bowing characteristics.

It is important to note that the images with the FIB were taken hastily, since the aluminum deposition was extremely thin (25 nm). The strength of the FIB caused the metal to evaporate and we were slowly destroying the grating structure by virtue of imaging it. This can be seen with the top row device, since imaging with FIB

was done prior to imaging with SEM, causing a fading of the grating structure in the SEM image. This was also the reason atomic force microscopy (AFM) was not performed on these devices. Since they were now partly evaporated, AFM would not yield a representative profile of the grating structure dimensions if freshly deposited. A more sophisticated, higher fidelity SEM imaging system, in conjunction with guiding markers for finding the device, are things that will be implemented in the future.

7 Project Overview - Winter 2019

7.1 More Precise Alignment Techniques

One of the hallmarks of this project involved gaining familiarity with creating such grating structures, as well as validating silicon nitride as a suitable candidate for the stencil material. However, even with features on the order of 150 nm were fabricated, the current process flow is pushing the limits of the implemented front-to-back alignment methods. This was apparent in Figures 8 and 9 where the rear aperture is clearly not in the center of the device as intended. Although this was not seen as too much of an issue with larger aspect ratios, this effect ultimately led to the failure of a significant amount of our devices. As seen in Figure 7, most of the unsuccessful devices were those with smaller aspect ratios, since they possessed a much smaller device footprint. This made it front-to-back wafer alignment more critical and the main survival factor.

7.2 Silicon Nitride Membrane Thickness

As mentioned previously, the SiN membrane thickness was also a major facet of the process flow that influenced the realization of the grating structure. In this study, we restricted ourselves to a 200 nm membrane thickness, although this was slightly thin when comparing this to the uncertainty of the wafer thickness itself, $\pm 30 - 50$ nm. For this reason, the SiN etches were characterized as being highly individual, with timed etches not being able to be transferred across devices without question or doubt.

The thin membrane thicknesses in turn drove the need for smaller metal deposition thicknesses, for the reasons mentioned in the section titled "Linewidth Quality Analysis". If thicker membranes were used, the target for etching would be larger and more comfortable to achieve and thicker metal depositions could be carried out.

7.3 Future Scope

Stencil lithography shows promise as a method to impart grating structures on a target substrate in a non-volatile, non-destructive fashion. This makes it an ideal method candidate for dealing with low-κ materials such as polymers and organics. Nanoscale features (on the order of 150 nm) have been proved to be deposited via stencil lithography and can provide the subwalength-scale periodicity needed for thermal metrology techniques and as mentioned in the "Motivating More Sophisticated Lithography Techniques" section.

If these gratings are to be implemented in real experiments, the resulting device footprints must be on the order of 50-100 μm squared. Thicker membranes are expected to aid in this effort, providing more structure throughout the entire process flow. At these scales however, the stencil-substrate contact would likely be more of an issue than mentioned here. For this reason, stencil modifications are being considered, such as using magnetic forces to ensure the most intimate contact possible.

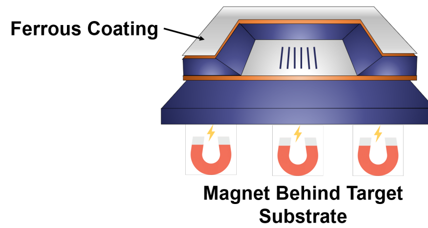

Figure 15: The high-level concept using magnetic force to improve stencil-substrate contact during the deposition process.

Regardless, this study reports the successful fabrication of nanoscale grating structures using stencil lithography. The produced work is on par with those structures realized in the literature, with the added benefit of covering a much wider deposition footprint across a target substrate. The comparison with this work and the available literature is given in the subsequent Figure 16:

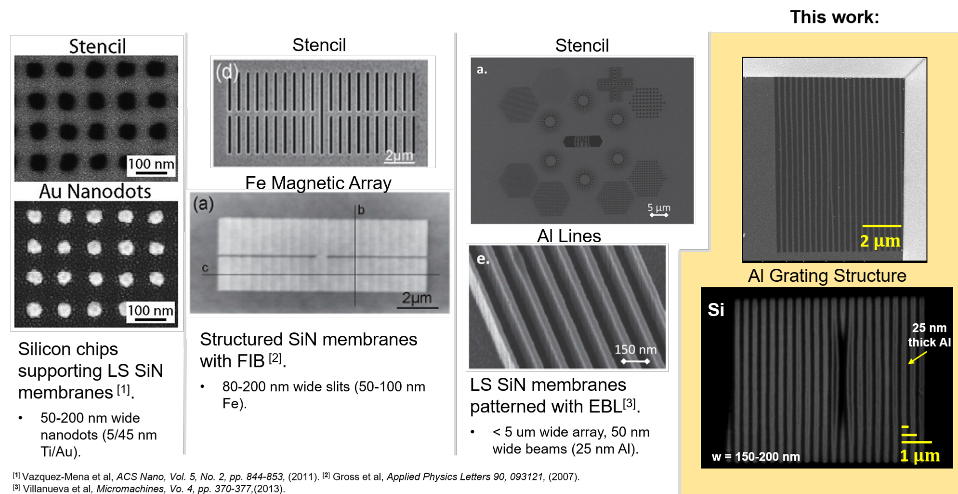

Figure 16: The current devices in the field that have achieved similar nanoscale features via stencil lithography, as well as the proof of concept provided in this report.

8 Project Contributions

Heungdong Kwon and **Christopher Perez** carried out the fabrication in its entirety.

9 References

[1] O. Vazquez-Mena, L. Gross, L.G. Villanueva, & J. Brugger, "Resistless nanofabrication by stencil lithography: A review", *Microelectronic Engineering* 132, pp. 236-254, 2018.
[2] SNF Labmembers Wiki, https://snf.stanford.edu/SNF/, 2018.
[3] Heidelberg Industries, "MLA 150 Maskless Aligner", *Doc. No.: DWL-HI-062*,Revision 1, pp. 42-67, 2016.