High Aspect Ratio Si Etching in STS2

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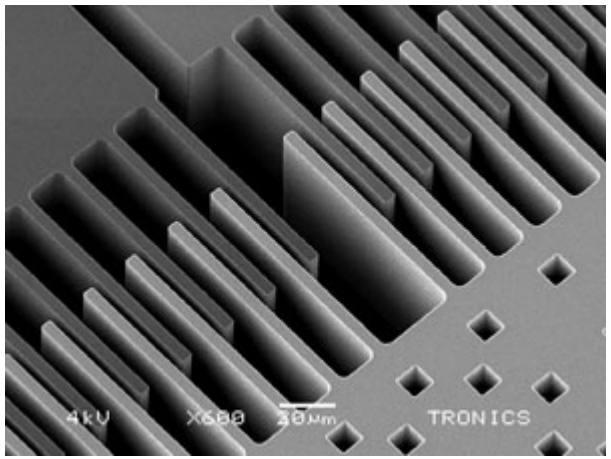
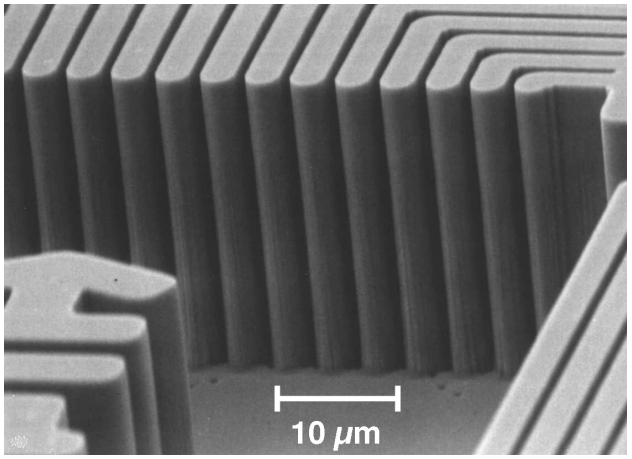
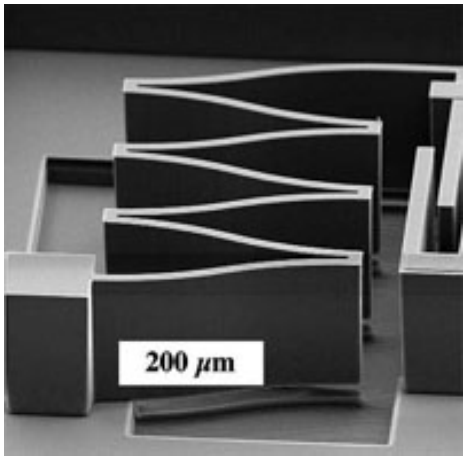
Motivation







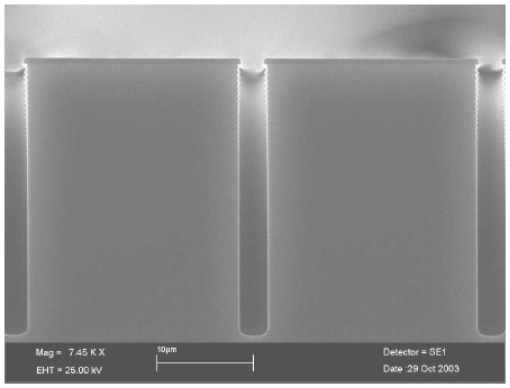
- Applications of DRIE:
  - MEMS (accelerometers, micromotors, etc)♪
  - Optical MEMS (scanners, optical switches, etc)
  - Microfluidic channels and ports
  - Electrical through wafer interconnects
- High aspect ratio etching for design flexibility and high device performance

Overview

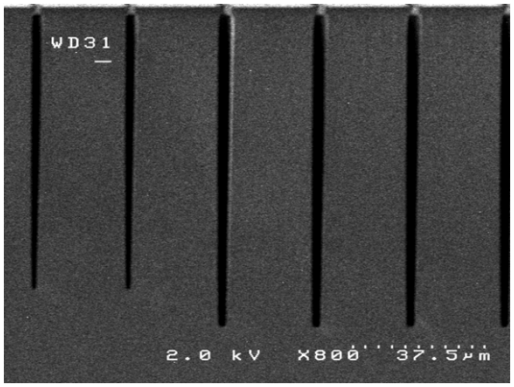
- Background for STS2 process
- Recipes for different purposes:
  - HAR recipe
  - Low frequency bias recipe for SOI wafer process
  - Low power recipe for low temperature process

Background

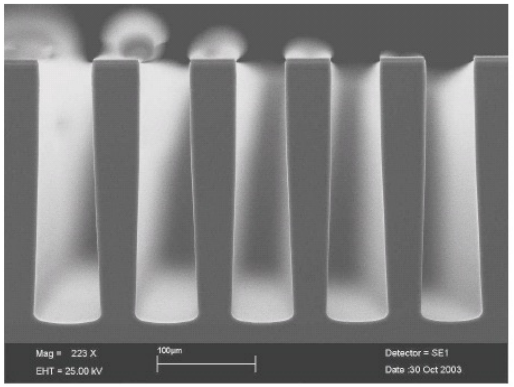
- Deep Reactive Ion Etch (DRIE) Profile



Vertical profile



Positive slope (V-shaping)



Negative slope (Reentrant)

- Summary of STS2 process trends

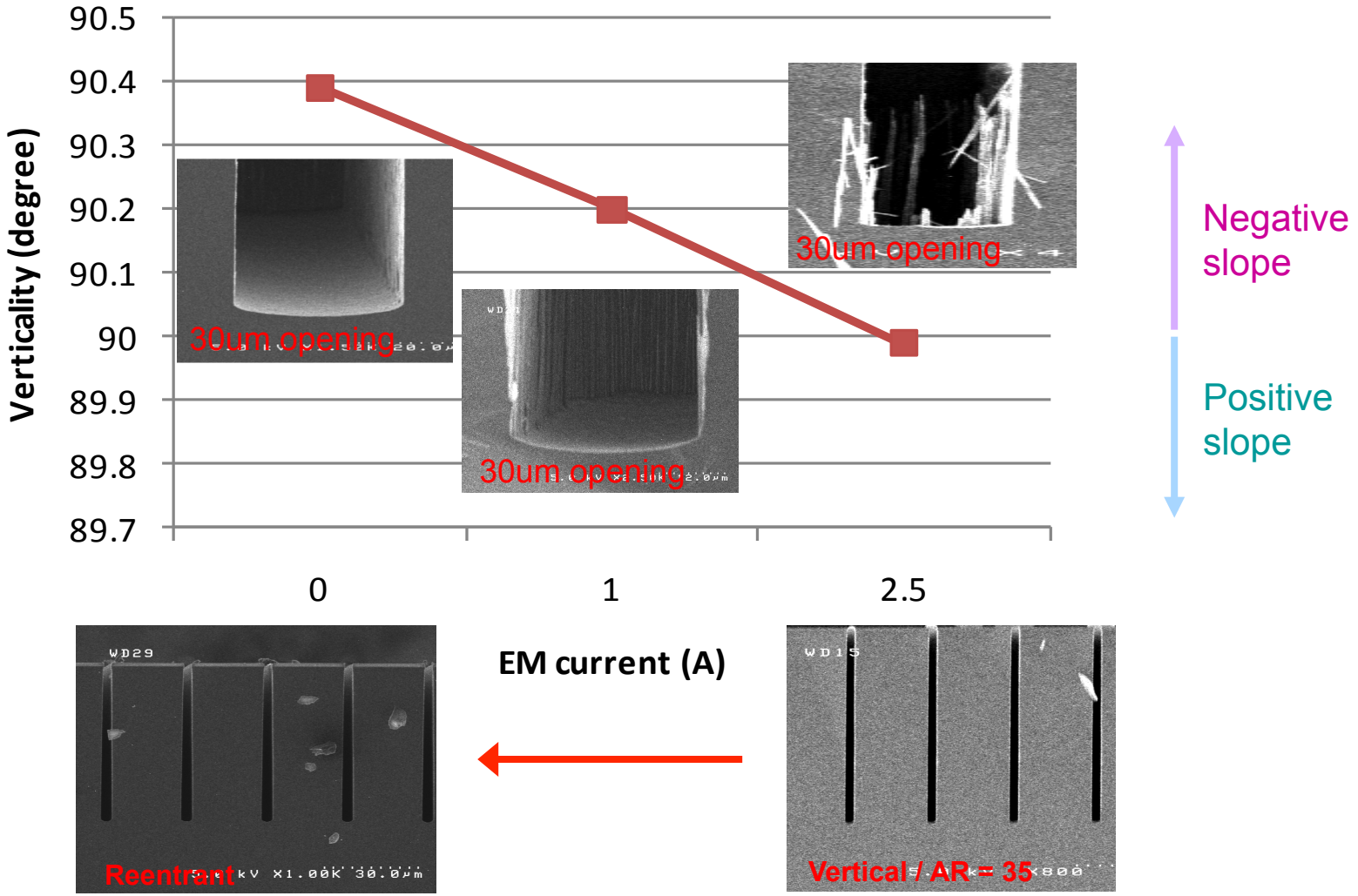
Trends for Controlling process results	Etch rate	Profile (↑ negative) (↓ positive)	Selectivity	Grass	Breakdown	Sidewall Roughness
Etch gas increase	↑↑	↑↑	↑	↓	↑	↑
Dep gas increase	↓↔	↔	↑	↑	↓↔	↓
Etch:Dep time ratio increase	↑	↑	↑↔	↓	↑↔	↑
Pressure increase	↑↑	↑	↑	↓↔	↑	↑
Dep Coil Power increase	↓↔	↓↔	↑↔	↑	↓↔	↓
Etch Coil Power increase	↑	↑	↑	↓	↑	↑
Platen Power increase	↑↔	↑↔	↓	↓	↔	↔
EM1 value (e) increase	↓↔	↓↔	↑	↑↔	↓↔	↔
EM1 delay (e) increase	↑↔	↑↔	↓	↓↔	↑↔	↔

HAR (High Aspect Ratio) Recipe

HAR – Influence of EM Current

HAR Recipe – tried different EM current

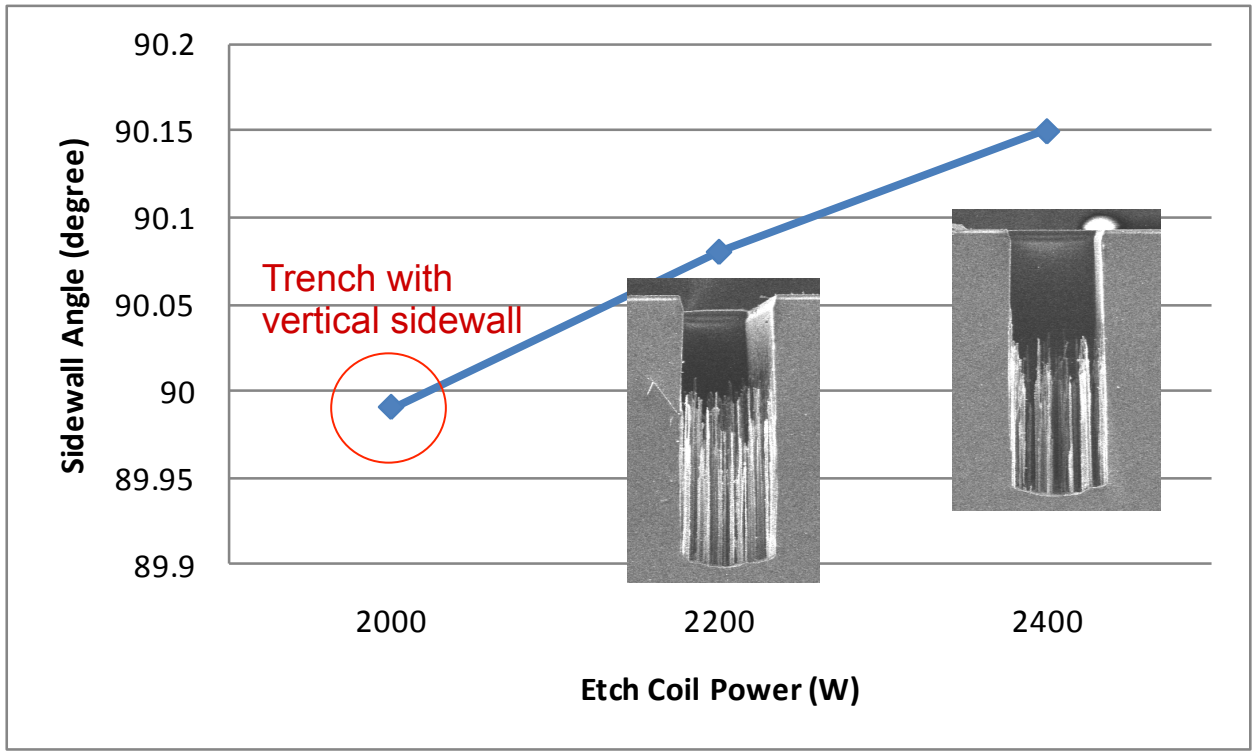
SF6/O2 Flow (sccm)	C4F8 Flow (sccm)	Etch Cycle Time (s)	Dep. Cycle Time (s)	Pressure (pass/etch)	Coil Power (pass/etch)	Platen Power (pass/etch)	EM/Delay	Temp
200/20	200	3.5	3	12%/26%	1200W/2000W	0W/85W HF	2.5A/2s	10C
200/20	200	3.5	3	12%/26%	1200W/2000W	0W/85W HF	1A/2s	10C
200/20	200	3.5	3	12%/26%	1200W/2000W	0W/85W HF	0A/0s	10C



HAR – Influence of Coil Power

- Enhanced coil power increases etch rate
- Increased coil power → bottle-shaped profile / reduced grass

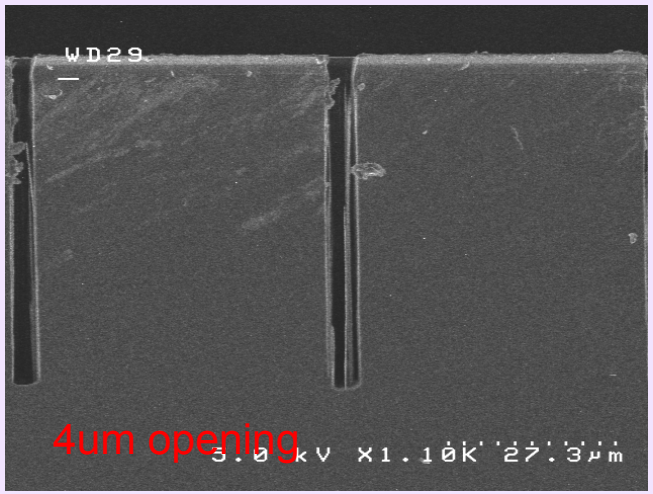
SF6/O2 Flow (sccm)	C4F8 Flow (sccm)	Etch Cycle Time (s)	Dep. Cycle Time (s)	Pressure (pass/etch)	Coil Power (pass/etch)	Platen Power (pass/etch)	EM/Delay	Temp
200/20	200	3.5	3	12%/26%	1200W/2200W	0W/85W HF	2.5A/2s	10C
200/20	200	3.5	3	12%/26%	1200W/2400W	0W/85W HF	2.5A/2s	10C

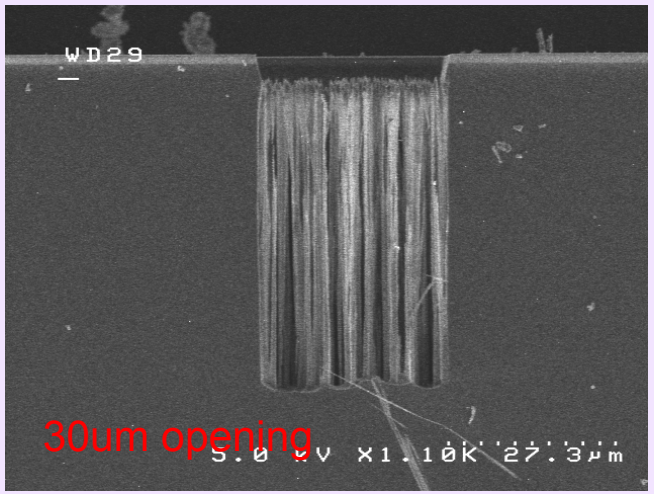


HAR – Influence of Temperature

SF6/O2 Flow (sccm)	C4F8 Flow (sccm)	Etch Cycle Time (s)	Dep. Cycle Time (s)	Pressure (pass/etch)	Coil Power (pass/etch)	Platen Power (pass/etch)	EM/Delay
200/20	200	3.5	3	12%/26%	1200W/2000W	0W/85W HF	2.5A/2s

10°C	20°C
▪ Grass starts to appear from 12~14 um-wide trench ▪ Sidewall angle ~ 90°	▪ Grass starts to appear from 4um-wide trench ▪ Sidewall angle ~ 90.2°

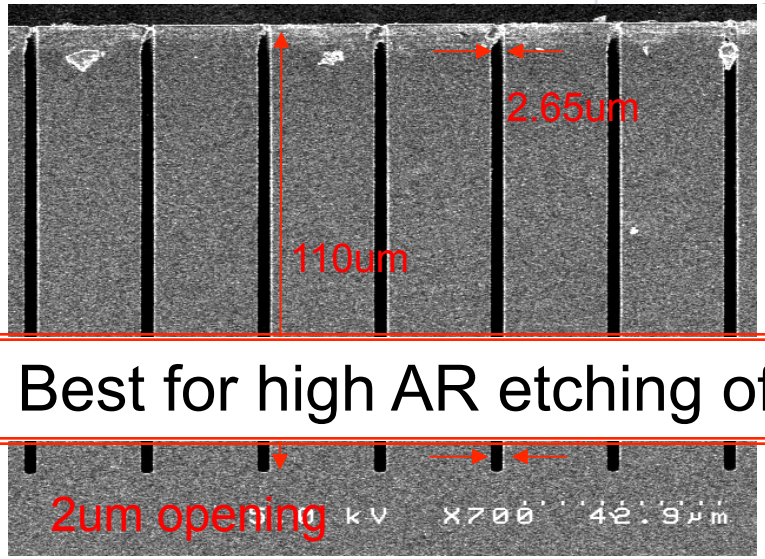


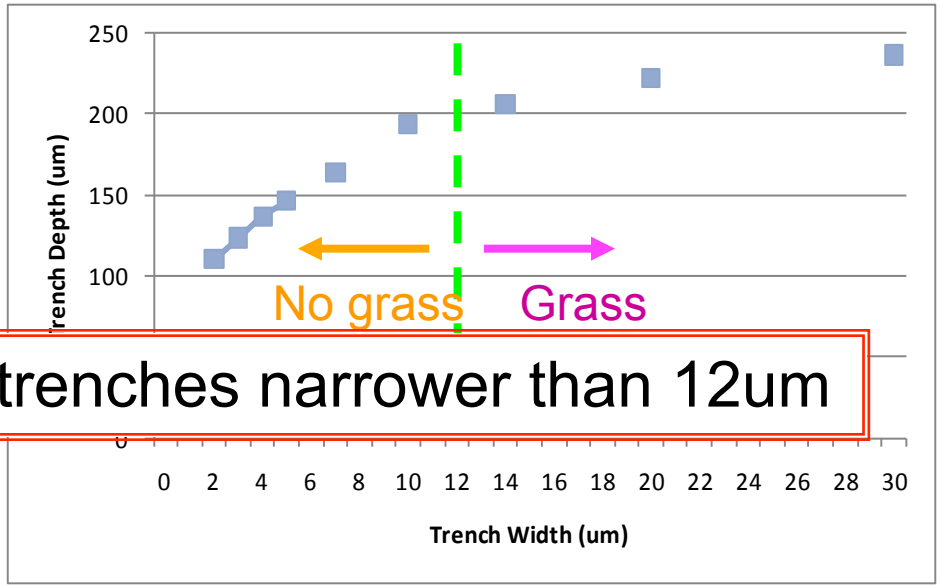


Optimized HAR for Vertical Sidewalls

Optimized Recipe

SF6/O2 Flow (sccm)	C4F8 Flow (sccm)	Etch Cycle Time (s)	Dep. Cycle Time (s)
200/20	200	3.5	3
Pressure (pass/etch)	**Coil Power (pass/etch)**	**Platen Power (pass/etch)**	**EM/Delay**
12%/26%	1200W/2000W	0W/85W HF	2.5A/2s





Best for high AR etching of trenches narrower than 12um

From three samples after 550cycles,

- Average AR = 41.71 (Goal achieved!)
- Standard Deviation of AR = 0.28

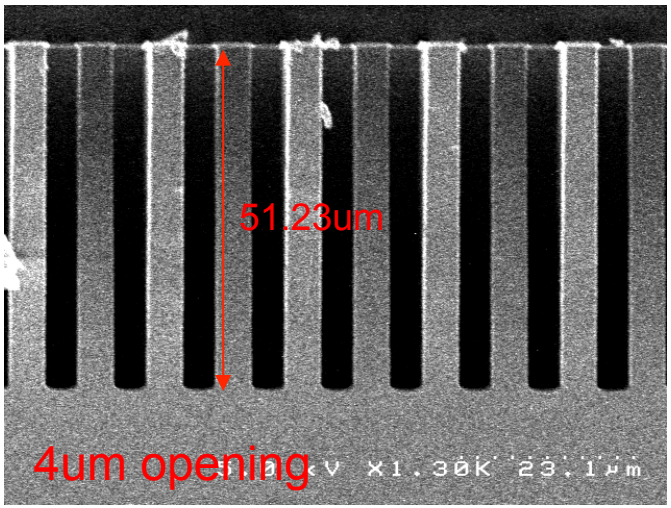
- Verticality = 89.99°
- Undercut ~ 350nm
- Sidewall roughness ~ 150nm

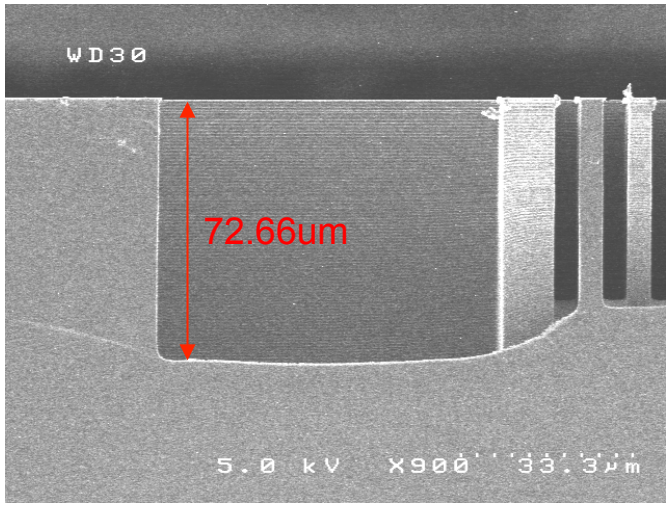
Low Frequency Bias Recipe

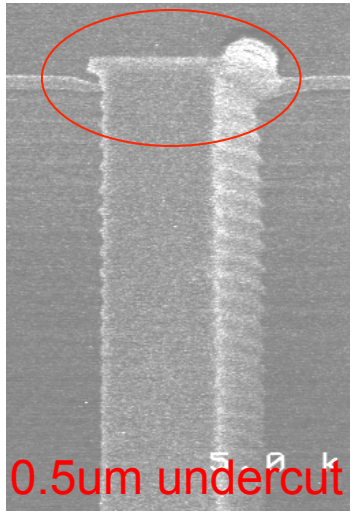
Low Frequency Bias Recipe

- LF bias recipe for SOI use

SF6/O2 Flow (sccm)	C4F8 Flow (sccm)	Etch Cycle Time (s)	Dep. Cycle Time (s)	Pressure (pass/etch)	Coil Power (pass/etch)	Platen Power (pass/etch)	EM/Delay	Temp
450/45	100	3	2	15%/15%	1000W/2400W	0W/45W	0A/0s	10C

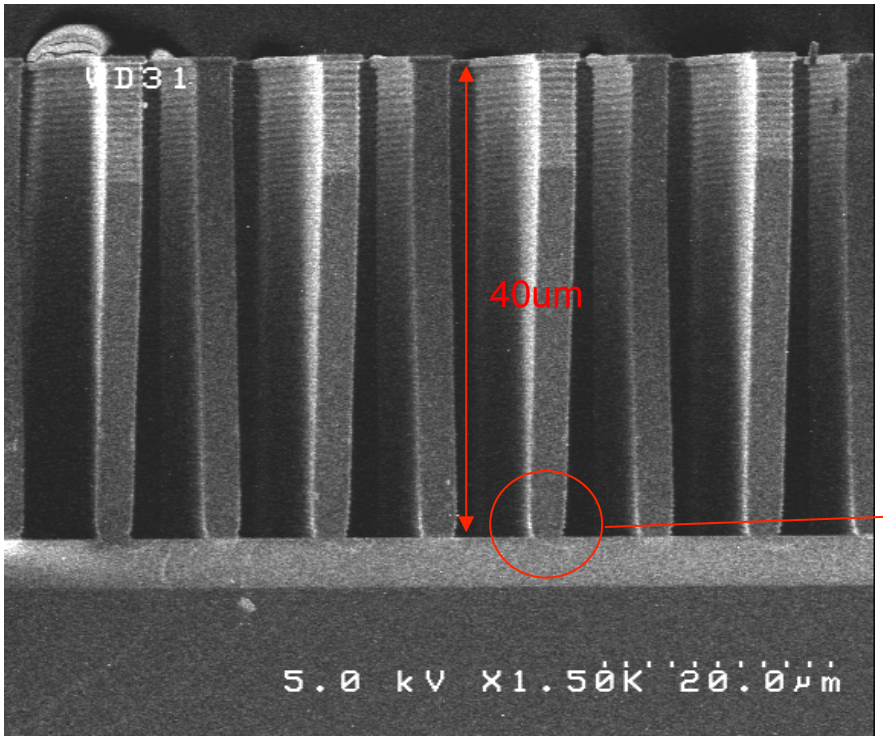


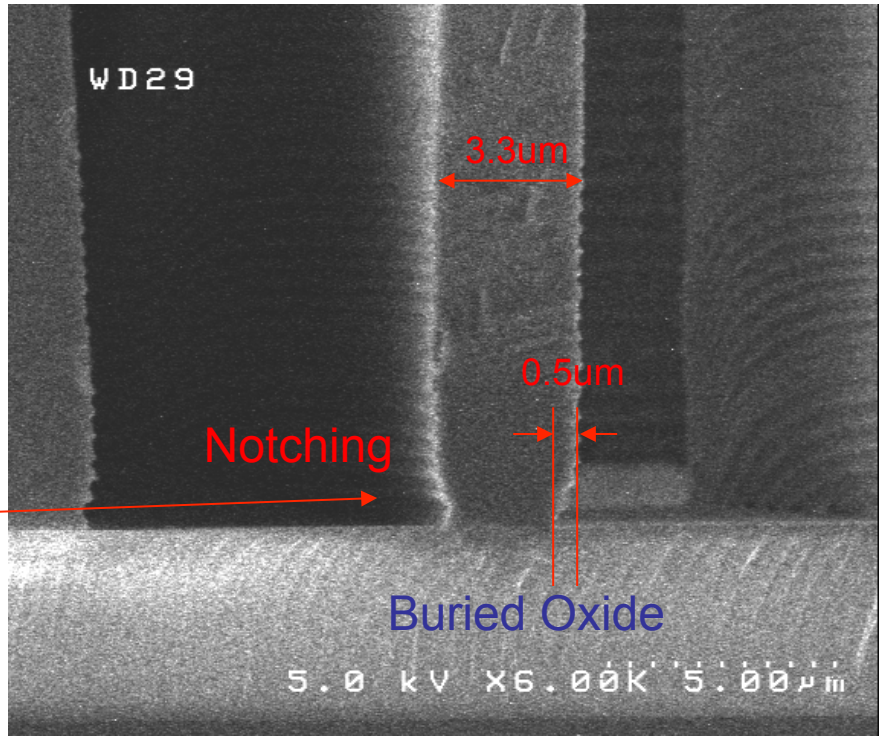




- Etch rate = 6um/min for 4um-gap trench
- Selectivity – Si:Ox = ~420:1
- Sidewall angle = 89.97° for 4um gap trench
- No grass found in 1.8mm X 1.8mm trench with 300um depth

Notching characteristics

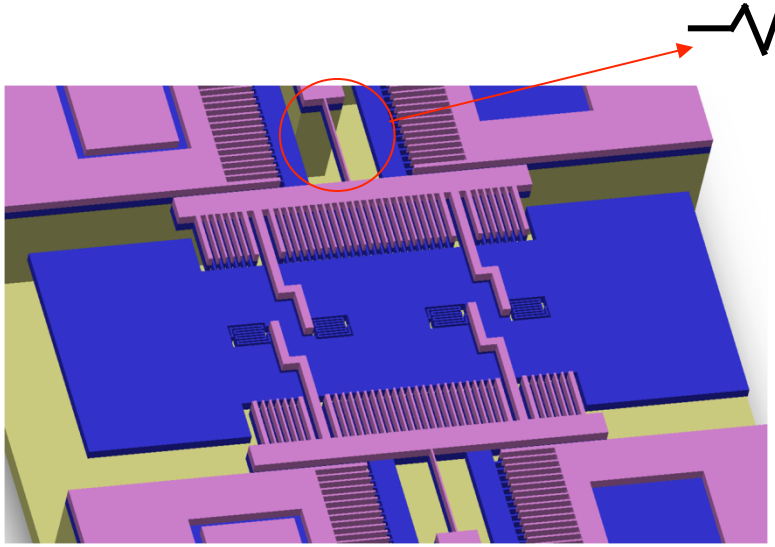




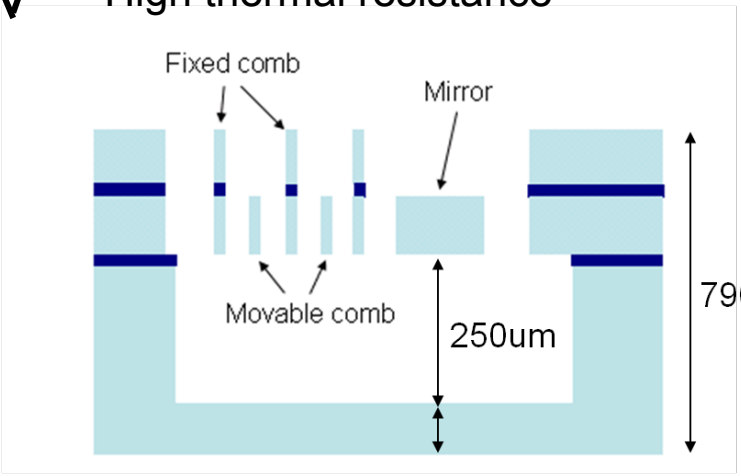
- 0.5um notching by 20% overetching

Low Power Recipe

Motivation toward Low Power Recipe

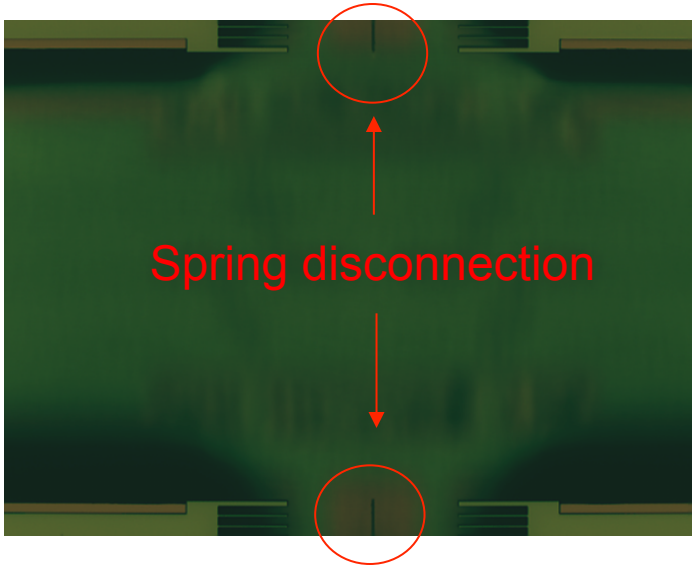


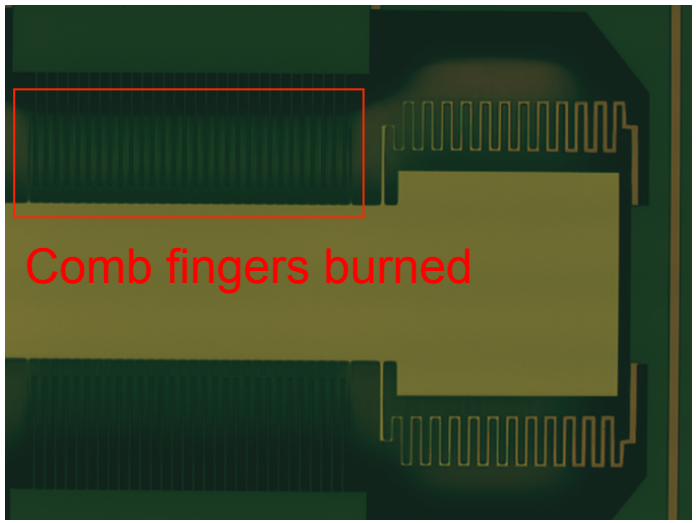
High thermal resistance



Cross-section of micromirror

Structure disconnections due to Si burn during STS2 etching

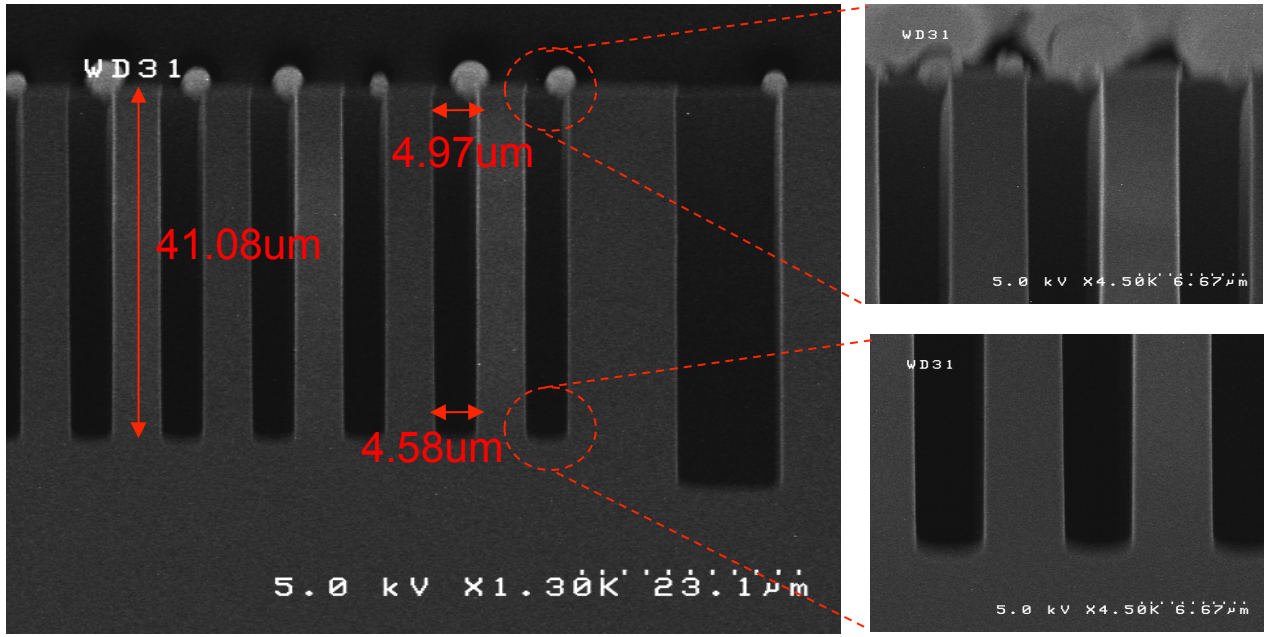




Low Power Recipe

- Low power recipe for reduced heating during etching

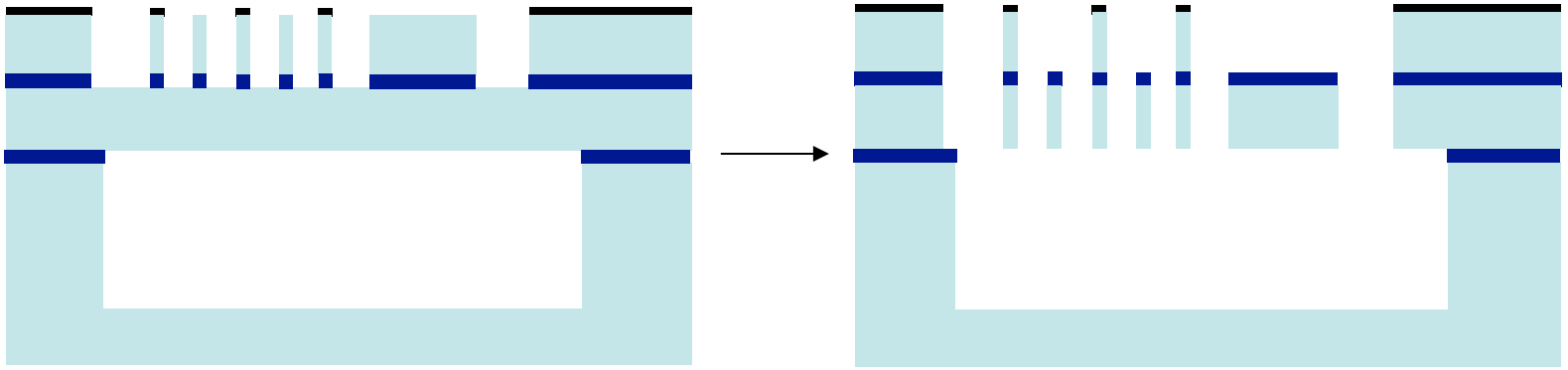
SF6/O2 Flow (sccm)	C4F8 Flow (sccm)	Etch Cycle Time (s)	Dep. Cycle Time (s)	Pressure (pass/etch)	Coil Power (pass/etch)	Platen Power (pass/etch)	EM/Delay	Temp
450/45	100	3	2	15%/15%	1000W/1500W	0W/45W	0A/0s	10C



- Etch rate = 4.89um/min for 4um-gap trench
- Selectivity – Si:Ox = ~580:1
- Sidewall angle = 89.93° for 4um gap trench

Low power DRIE

Two step etching to solve the heating problem

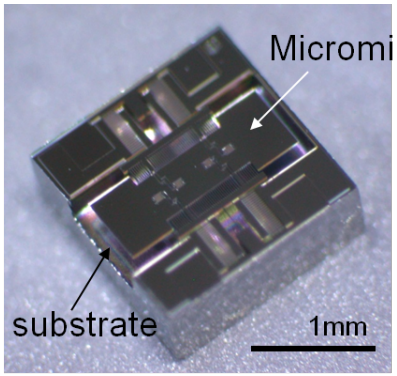


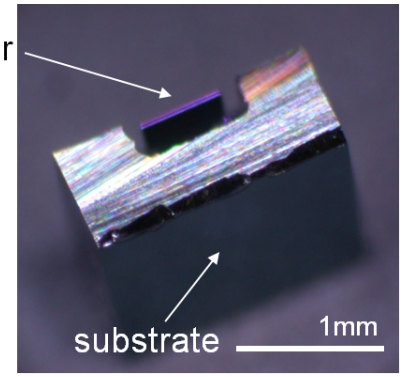
1. Top device layer etching:
Coil power = 2400W in LF bias recipe

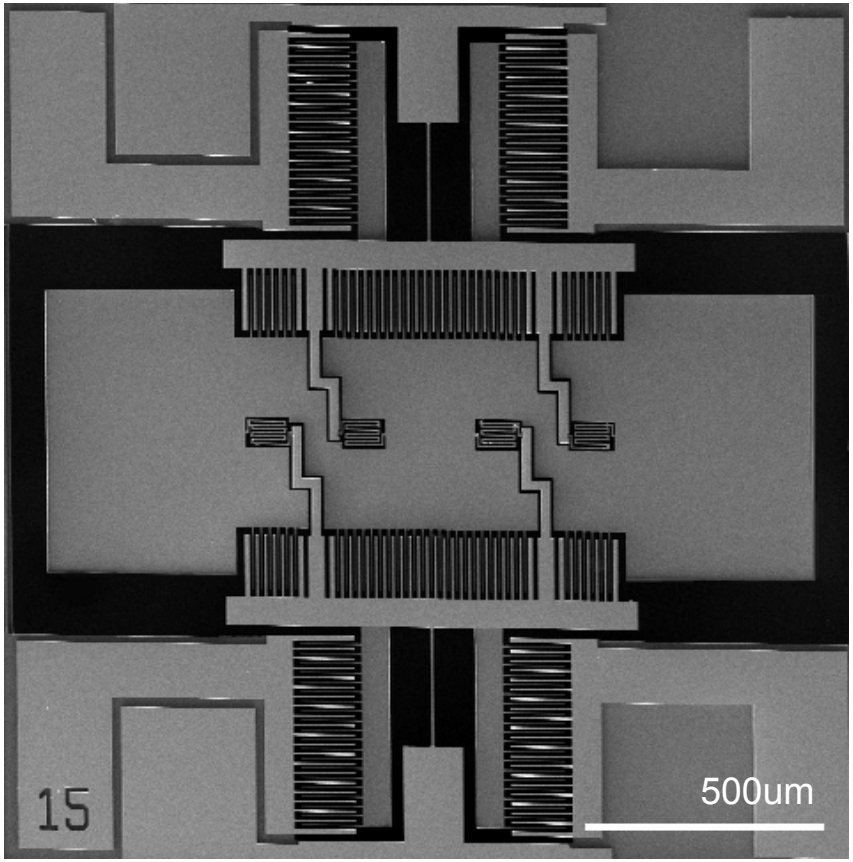
2. Bottom device layer etching
Three step etching in Coil power = 1500W

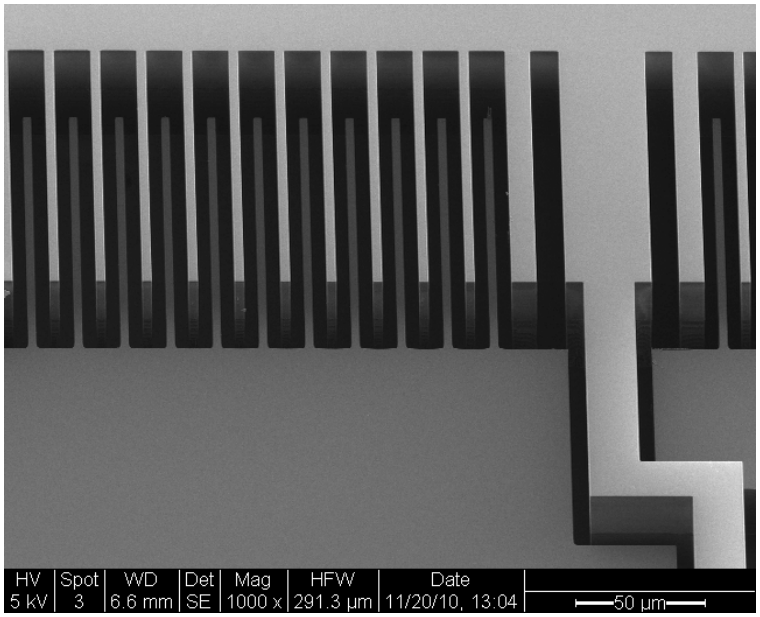
Etch → Cool → Etch → Cool → Etch

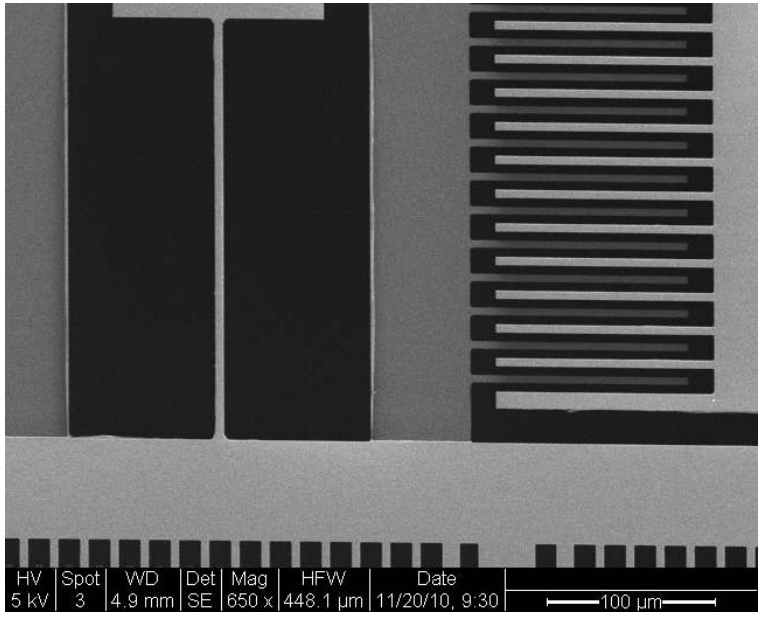
Image of fabricated MEMS scanner











Conclusion

- High aspect ratio recipe has been developed
  - HAR
    - AR of 41 for 2um-gap trench
    - No grass for trench narrower than 12um
  - Low frequency bias recipe for processing SOI wafers
  - Low power recipe to minimize the heating problems in STS2
    - Good for etching Membrane structures

Thank You!