Standard Process for Prototyping Flexible Devices

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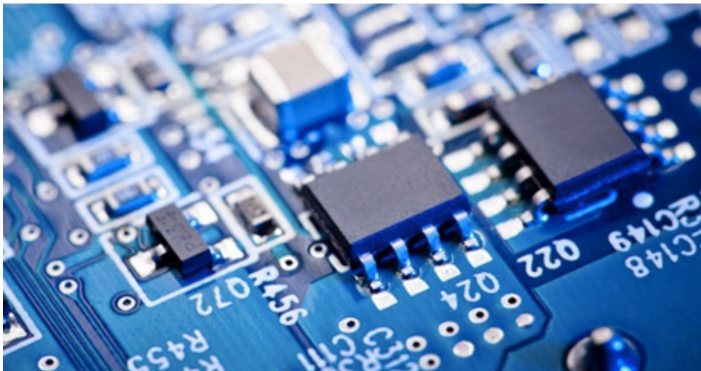
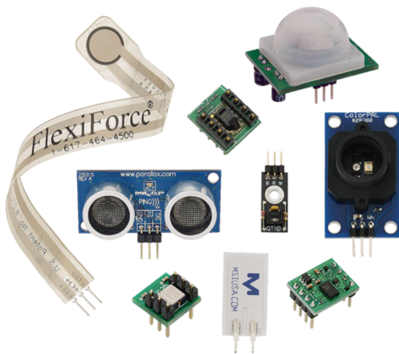
Introduction

We are focusing on the field where flexible electronics meet stretchable devices.

PRESENT



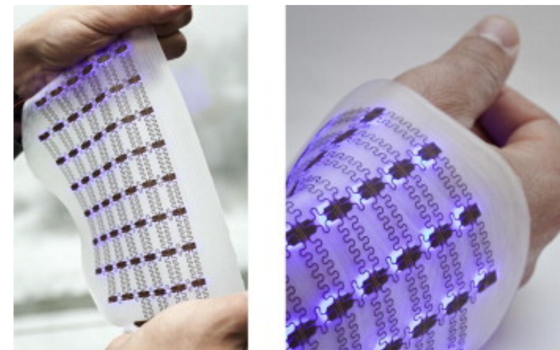
Rigid and planar integrated electronics



Separate sensors without connections

FUTURE

“Unbreakable” flexible and bendable displays



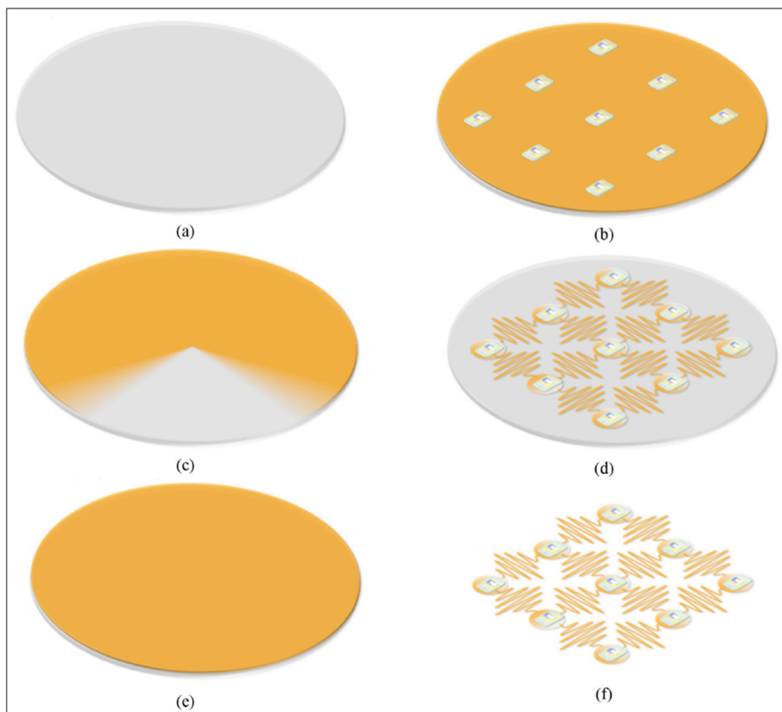
Sensors connected into stretchable network

van den Brand, Jeroen, et al. "Flexible and stretchable electronics for wearable health devices." *Solid-State Electronics* 113 (2015): 116-120.

Prototyping Process Development

Current process for fabricating stretchable network developed by Structures and Composites Laboratory (SACL) at Stanford University.

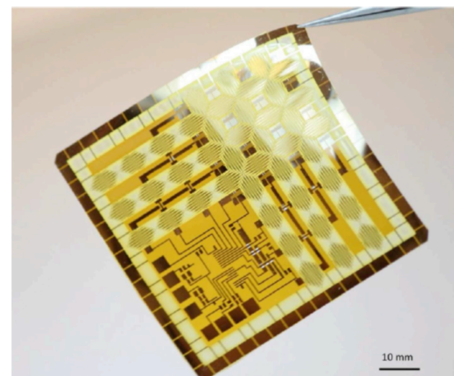
- Wafer preparation
- Release methods
- Photolithography
- PI patterning



Issues with the current process:

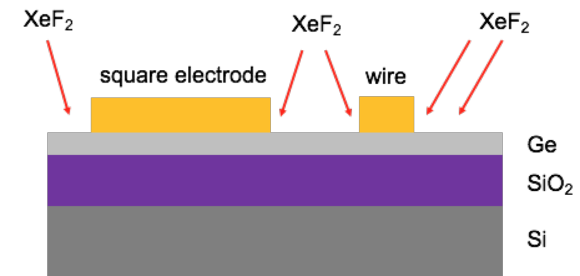
- ❖ Time - consuming
- ❖ Costly

Goal:
General process for all users, starting from existing process



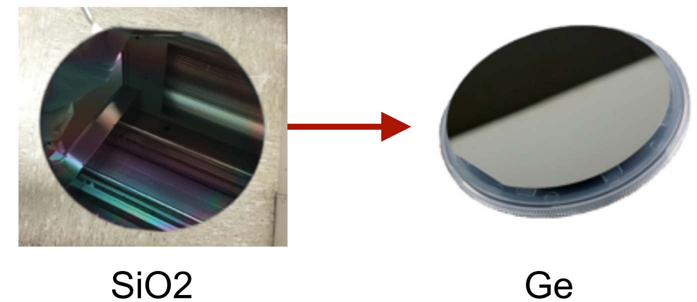
Guo, Zhiqiang, et al. "Functionalization of stretchable networks with sensors and switches for composite materials." *Structural Health Monitoring* (2017): 1475921717709632.

Wafer Prep, Release Methods



Dry Etch Method (Ge - XeF2, ~5um/min)

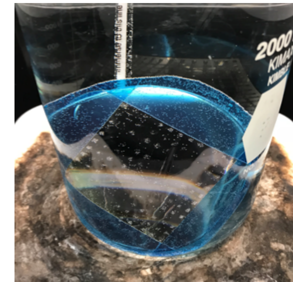
- 1.5 um SiO2 and 300nm Ge
- "SiO2 + Si" wafer can be purchased (lead time)
- Ge wafer is available but high cost (~$200)
- Manual Process for SiO2 + Ge
  - CVD for SiO2 and E-beam dep for Ge

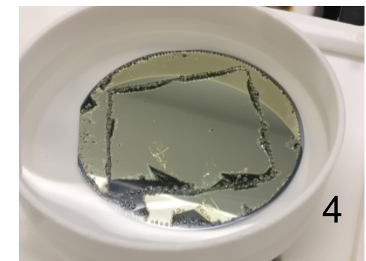


SiO2 Ge

Wet Etch Method

- Ge-H2O (60C) : Ge-H2O2 known to 460nm/min etch rate.
- Al- HF (250nm/min) : Bubbles tear user process if too thin.
- **Wet etch cause stiction** → Critical Point Dryer needed (time consuming)
- Water or acetone soluble layers: limited process compatibility





Polyimide (PI) Patterning

O2 Plasma etch with Al Masking from lift-off

- Finer resolution of features.
- Multiple steps required (PR- Expose - Dev - Al dep - LIft-off - O2 Plasma)

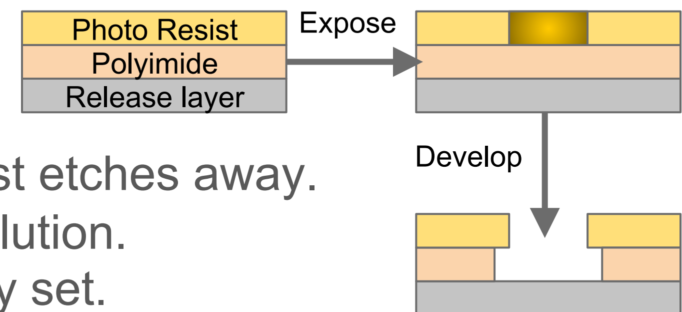


Photo-Patternable PI (PI 2545)

- Polyimide Patterned as the overlying photoresist etches away.
- Easy, fast prototyping ⇔ undercutting, low resolution.
- Dose and Development time should be carefully set.

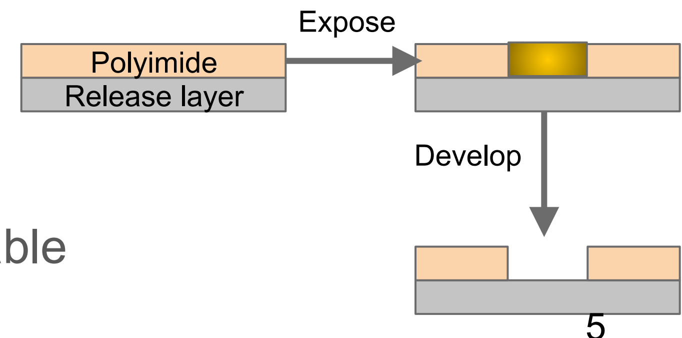


Photo-Definable PI (HD 4110)

- The polyimide is exposed and developed.
- No undercut issue
- 5-10 um thickness → thicker than photo patternable
- Manual develop needed (PA401-D)

Photo Patternable PI - Recipe and Dose

PI 2545 Recipe-

1. VM-652 Adhesion Promoter -spin coat 5000RPM, 20sec
2. PI2545 : T9039 = 1:2, spin coat 2000RPM, 60sec
3. Hotplate 140C 10min

Photoresist - Shipley 3612 - 1um

Maskless Expose (Heidelberg) - Dose Matrix.

Dose [55: 5: 100]mJ/cm^2 , Defoc [-3:1:0]

Develop - 2x 6sec (SVG DEV)

Negative Test Positive Test
2um to 128um feature sizes.

Smallest Feature size (Square)

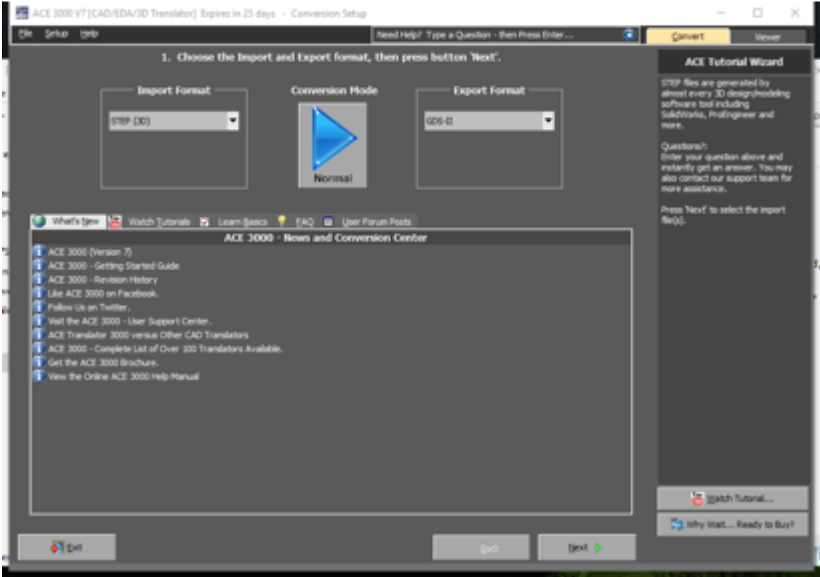
Dose	Negative	Positive
75	8um	4um -undercut of 1.0um
80	16um	4um- undercut of 1.2um
85	16um	4um - undercut of 2.1um

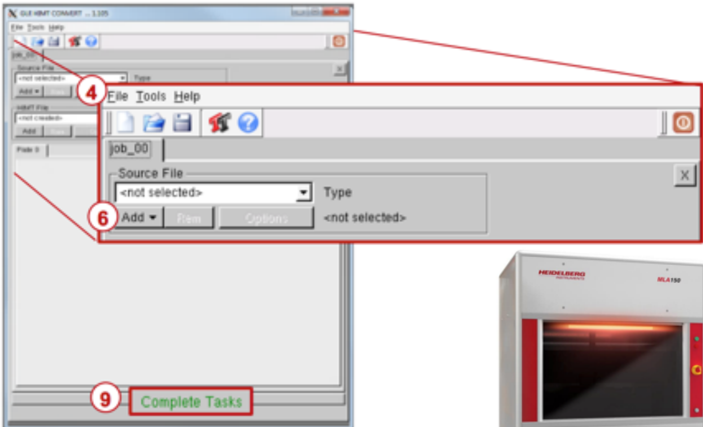
Dose & Development time

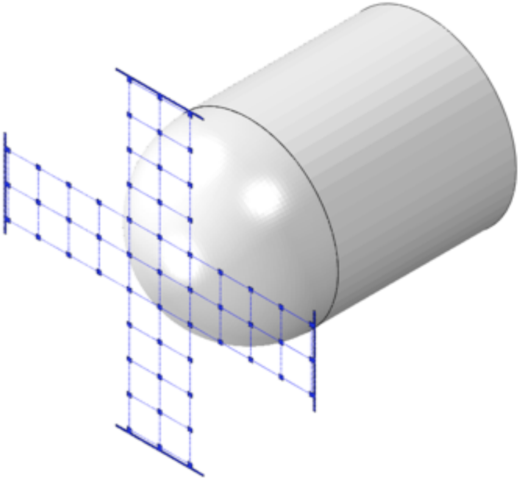
Dose (mJ/cm^2)	Develop	Description
75	2 x 6sec	Center - Ok, Peripheries - Under develop.
75	2x6sec + 2x6sec	Fully developed, Undercut of 8.5 um (center), 4.9 um (peripheries)
85	2 x 6sec + 2x1sec	Fully developed, Undercut of 6.1um(center), 2.5 um (peripheries)

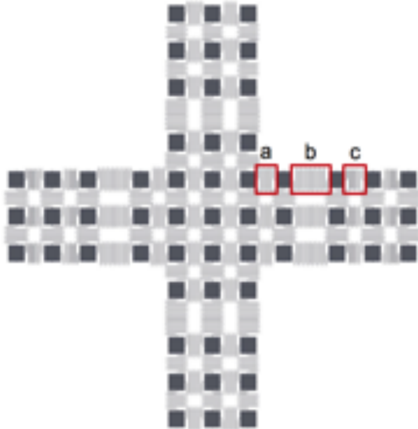
Transition from FEA 3D Simulation to Microfabrication

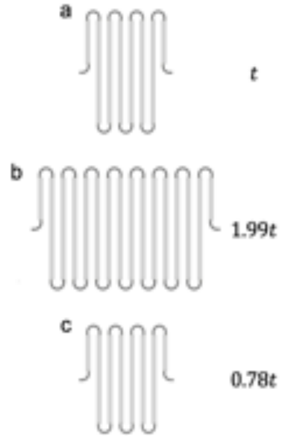
ACE 3000 Translator ($75/month)





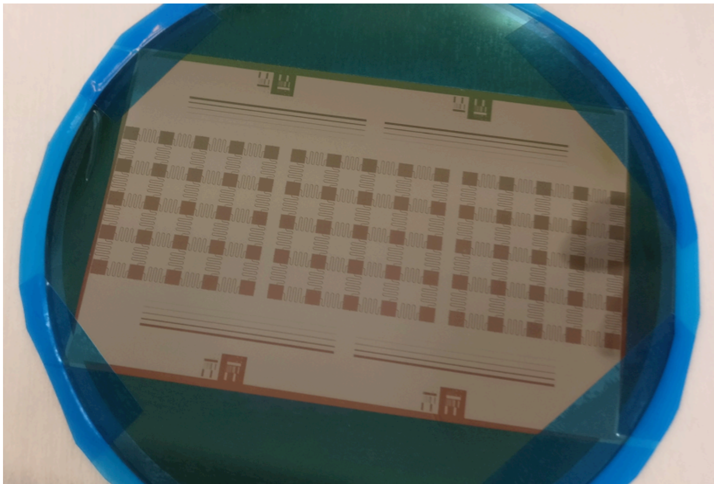


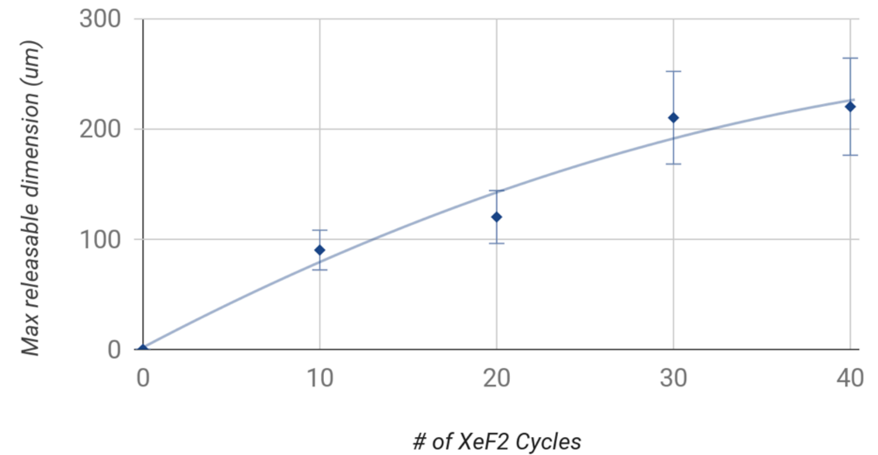


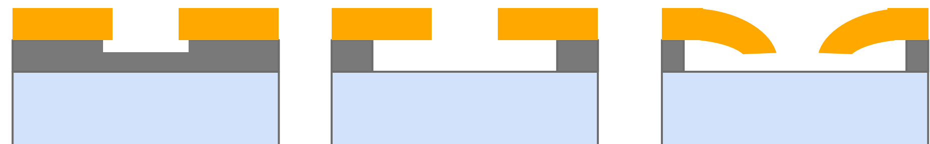


XeF2 Release Characterization

Photo-patternable PI structures with edge-to-edge dimension of 100um or less can be fully released in 30 cycles of XeF2



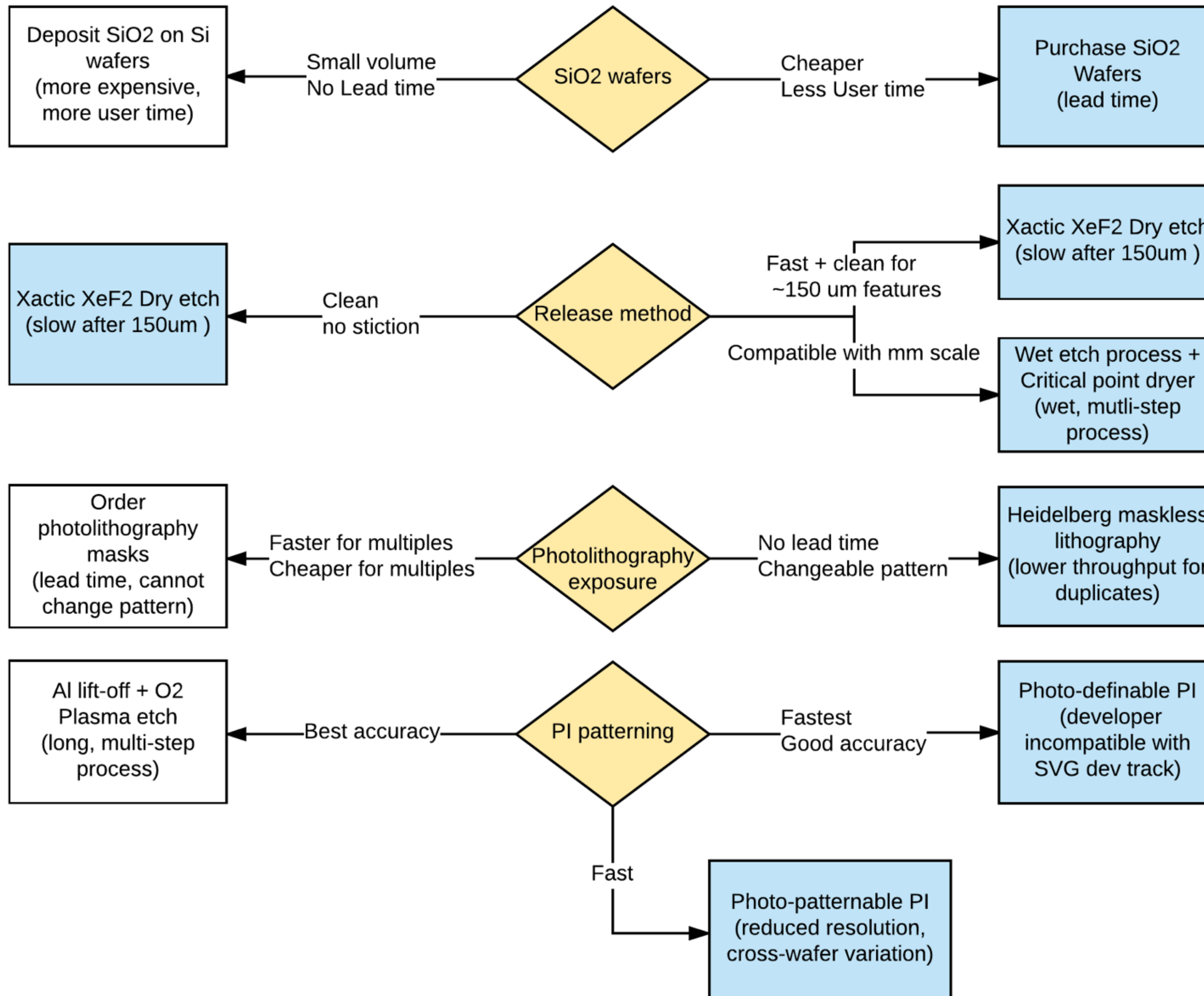




Etch rates decrease as the XeF2 needs to travel laterally beneath the structures

- May be further slowed by deflection of PI layer

Release holes can be added to expedite release of large areas

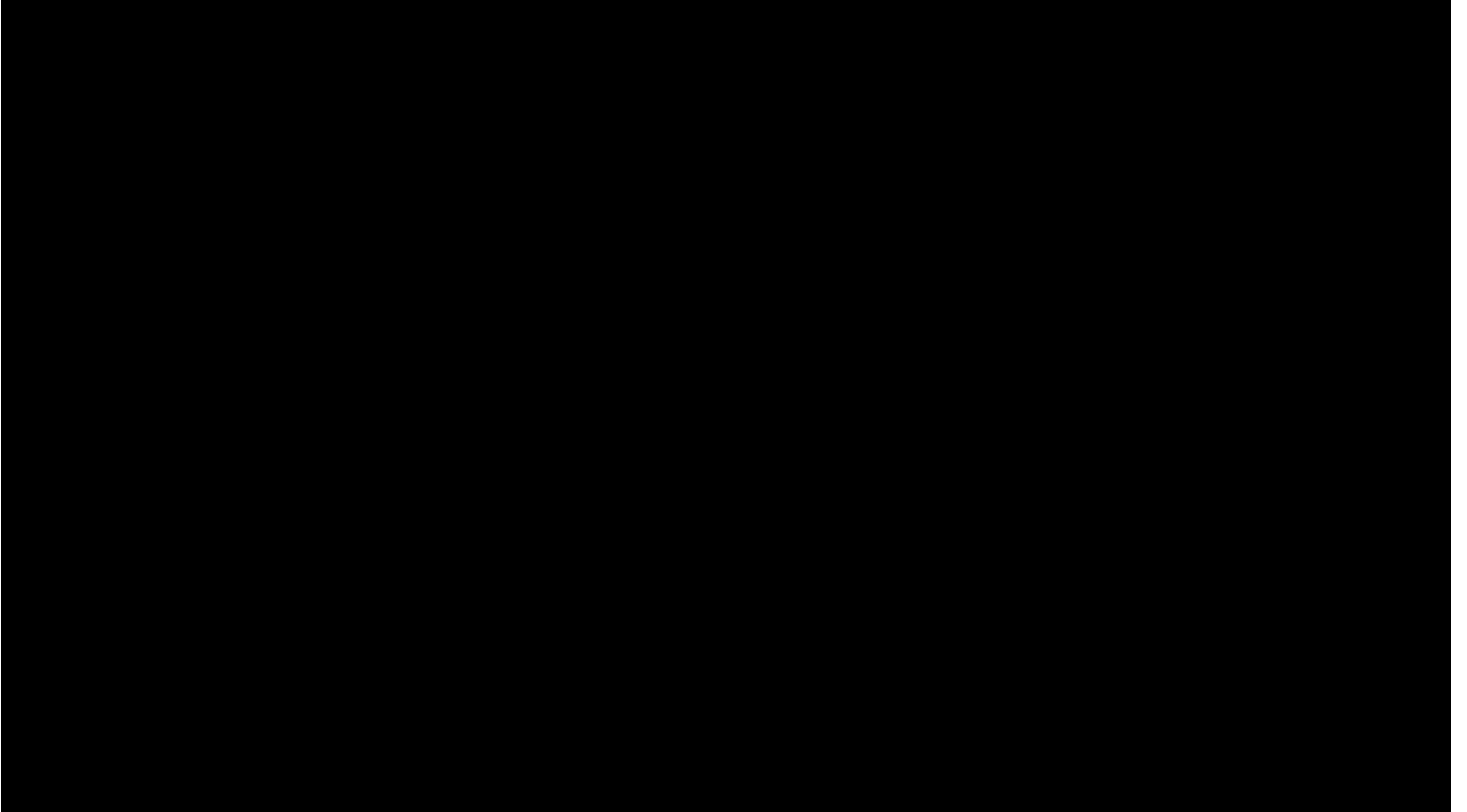

Maximum Quality
Quickest Prototyping
Deposit SiO2 on Si wafers (more expensive, more user time)
Small volume
No Lead time
SiO2 wafers
Cheaper
Less User time
Purchase SiO2 Wafers (lead time)
Xactic XeF2 Dry etch (slow after 150um)
Clean
no stiction
Release method
Fast + clean for ~150 um features
Xactic XeF2 Dry etch (slow after 150um)
Compatible with mm scale
Wet etch process + Critical point dryer (wet, mutli-step process)
Order photolithography masks (lead time, cannot change pattern)
Faster for multiples
Cheaper for multiples
Photolithography exposure
No lead time
Changeable pattern
Heidelberg maskless lithography (lower throughput for duplicates)
Al lift-off + O2 Plasma etch (long, multi-step process)
Best accuracy
PI patterning
Fastest
Good accuracy
Photo-definable PI (developer incompatible with SVG dev track)
Fast
Photo-patternable PI (reduced resolution, cross-wafer variation)

Comparison - Old vs New

Main Process	Old Method	New Method	Time	Cost	Feature Size
Wafer preparation	LPCVD growth of SiO_2 on Si wafer	Purchase SiO_2 wafers	10 hrs → 4 hrs	\$60/wafer → \$49/wafer	N/A
Release method	Ge + XeF_2	Ge + XeF_2 + release facilitating holes	3-6 hrs → 1 hrs	\$270/wafer → \$60/wafer	N/A
Photolitho-graphy	KarlSuss Contact Aligner	Heidelberg MLA	Almost the same (2 min → 8 min/wafer)	Saved \$500/ mask	Almost the same (1 um vs 0.9 um)
PI patterning	PI2611+Al mask+O_2 plasma	PI2545 photopatternable	10 hrs → 2 min	Saved ~\$400/wafer	2 um → 20 um

In total, we saved **10.5 hrs** and **\$620** per wafer with the new process we developed!

Network Stretching and Integration



1-Page summary for processes

Wafer preparation

Purchase 1.5um oxide on Si wafer

Ge -- Tool: Innotec Thickness: Cr 100A Ge: 3000A Rate: Cr 0.5A/sec Ge: 2.2A/sec

Photolithography

ACE 3000 Translator (FEA layouts to GDS)
High complexity polygons can prevent layout from loading
- Ex. large areas with many polygons subtracted

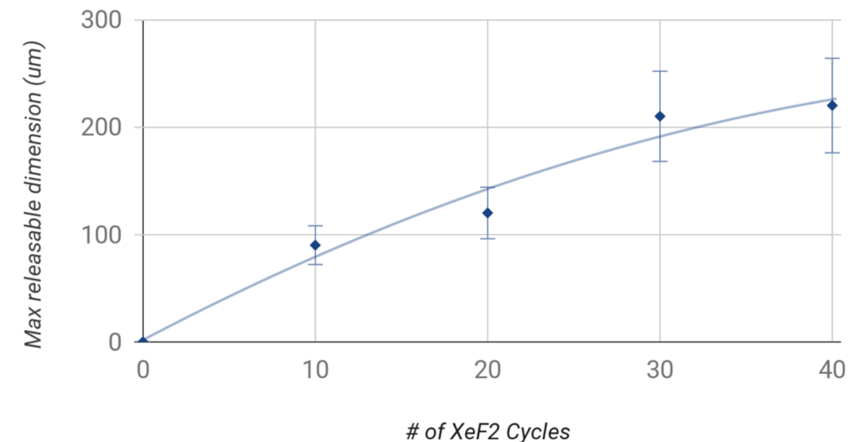
Photo-Patternable PI (PI 2545)

Spin Coat: Adhesion Promoter (VM-652) spin coat 5000RPM, 20sec
PI2545 : T9039 = 1:2, spin coat 2000RPM, 60sec
Hotplate 140C 10min
Exposure: 85 mJ/cm^2
SVG Dev: 2 x 7sec

Ge dry release

Xactic etch
30s/cycle 3mTorr

Recommended:
30 cycles to etch 100um
Release holes for large areas



Thanks for your attention!

Any questions?