ALD on MoS_2 using Seed Layer Deposition & Characterization of Oxidized Seed Layer with ALD Aluminum Oxide

Standard Operating Procedures

ENGR 241 Fall of 2019/2020

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Table of Contents

1. **Introduction**
    a. **SOP motivation:** Making a CMOS compatible 2D devices has been limited because there are no dangling bonds at the surface of 2D materials. Using ALD to construct a top gated structure is difficult and it is required to do a treatment at the surface to create nucleation sites. Creating a metal seed layer using e beam evaporation is optimal since it does not damage the surface which is essential in few-layered 2D devices. However, there is currently no process flow in SNF to construct a top gated device and there has been no thorough study in characterizing the oxides composed of an oxidized seed layer and ALD deposited layer. Here, we introduce a process flow for top gating on 2D materials and for characterizing the layers' electrical properties.
    b. **SOP objective**: Standard operating procedures for seed layer aided ALD on 2D materials and 1. Quality check of ALD deposited oxides with seed layer for CVD-grown monolayer 2D materials (in our case, monolayer MoS_2) with AFM (roughness), 2. Electrical results comparison of the oxides with seed layer on Si substrate by making MIM structure

These SOPs are significant to the SNF members working on 2D devices, since top-gated structures have been limited due to difficulties using ALD which is essential for constructing CMOS compatible devices. From this SOP, ALD with seed layer deposited oxides can be well characterized in terms of electrical properties and on MoS_2 samples.

All the tools for the experiment and characterization has been done with the tools in SNF except 2D materials were provided from Pop group in Electrical Engineering.

Moreover, there will be a simple demonstration of top gated 2D devices: process flow of how to make a 2D FET device, and further characterization and optimization will be done for research in the future. It is recommended that 2D samples be stored in a dry box.

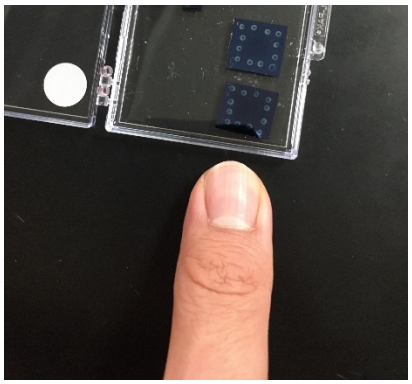
All data and scripts for processing the data are available: https://github.com/akashlevy/ENGR241-Q1

Dry box in Allen B103

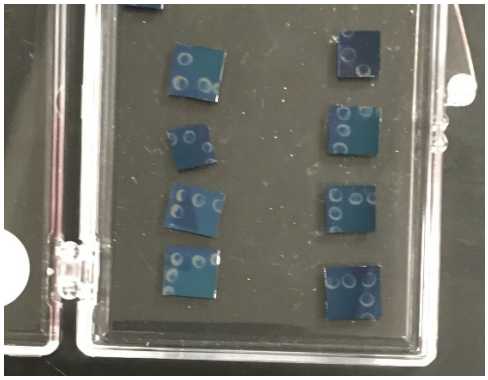
2. SOP

Seed Layer Deposition on CVD Grown monolayer MoS_2

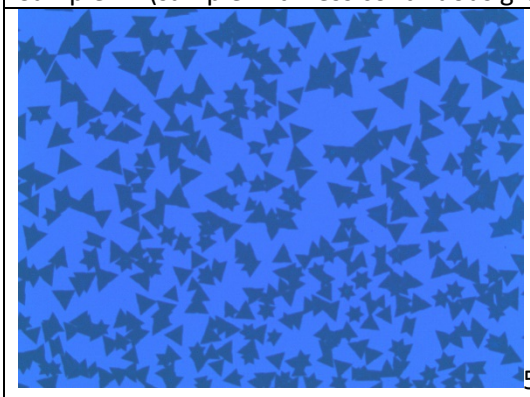
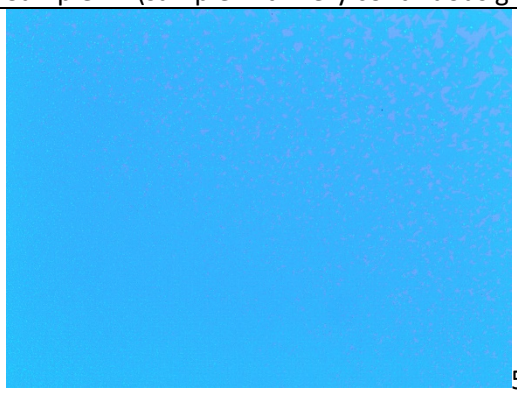
1. Get MoS_2 samples (CVD Grown) from Pop group
    a. Check the quality from optical microscope / AFM / SEM
    b. Quality varies from exfoliation / transfer / CVD-grown, so it should be checked before the experiment. Also, CVD-grown samples have variations as can be seen in the table below, so it is important to check them with microscopes in advance.
    c. Substrate roughness should also be checked since monolayer 2D materials will be deposited which has thickness of ~0.65nm. Roughness of the sample should be on the order of the sample substrate.
    d. Other CVD-grown 2D materials are also available in Pop group, so for any collaboration, contact Prof. Eric Pop. The chip size is ~1inch by 1inch. For more experiments to be done, it can be cleaved into pieces exactly as is done with Si wafers. The circles at the edges are Perylene-3,4,9,10-tetracarboxylic acid tetrapotassium acid salt (PTAS) which helps grow MoS_2 towards the middle. These parts are not considered important after the MoS_2 CVD process, so this may be a good position to place sample holders. PTAS contains Potassium, and some K is found at the surface of the samples (verified with Auger electron spectroscopy).

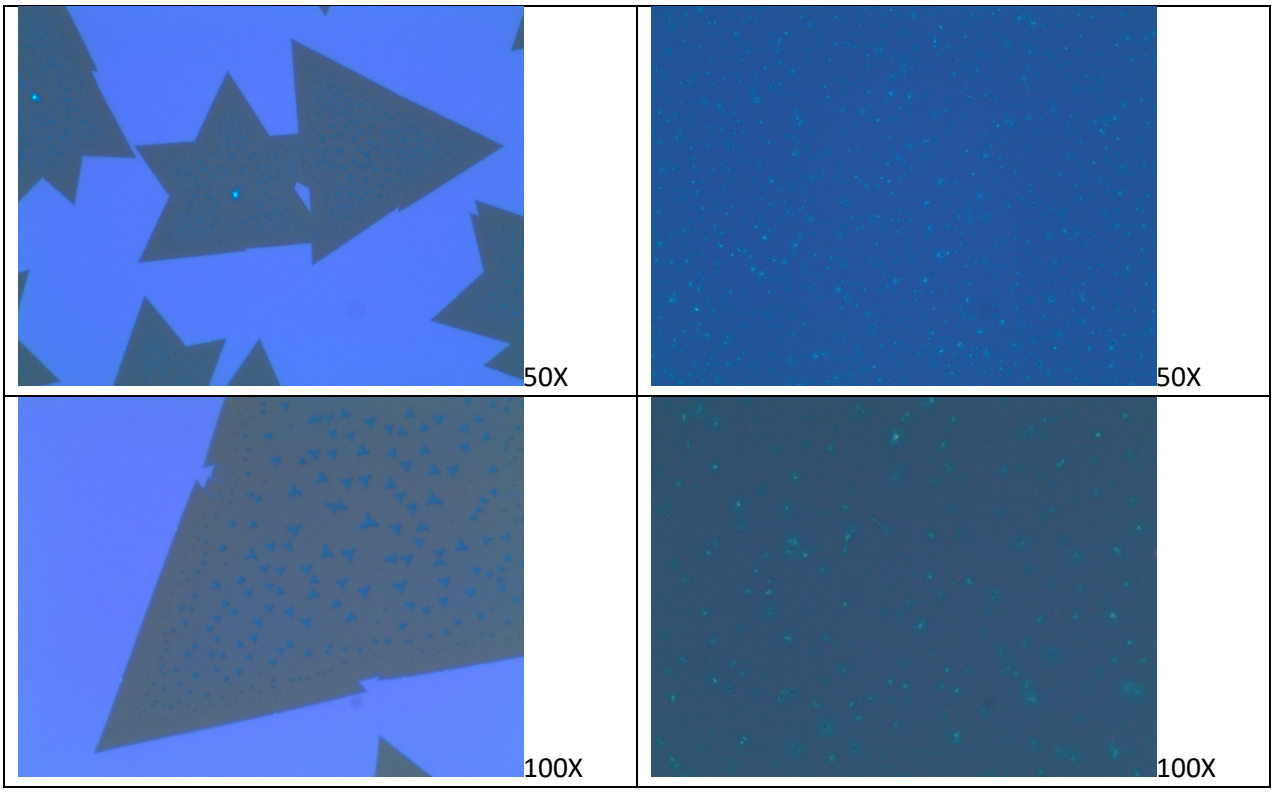


Two MoS2 CVD grown sample chips and chip size



MoS2 sample chips cleaved into 4 pieces

Sample #1 (sample with less continuous growth)	Sample #2 (sample with very continuous growth)
 5X	 5X



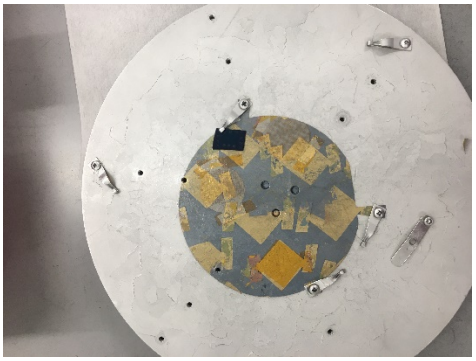
MoS2 samples under optical microscope to show sample variation

2. AFM / SEM on bare MoS_2 samples
    a. Since monolayer MoS_2 is being grown, the expected roughness should be approximately that of the underlying SiO_2/Si substrate. Small amounts of additional roughness are due to residues from MoO_3 involved in the growth process. This value may vary based on the substrates being used, and for our samples, the roughness before the deposition is measured to be ~200pm.
    b. Bilayer and grain boundaries can be seen, but no devices are made at the grain boundaries or bilayer regions, so measurement should be done on areas where it seems to be clean monolayer MoS_2.
    c. If the chip size is large, and we want to perform parallel multiple experiments, samples with 2D materials can be cleaved in the same way as Si wafers. Before any deposition on the samples, it is always a good practice to blow the surface of the samples with an N_2 gun to reduce the likelihood of dust causing problems.
3. E-beam evaporate metal on MoS_2 surface with AJA

a. Blow the surface of the samples with N_2 gun which is at the side of AJA

N2 gun placed at the side of AJA

b. Place the samples on the sample holder plate (multiple samples can be held)

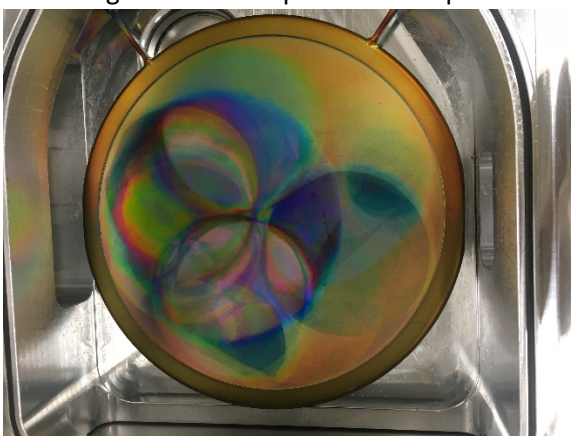


Samples placement: make sure it is attached firmly since the plate will be hanging upside down

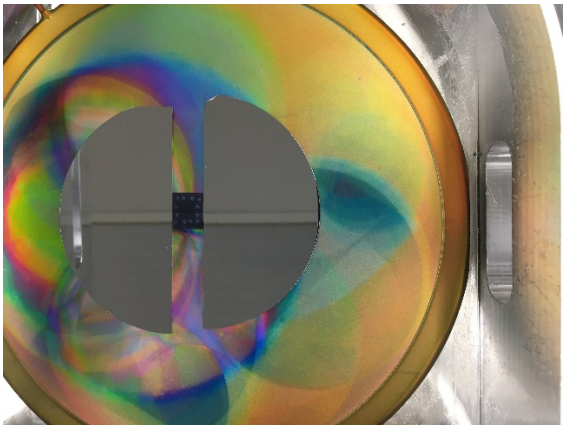
c. In case of aluminum, use the Al_0.2A/s deposition recipe.
    i. The deposition rate should be watched closely since this may be unstable from time to time.
    ii. The Al_0.2A/s is developed for thin Al film deposition, so use this recipe for seed layer deposition.
d. Deposit metal at the target seed layer thickness

4. Remove the samples from AJA. In the case of alumina, the seed layer will naturally oxidize; it has been verified from other group members that the full depth of the seed layer is oxidized for up to a 2nm seed layer using XPS.
5. AFM / SEM on the samples after e-beam evaporation
    a. Since 2D materials have not been well characterized with ellipsometry tools, thickness can be measured from step height from AFM. For our case, we determined the step height using equivalent experiments on Si substrate and extracting the thickness from that

6. ALD using standard recipe on 2D samples with Fiji 2



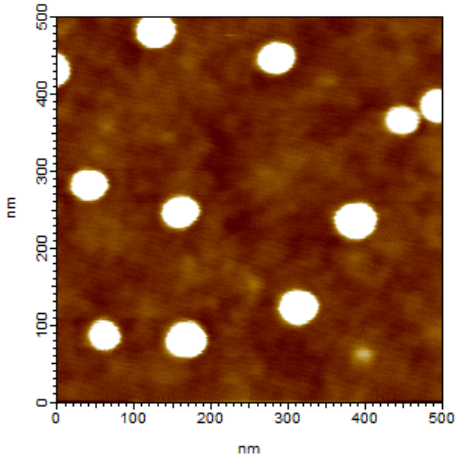
Inside Fiji 2 loadlock

7. 

Sample placement when using small pieces

    a. If samples are pieces, they can be put in load lock using pocket wafer (process for making one is in Fiji 1/2 wiki page). Another option which may be simpler is to put test wafers around the sample so that it does not move when loading and deposition process.
    b. When retracting the arm to drop the plate back at the chamber, it must be done carefully so that the sample does not move significantly. Otherwise, the samples may move a lot, or in the worst case, flip over.
8. AFM / SEM on the samples
    a. Measurement should be done at a small scan area, since using a larger scan window tends to average out roughness. Recommended window for small area scan is 500nmX500nm.
    b. Large scan area is helpful for understanding the surface topology, and helps identify and measure grain boundaries, bilayer regions, residues, pinholes, etc.
    c. During measurement, some areas seem to include multiple island-shaped dot regions. This is likely due to either AFM tip artifacts or real island-shaped residues. Whether they are artifacts or real islands can be verified by measuring the same scan area after rotating the samples. It can also be simply verified from line scan of the areas whether

the islands have a distinct height, and also from phase scan information. From our measurement, the height of the island showed ~1nm and phase information showed that it is a different material from the background material. As a result, we believe the islands observed are real residues. Image below shows some residues which are in color white, and these areas will be more easily found in grain boundaries. The measured height of the white islands in the image were ~1nm.



AFM image (500nmX500nm) with MoO3 residues on the flakes (white dots)

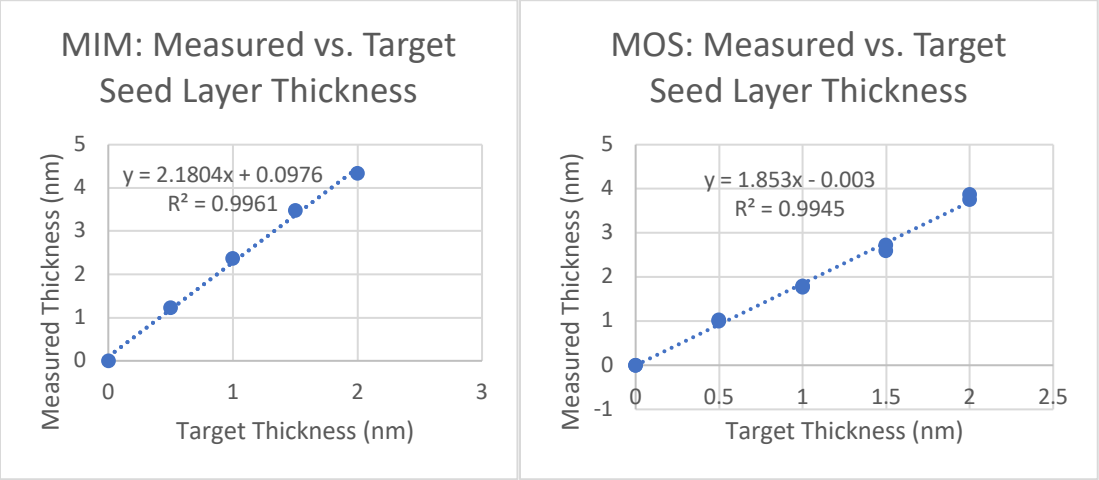
3. SOP

Seeded MOSCAPs and MIM structures on Si substrates: Process and Measurement

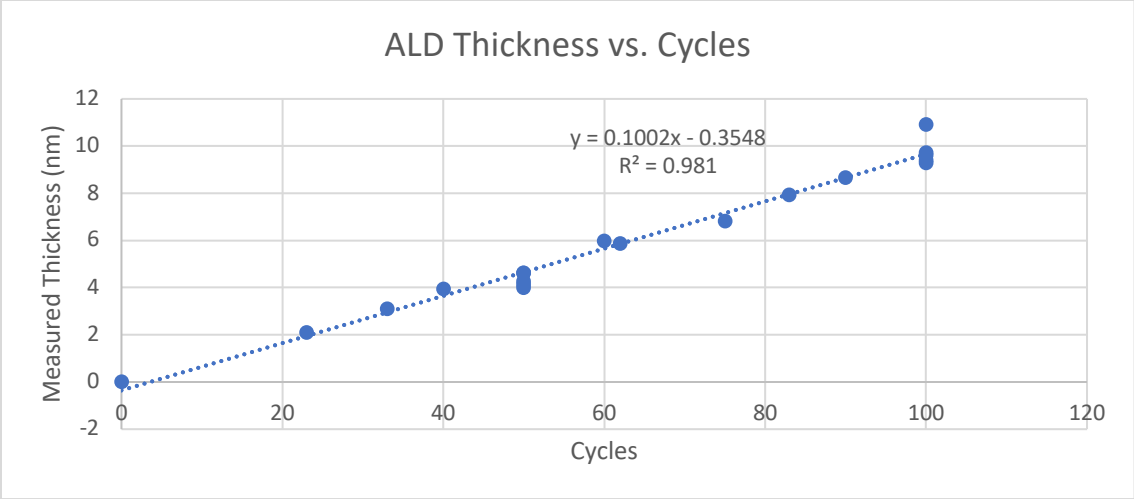
1. Obtain substrate and determine whether final structure will be MOSCAP or pseudo-MIM
    a. The substrate doping and wafer resistivity have a large impact on the electrical characteristics of the final product. The substrate doping will affect whether a p-MOSCAP, n-MOSCAP, or pseudo-MIM structure is formed.
    b. Using a lightly p-type doped substrate will result in a p-MOSCAP being formed, using a lightly n-type doped substrate will result in an n-MOSCAP being formed, and using a heavily-doped substrate will result in a near-metallic low-resistance bottom contact for the MIM structures that will be developed.
    c. In this report, we will show results for p-MOSCAPs (i-test) and highly n-doped pseudo-MIM structures.
2. Perform a standard RCA clean of the wafer
3. (Optional) Cleave the wafer to process different pieces with separate seed layer/ALD thicknesses
4. Measure native oxide thickness with Woollam
    a. This will allow us to later subtract out the native oxide thickness when doing ellipsometry measurements on the seed/ALD layers.
    b. Use the default Woollam measurement settings given on the Woollam wiki page.
    c. In VASE, use Si 1mm, NTVE_OX (fit, guessing 15A).
    d. Ensure that the MSE < 5 and the NTVE_OX fit returns between 5A and 25A.
    e. If the thickness is way off, there may be a thin film already deposited on your substrate.
    f. If the fit is not great, try fitting the n and k parameters, and refitting.
5. Use AJA to deposit seed layer
    a. Blow the surface of the samples with N_2 gun which is at the side of AJA to remove dust.
    b. Load the wafer/pieces into AJA using the correct sample holder.
    c. For alumina, use the Al_0.2A/s recipe which is in the AJA recipe list to deposit the desired seed layer thickness.
        i. Change the target thickness
        ii. This recipe is developed for thin Al film deposition, so for thin seed layer deposition, use this recipe.
    d. Remove the wafer/pieces from the system. With Al deposition, the seed layer should immediately oxidize in the ambient atmosphere (up to 2nm should fully oxidize within an hour based on published results[1] and lab member's findings).
6. Measure seed layer thickness with Woollam
    a. Use Si, NTVE_OX (with the previously measured thickness), use dielectr/Alumina (fit, guess seed layer thickness)
    b. As described in step 4, we can tune dielectr/Alumina layer fit by fitting n and k if necessary.

[1] https://www.spiedigitallibrary.org/conference-proceedings-of-spie/11116/111160O/Using-ellipsometry-and-x-ray-photoelectron-spectroscopy-for-real-time/10.1117/12.2529893.short

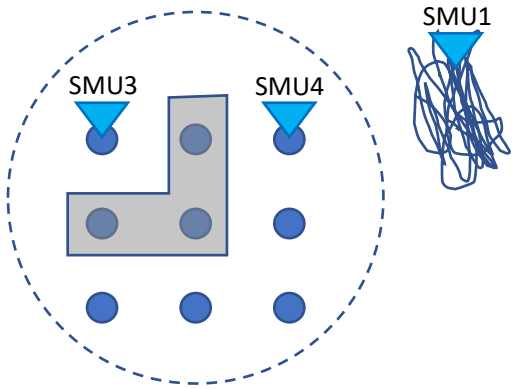
c. Seed layer oxidation is expected to produce larger thicknesses than the seed layer that was deposited. We believe this is due to a combination of oxidative expansion and a poorer oxide quality (lower density).
d. The plot for the ellipsometry measurements of alumina thickness vs. seed layer thickness is given below for the heavily n-doped pseudo-MIM and the p-doped MOSCAP:



7. Use Fiji1/2 to deposit oxide film
    a. Alumina with standard thermal alumina recipe (~1A/cyc)
        i. Thermal Al2O3 STANDARD @ 200C default
    b. Depending on whether you need fine-grained control over your total oxide thickness, you may either:
        i. Subtract your measured seed layer thickness from your total desired oxide thickness to determine the number of cycles to run. We used this approach for our MOSCAPs.
        ii. Ignore the seed layer and run ALD for the desired number of cycles. This is useful for running multiple samples at once when testing multiple seed layer thicknesses. We used this approach for our MIM structures.
8. Measure final oxide thickness with Woollam
    a. Use Si, NTVE_OX (with the previously measured thickness), dielectr/Alumina (fit, guess measured seed layer thickness + expected ALD thickness)
    b. Tune n,k if needed
    c. ALD thickness fit is given below:



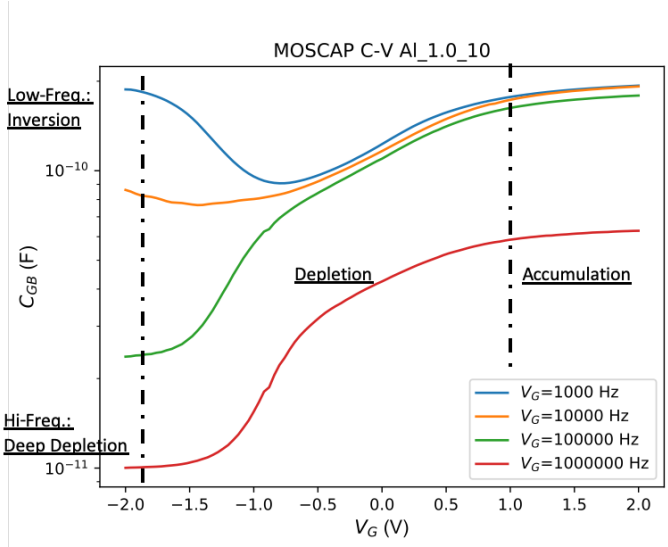
9. Obtain shadow mask and prepare samples for patterned deposition
    a. Obtain a shadow mask that contains holes for defining the top contacts of the MIM structures you wish to measure. We used a shadow mask with 200-micron diameter holes. It is possible to put multiple samples under the shadow mask if the samples are small enough and the mask is large enough.
    b. Run Ti 0.5A/s recipe for a final thickness of 5 nm. This layer is for adhesion since Au is not very hard or good at sticking to other materials.
        i. Ti_0.5A/s recipe
    c. Run Au 1A/s recipe for a final thickness of 20 nm.
        i. Au_1A/s recipe
10. Fabrication complete! Now begin measurements with micromanipulator6000.
11. Open micromanipulator6000 and load the akashl_E241 workspace.
12. Scratch surface of sample
    a. The scratches dig under the oxide layer and enable one of your probes to contact the substrate directly.
    b. Scratch oriented away from your contacts to minimize dust getting on contacts.
13. Contact SMU1 probe to scratched area
14. Identify a 3x3 grid of contacts that have no dust



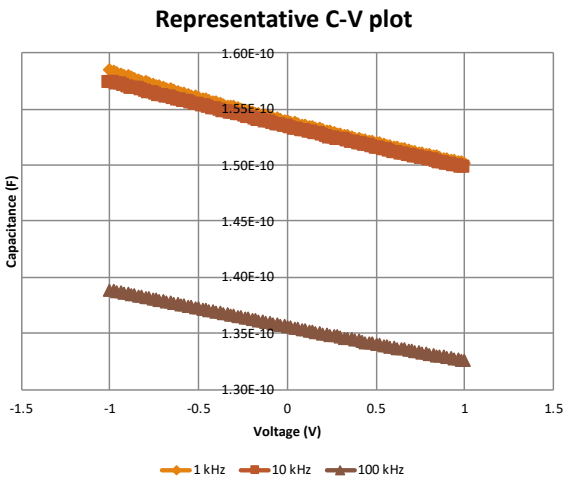
15. Contact SMU3 probe in top-left corner contact
16. Breakdown top-left corner structure

a. Use Backgate Breakdown test
    i. Bidirectional 0V – 50V sweep (101 steps each way) on SMU3
    ii. 50 mA compliance current
    iii. SMU1 grounded, SMU4 floated
b. Advantage: now backgate contact is physically closer to structures being tested
c. Less IR-drop through substrate (less wafer resistance when contacts are closer)
d. You should see a low current that jumps up very quickly to a high current beyond a certain threshold voltage. See the I-V curves below to understand what dielectric breakdown looks like.

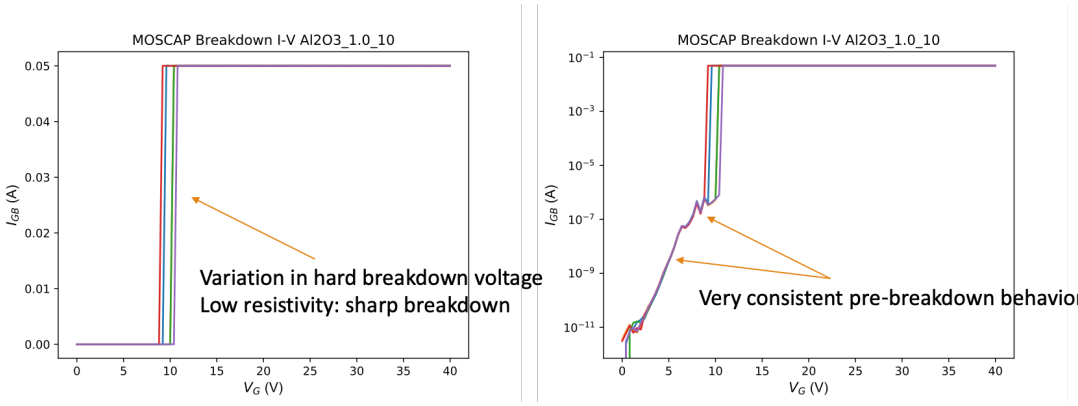
17. Contact SMU4 to 3 closest contacts for C-V
    a. See gray area in figure above
    b. Use C-V Sweep formula
        i. Bidirectional -1V – 1V sweep (101 steps each way), measuring Rs-Cs b/w SMU3 and SMU4, no delay, 50 mA AC signal
        ii. 1kHz, 10kHz, 100kHz, 1MHz, 5MHz measured C-V frequencies
        iii. SMU1 floated
    c. For MOSCAP, you should see MOS behavior
        i. At low frequency, you should see inversion, depletion, and accumulation regions
        ii. At high frequency, you should see deep depletion, depletion, and accumulation regions
        iii. An example is given below



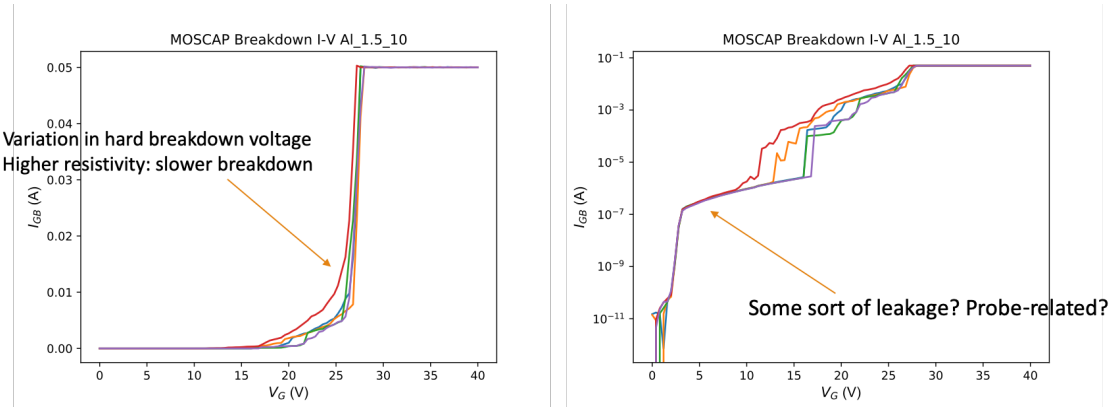
d. For MIM structures, you should see nearly constant capacitance as shown below



18. Contact SMU4 to 5 remaining outer contacts for breakdown measurements (I-V)
    a. Use Breakdown formula
        i. Unidirectional 0V – 50V sweep (101 steps) on SMU4
        ii. 50 mA compliance current
        iii. SMU1/SMU4 grounded
    b. For MIM structures, you should see sharp breakdown behavior where the current is near zero and shoots up to the compliance current at some threshold voltage

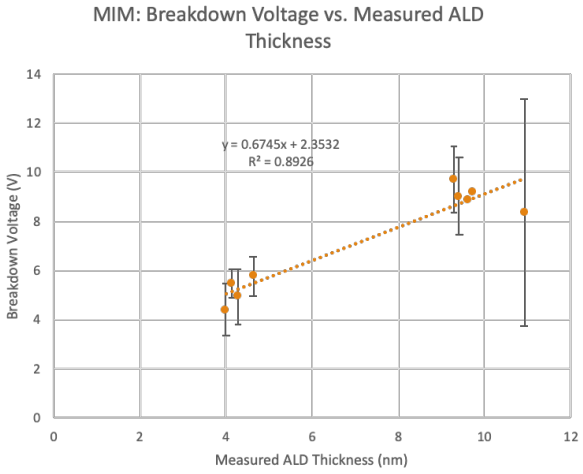


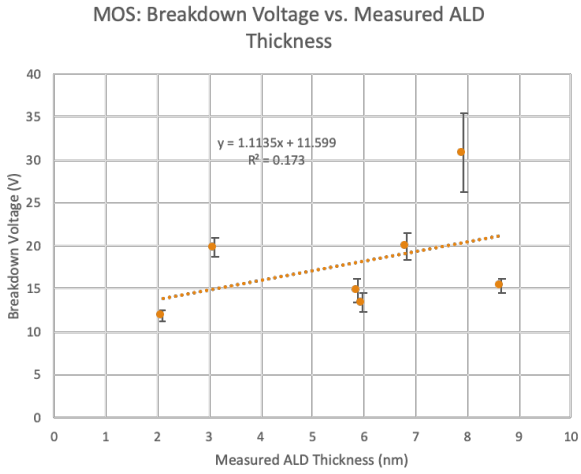
    c. For MOS structures, you may see less sharp breakdown behavior depending on the resistivity of the substrate and the exact doping profile



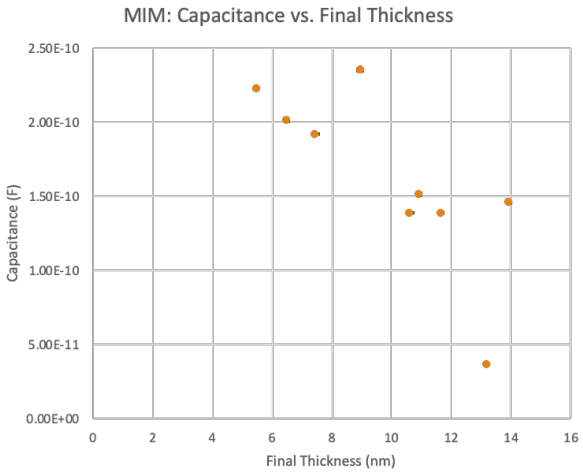
d. In either case, you can expect to see variation in the breakdown threshold voltage due to intrinsic variations in the breakdown behavior device-to-device

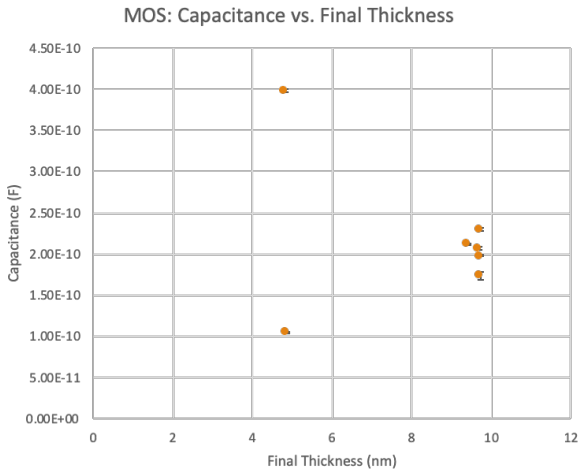
19. Compute desired values



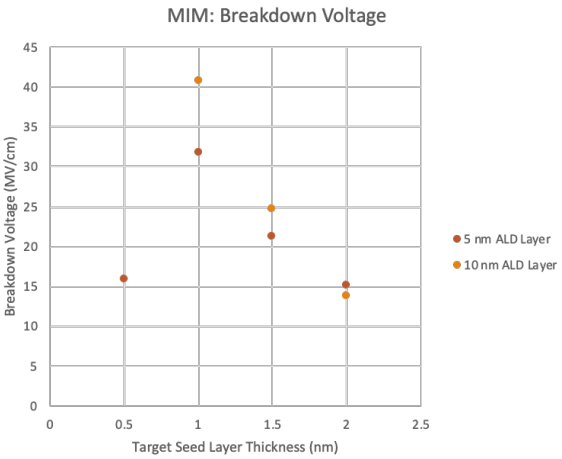


Breakdown voltage is defined as 1st intersection of I-V curve with 1mA current threshold

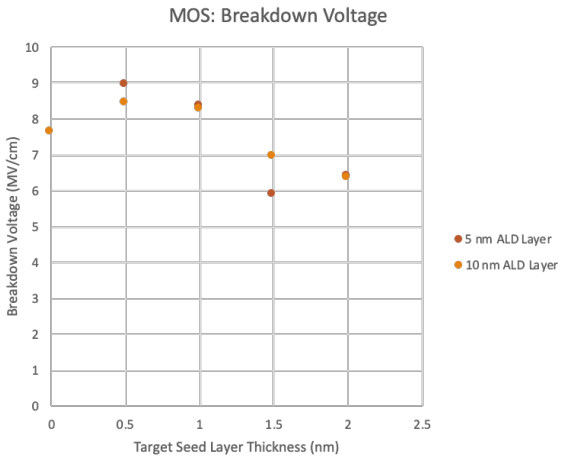




Capacitance is extracted from low-frequency (1kHz) C-V curve @ 1V



Note: # of ALD cycles was NOT dependent on seed thickness here



Note: # of ALD cycles WAS dependent on seed thickness here