Low-T, High-κ Dielectrics for Transparent/ Flexible 2D Electronics

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EE 412 – Advanced Nanofabrication Laboratory

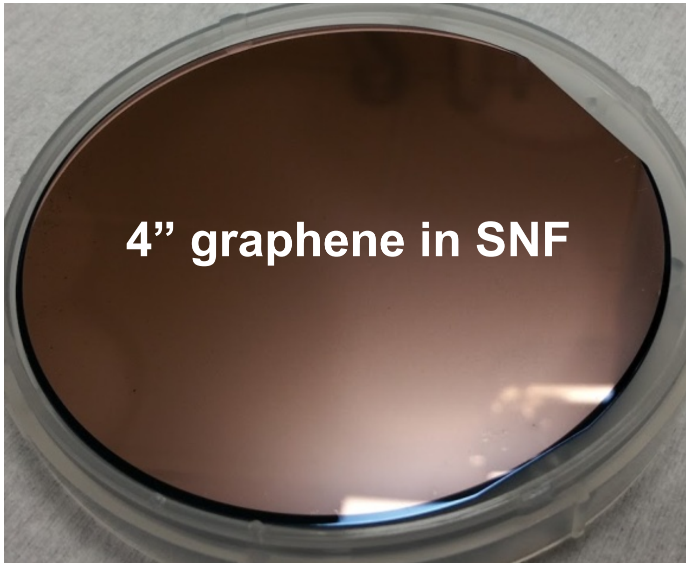
25 slides

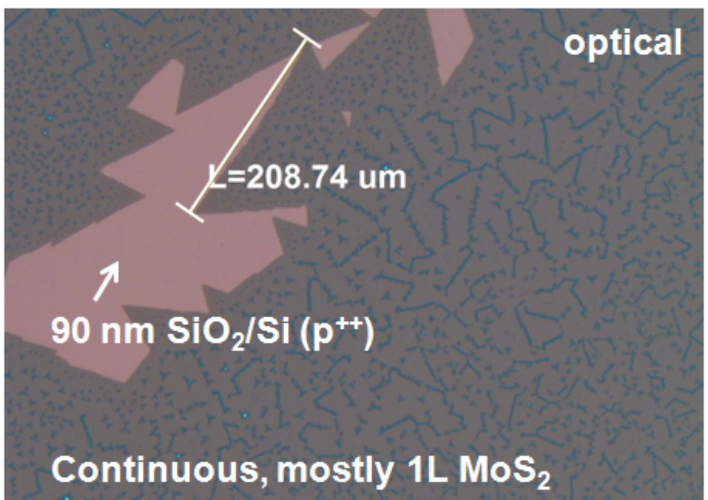
Outline

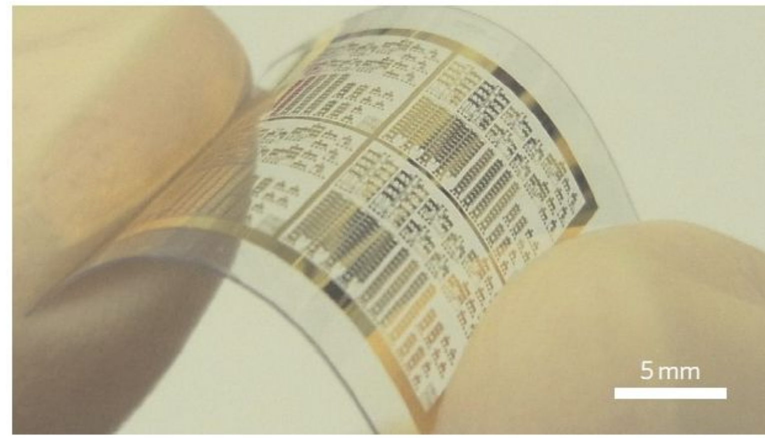
- **Introduction and Motivation**
- **Methodology**
- **Benchmark ALD Oxides**
- **Processing on PDMS**
- **Processing on PEN**
- **Conclusions and Future Work**

1L G/1L MoS_2/PDMS/Batman

Motivation – Transparent/Flexible 2D Oxides



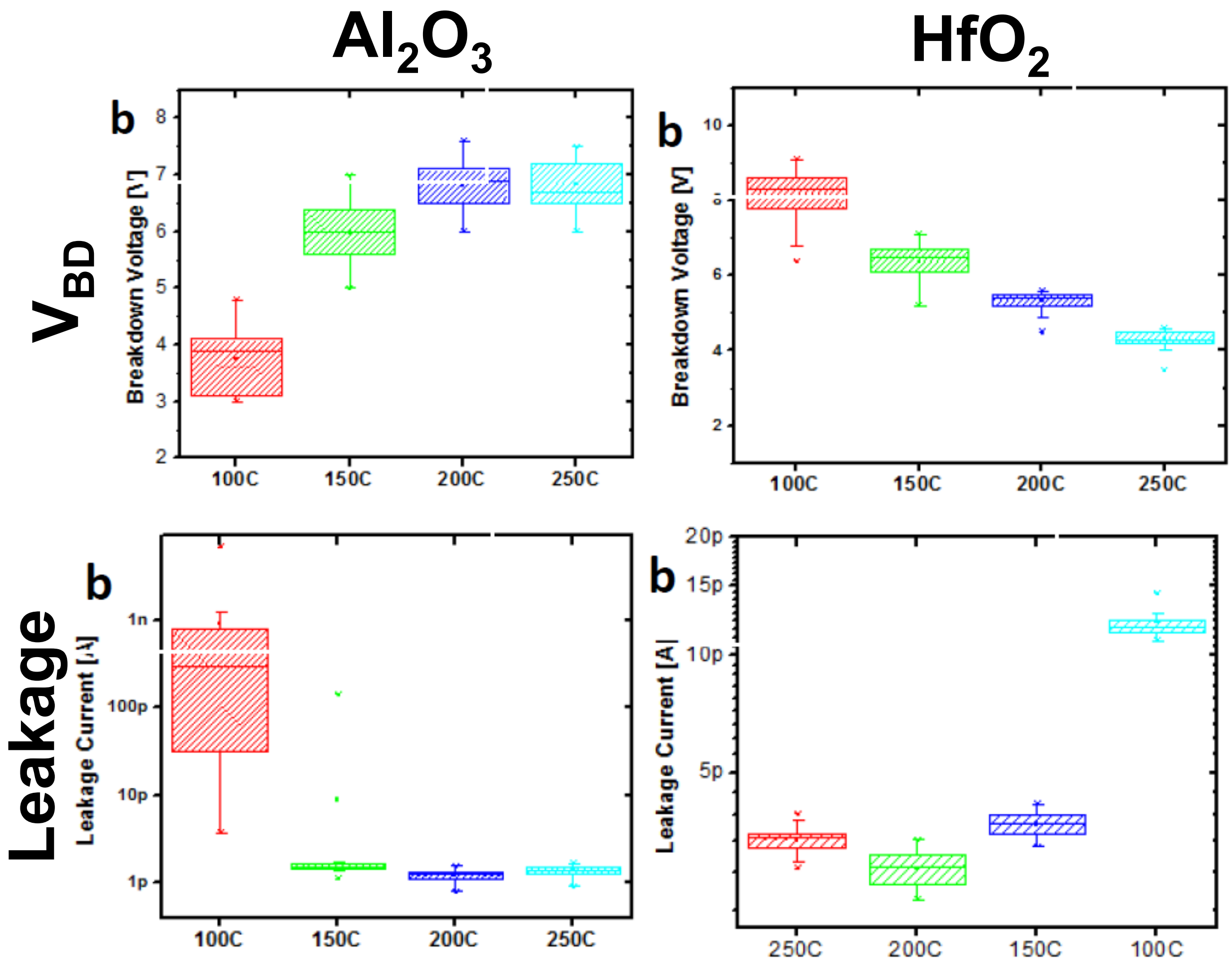




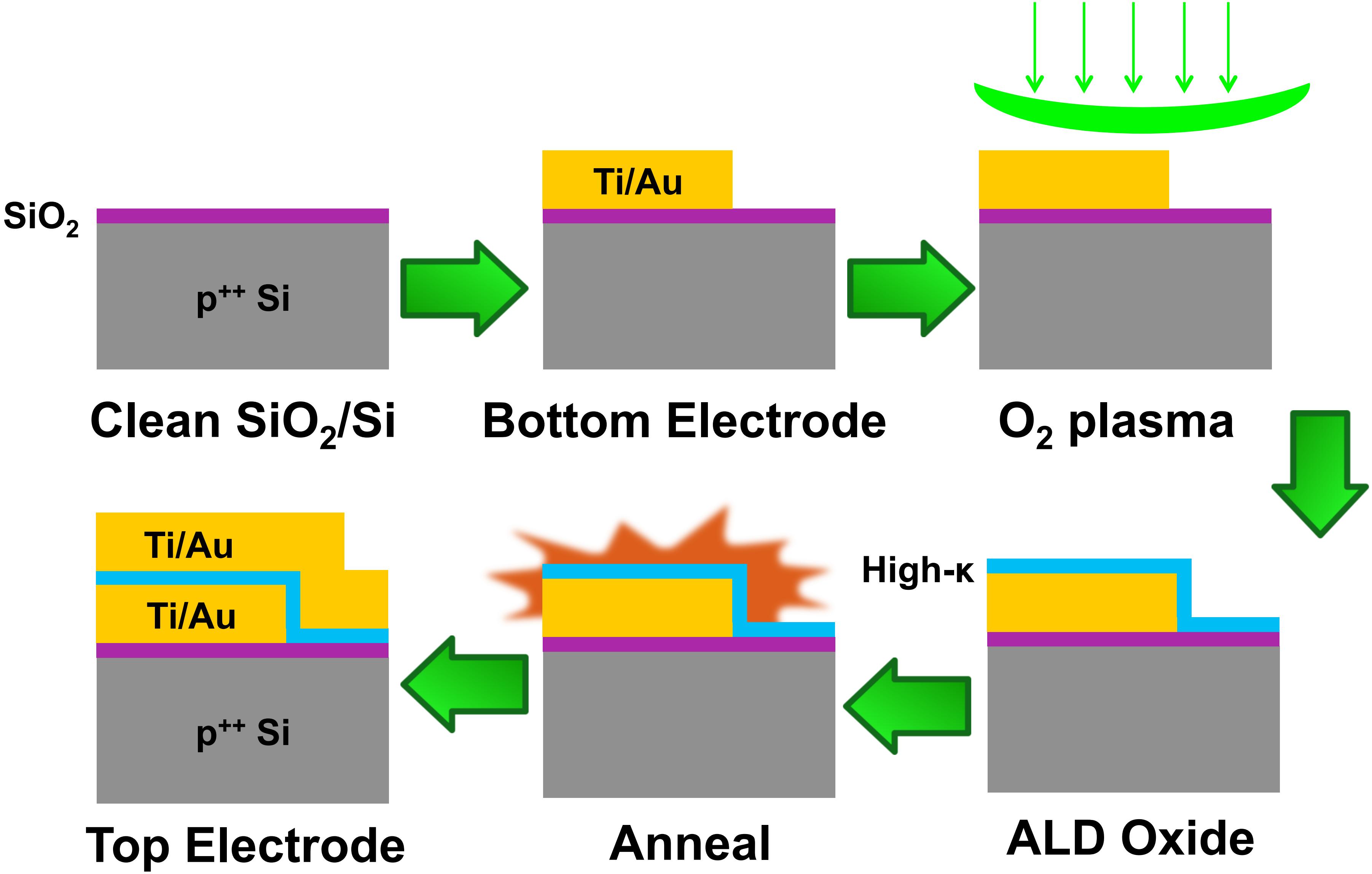
- **NEED: Low-T, high-κ, flexible-compatible, thin film oxides**

Motivation – Transparent/Flexible 2D Oxides

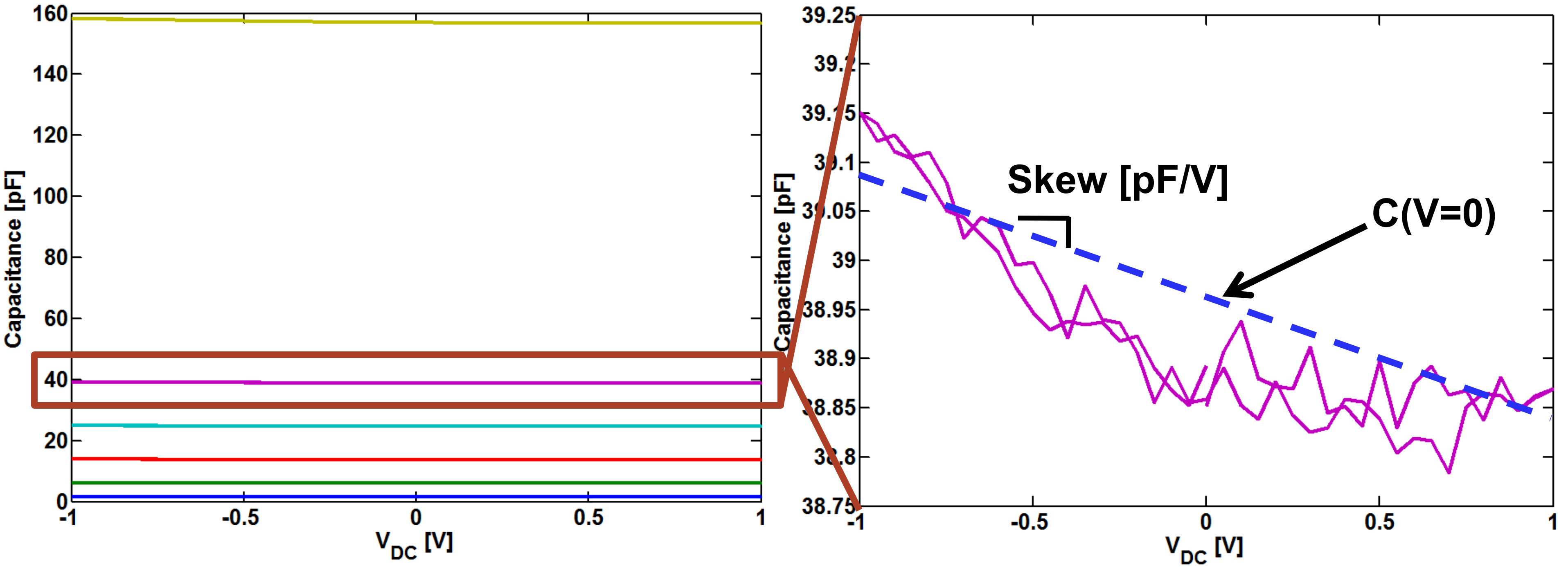
- Y. Wu, S. Yu, and S. Li with J. Provine (EE 412, Fall 2010)



Methodology – Process Flow

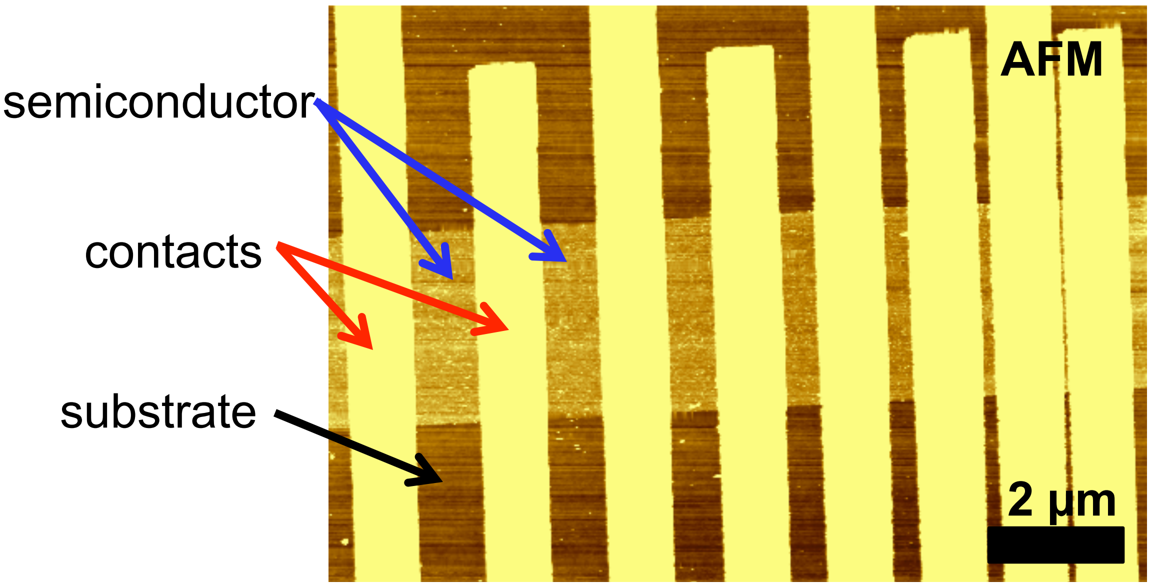


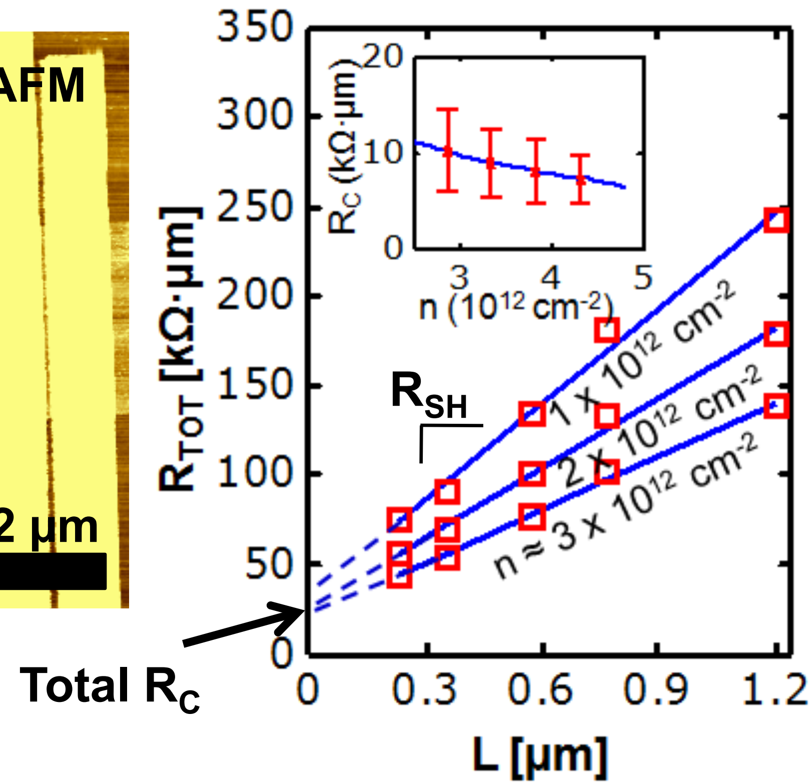
Methodology – Measurements



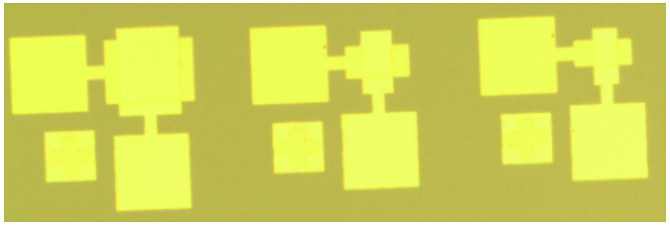
- All caps were measured from 0 → 1 → -1 → 0 V.
- Capacitances changed by <1% over this range.
- A line was fit to the data, with the slope being the “skew” and the C-V intercept value taken for fitting C/A.

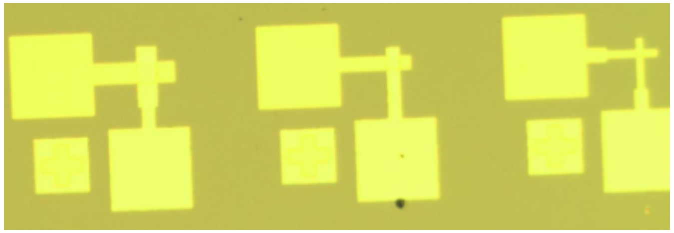
Methodology – Capacitor “TLM” Arrays





We can do the same thing with capacitors!





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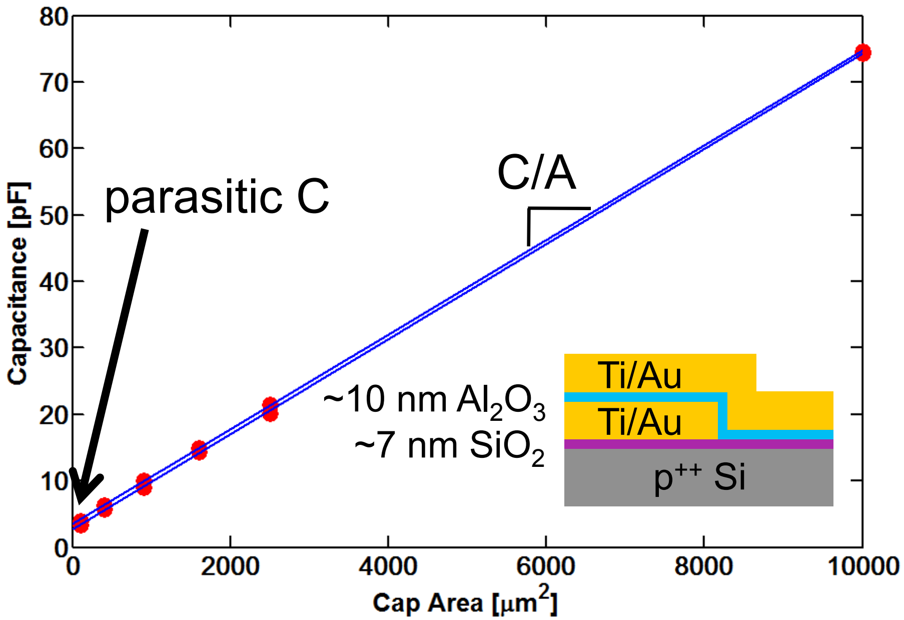
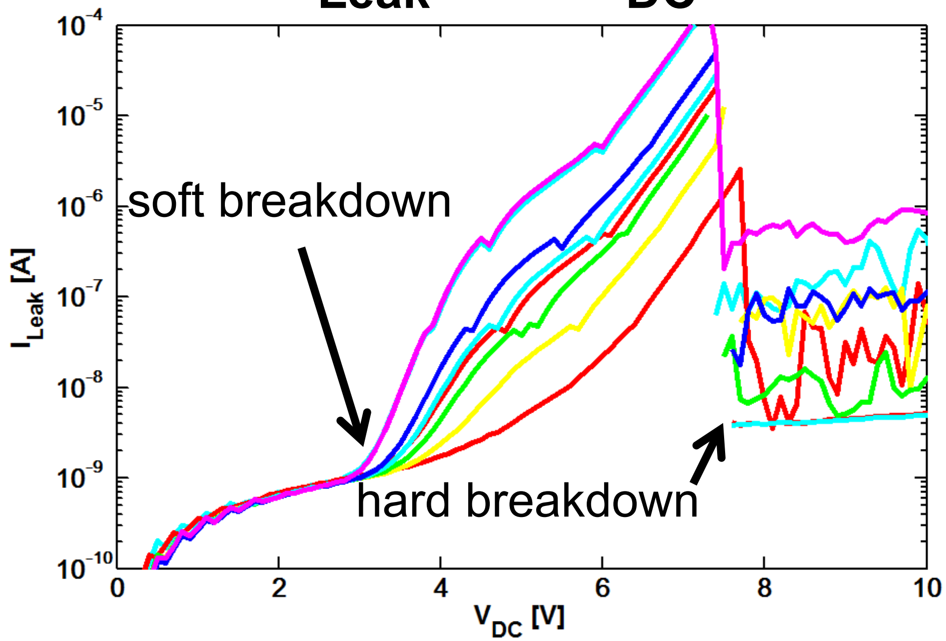
Savannah - 150 °C Alumina + 200 °C FGA

C vs. A



I_{Leak} vs. V_{DC}

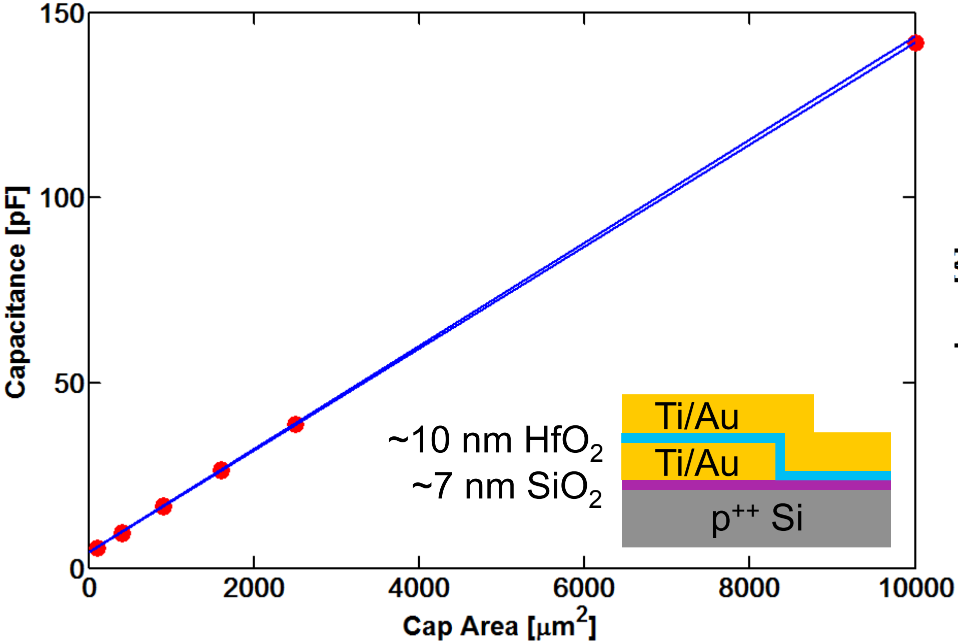


- $C = 0.716 \pm 0.009$
- 0.713 ± 0.006 μF/cm²
- $R^2 = 1.000, 1.000$
- d = 9.4 nm
- $\kappa = 7.60 \pm 0.10, 7.56 \pm 0.06$

- I_{Leak} < nA
- $V_{BD,soft}$ ~ 3.0 V
- $E_{crit,soft}$ ~ 0.32 V/nm
- $V_{BD,hard}$ > 7.0 V
- $E_{crit,hard}$ ~ 0.74 V/nm

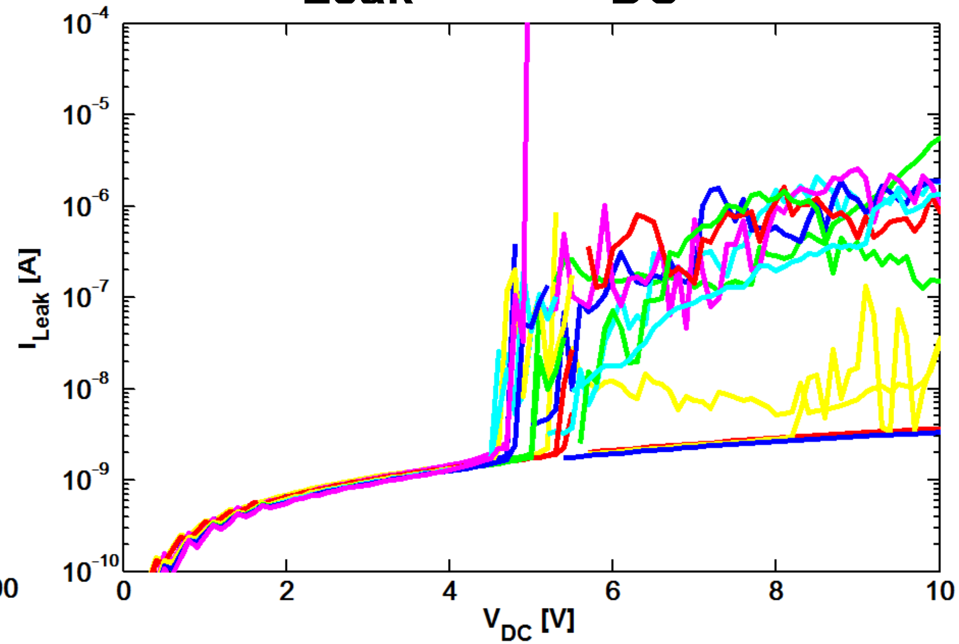
Savannah - 150 °C Hafnia + 200 °C FGA

C vs. A



- C = 1.39 ± 0.02
- 1.38 ± 0.01 μF/cm²
- R^2 = 1.000, 1.000
- d = 10.5 nm
- κ = 16.5 ± 0.3, 16.3 ± 0.1

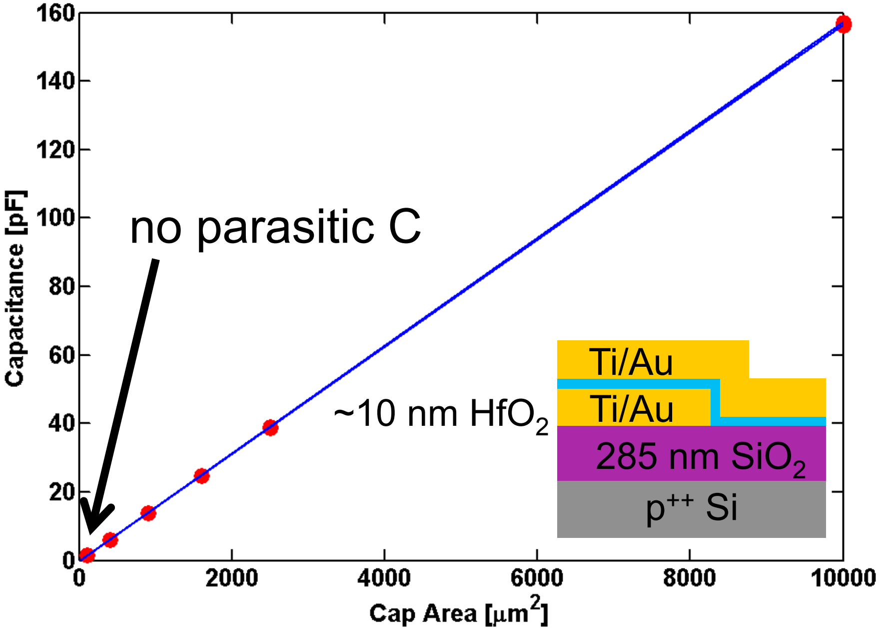
I_{Leak} vs. V_{DC}



- I_{Leak} < nA
- V_{BD} > 4.5 V
- E_{crit} ~ 0.43 V/nm

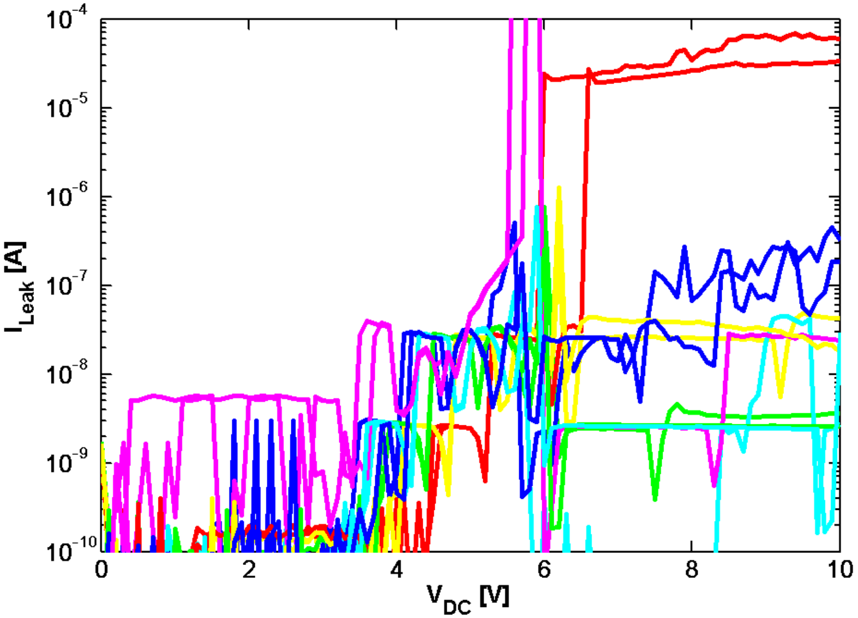
MVD - 125 °C Hafnia + 125 °C FGA

C vs. A



- $C = 1.57(4) \pm 0.004$
- $1.56(6) \pm 0.004$ μF/cm^2
- $R^2 = 1.000, 1.000$
- $d \approx 11.2$ nm
- $\kappa \approx 15.9 \pm 0.1, 15.8 \pm 0.1$

I_{Leak} vs. V_{DC}



- I_{Leak} < nA
- $V_{BD} > 5.5$ V
- $E_{crit} \sim 0.49$ V/nm

Results – Benchmark ALD Oxides on SiO_2

Savannah	Alumina				Hafnia			
ALD temp	200 °C	200 °C	150 °C	100 °C	200 °C	200 °C	150 °C	100 °C
anneal	+ 50 °C O_2	+ 50 °C FGA			+ 50 °C O_2	+ 50 °C FGA		
d [nm]	10.0	10.0	9.4	8.4	8.7	8.7	10.5	11.9
Skew [pF/V]	~-0.15	~-0.01	~-0.15	X	~-0.2	~-0.2	~-0.1	~-0.15
C [μF/cm^2]	0.670	0.690	0.715	X	1.51	1.61	1.39	1.15
κ	7.6	7.8	7.6	X	14.8	15.8	16.4	15.5
I_{Leak}	<nA	<nA	<nA	X	<nA	<nA	<nA	<nA
V_{BD} [V]	>3.5	>3.5	>3.0	X	>3.2	>3.2	>4.5	>6.0
E_{crit} [V/nm]	0.35	0.35	0.32	X	0.37	0.37	0.43	0.50

MVD	Alumina		Hafnia	
ALD temp	125 °C	100 °C	125 °C	100 °C
FGA	125 °C	100 °C	125 °C	100 °C
d [nm]	~8.9*	6.9	~11.2*	11.3
Skew [pF/V]	~-0.05	X	~-0.7	~-0.4
C [μF/cm^2]	0.760	X	1.57	1.32
κ	~7.7*	X	~16*	13.2
I_{Leak}	<nA	X	<nA	<nA
V_{BD} [V]	>3.0	X	>5.5	>5.5
E_{crit} [V/nm]	~0.34	X	~0.49	0.49

*d interpolated from Savannah data

- Savannah and MVD oxides are quite similar.
- Al_2O_3 and HfO_2 show opposite trends in thickness, capacitance, and breakdown at lower temperatures.
- HfO_2 seems to be a considerably more stable process at low T.

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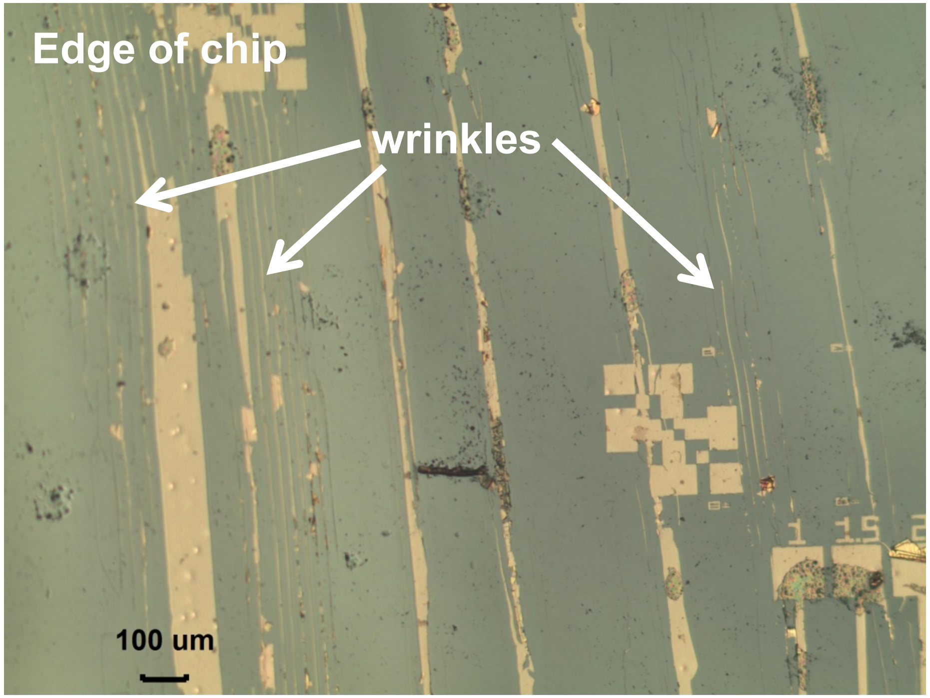
Overview – Processing on Flexibles

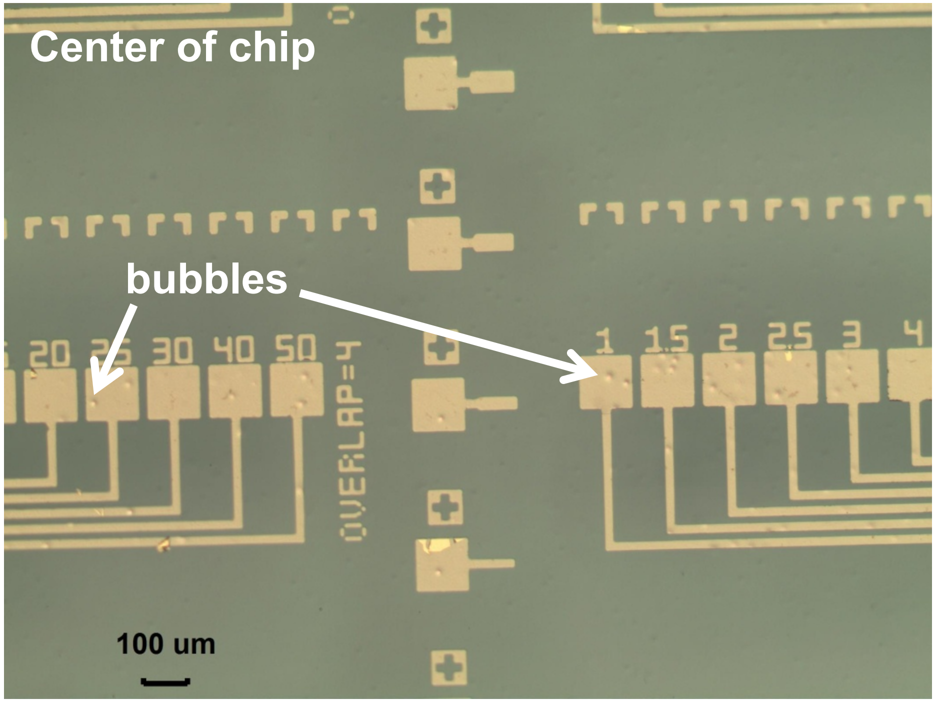
	Hotplate Curing	Ovens ≥150 °C	Direct SPR 3612	Oxide/Metal Cracking	Thermal Wrinkling	Trivial Alignment
SiO_2/Si	yes ✓	yes ✓	yes ✓	no ✓	no ✓	yes ✓
PDMS	no ✗	no ✗	no ✗	yes ✗	yes ✗	yes ✓
PEN	yes ✓	no ✗	? ?	no ✓	no ✓	no ✗

- Spoiler: PEN is easier to work with as a substrate than PDMS

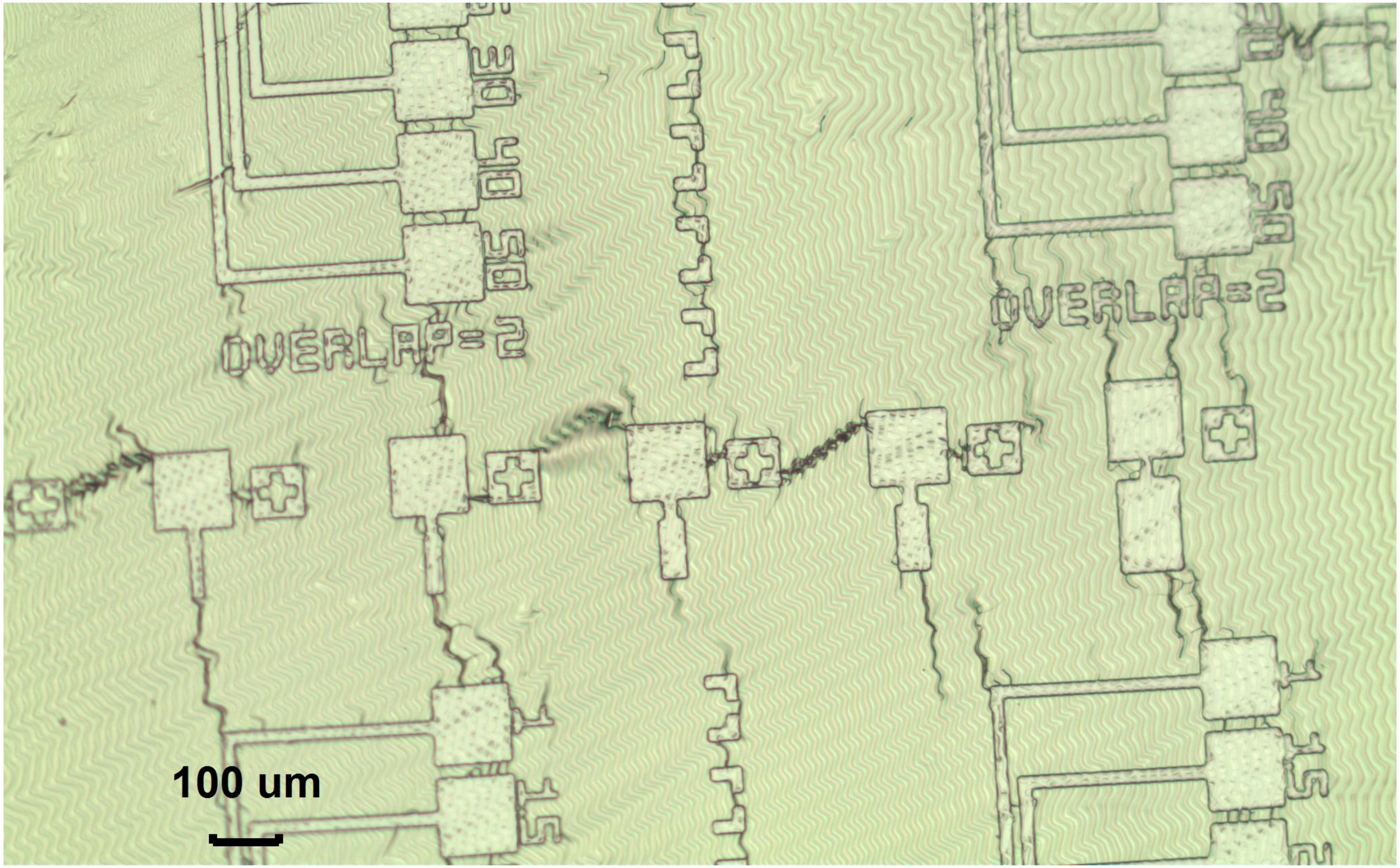
Initial Cap Pads on PDMS

- PDMS thoroughly outgassed for 2 hours in vacuum and baked at 80 °C for 2 hours in ambient oven.
- PMGI (liftoff layer) baked on at 200 °C for 5 minutes
- Strong temperature gradient caused visible wrinkles near edges
- SPR 3612 baked in 90 °C oven for 25 minutes
- ~1 cm^2 in center of 2×2 cm chip had bubbles but no wrinkles



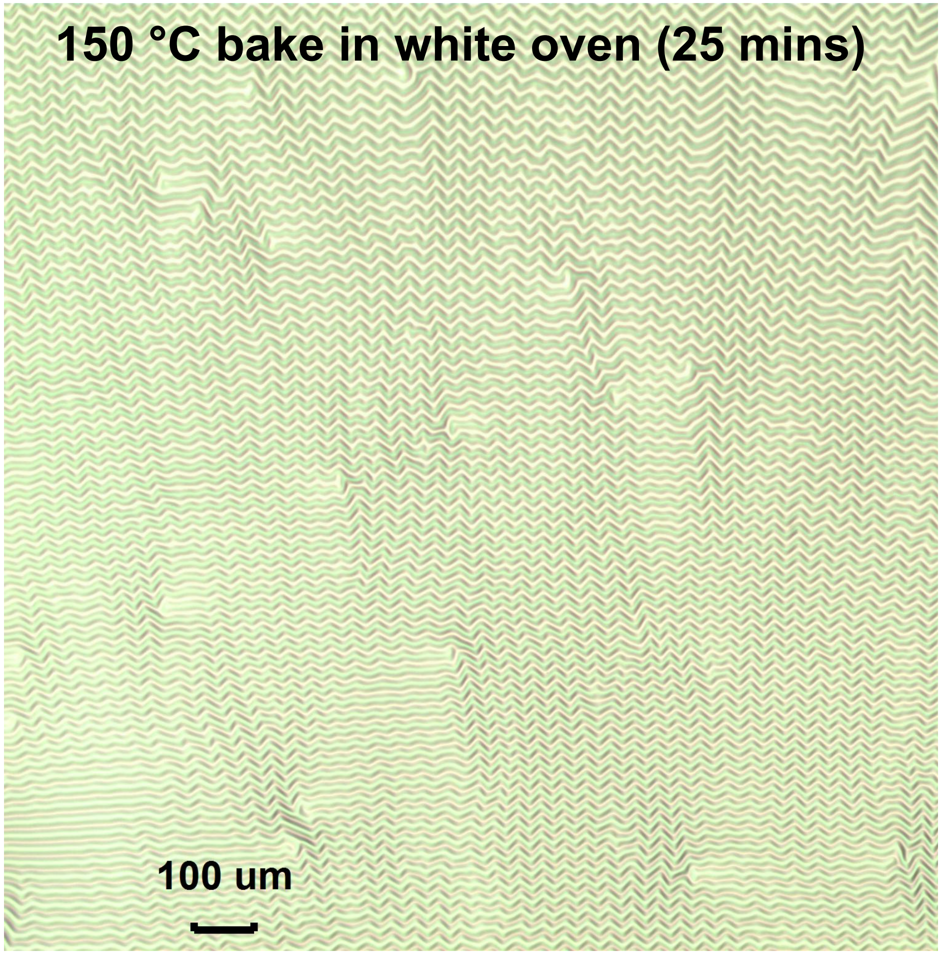


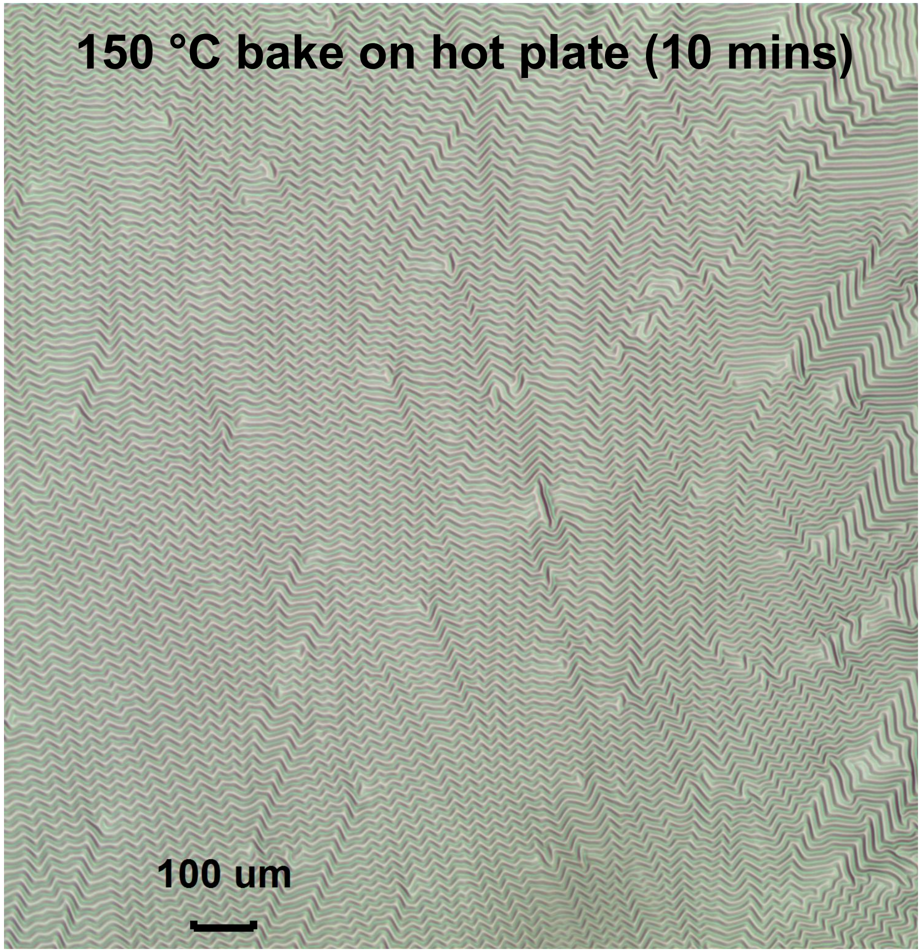
Cap Pads on PDMS – 2nd Try



- PMGI spun on at 3000 rpm
- 230 °C bake in white oven for 25 mins (+ SPR 3612 and develop)

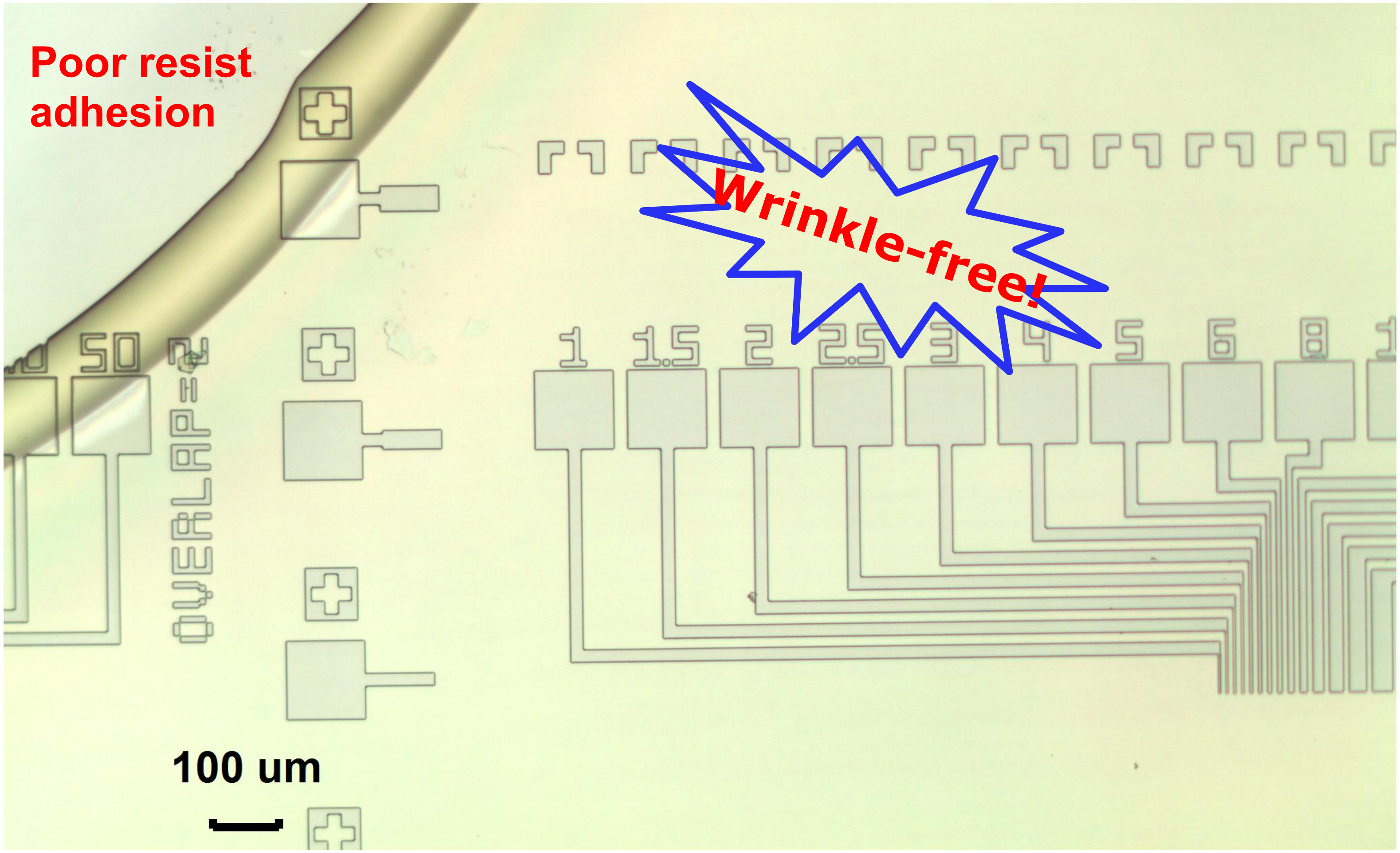
Cap Pads on PDMS – 3rd Try





- PMGI spun on at 3000 rpm
- 150 °C bake in white oven (25 mins) or on hot plate (10 mins)

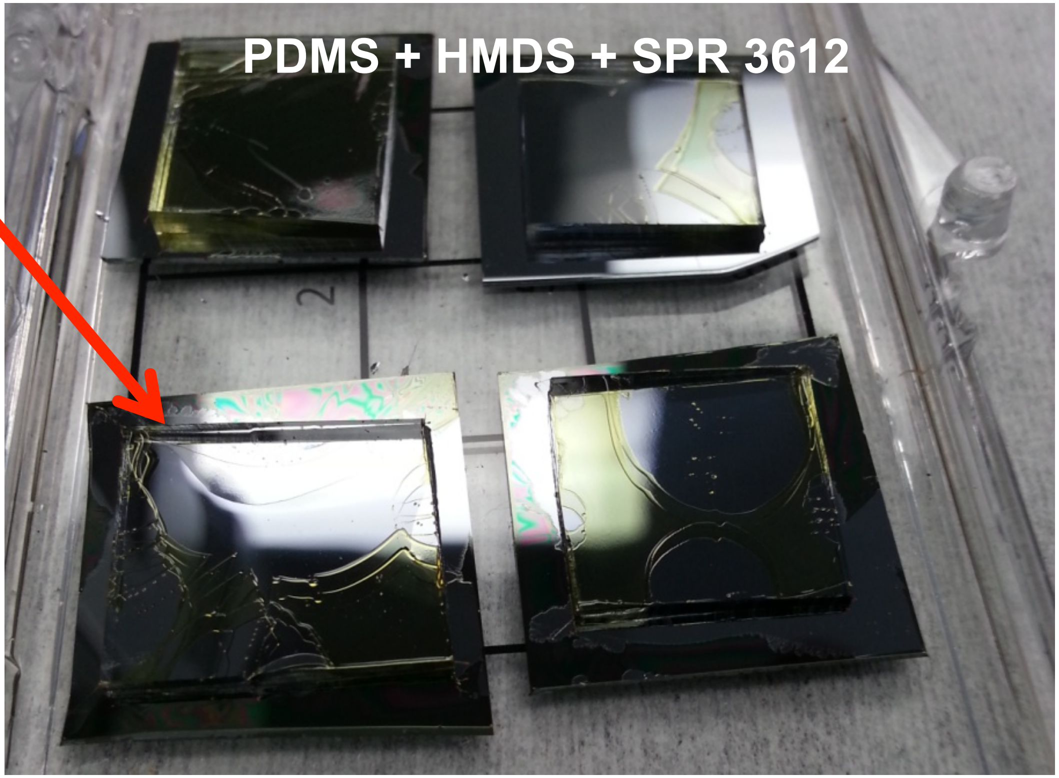
Cap Pads on PDMS – 4th Try



- No LOR – only SPR 3612 + 25 min bake in 90 °C oven
- Resist did not adhere well to PDMS – will need HMDS treatment

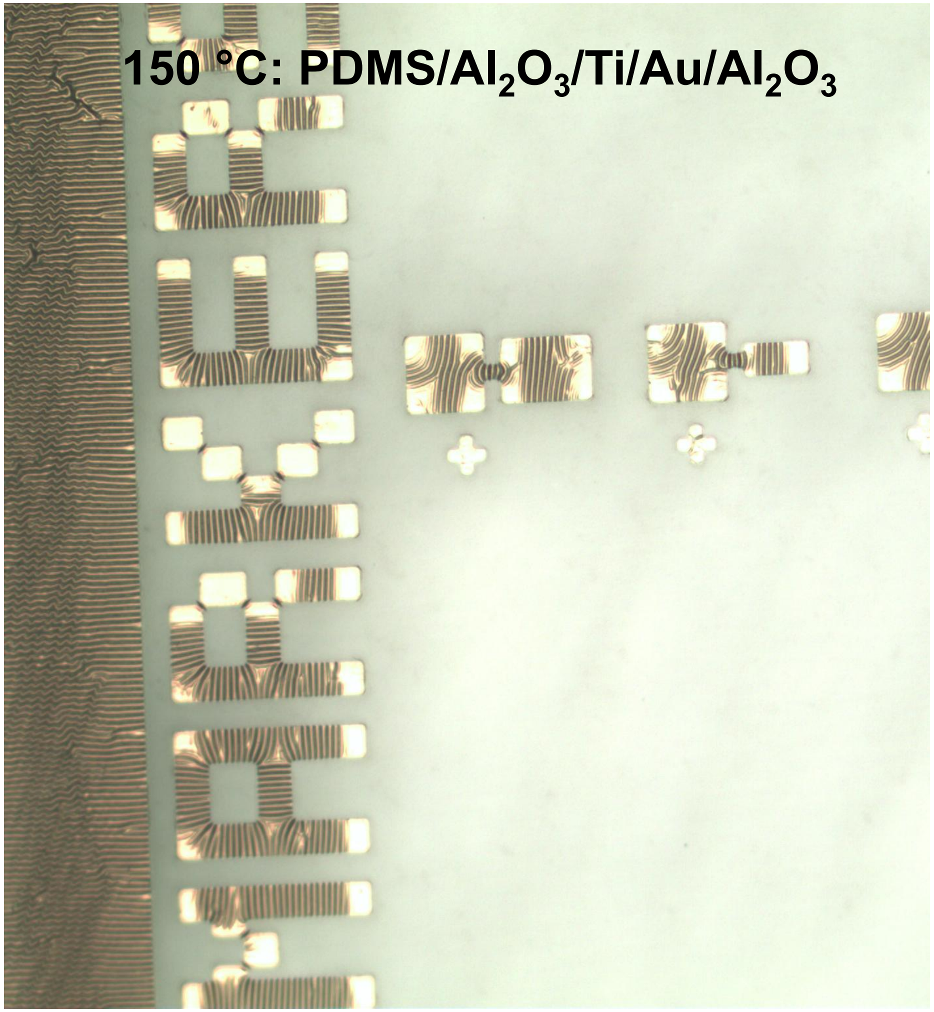
Photoresist and PDMS

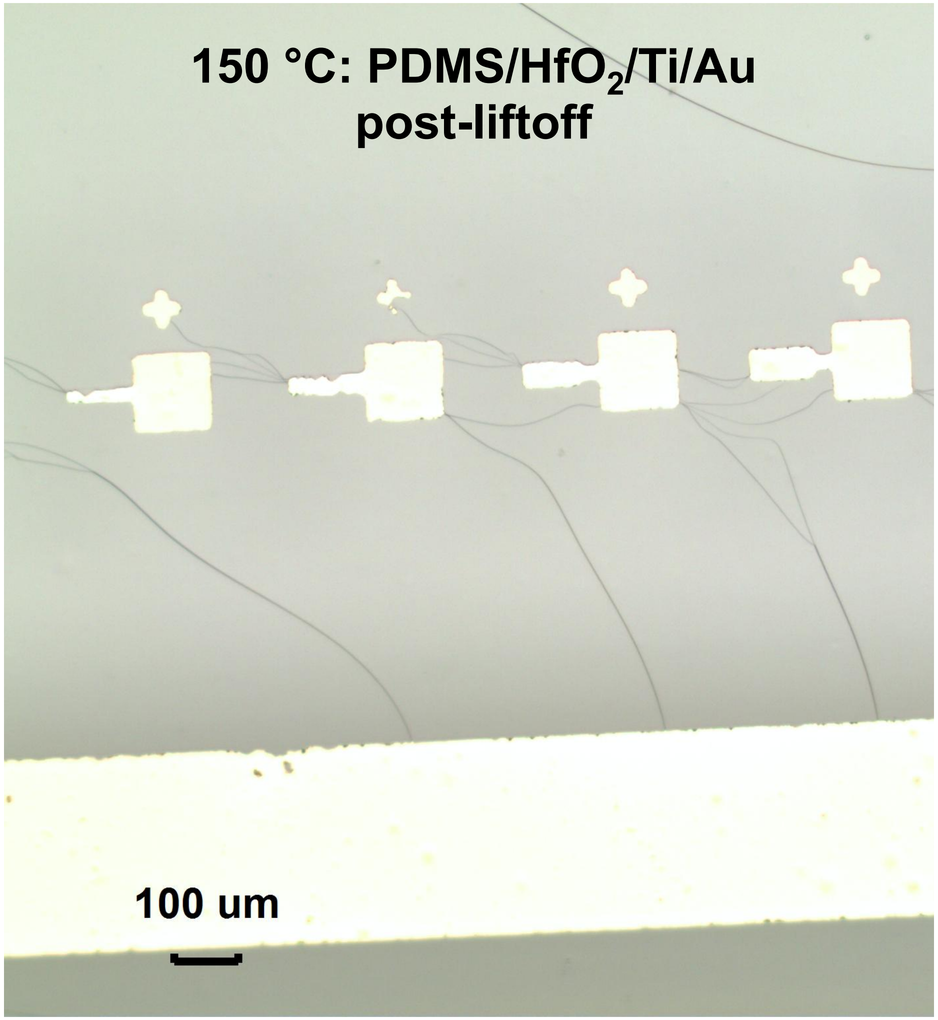
- HMDS does not help with resist adhesion to PDMS.
- Deposited 100 cycles of ALD oxides prior to lithography.
- SPR 3612 much easier to spin on (without HMDS) to PDMS/high-κ.



- Possible alternative: spin on LOR and bake in the White oven at 100 °C for at least 4 hours before continuing with SPR 3612 and lithography.

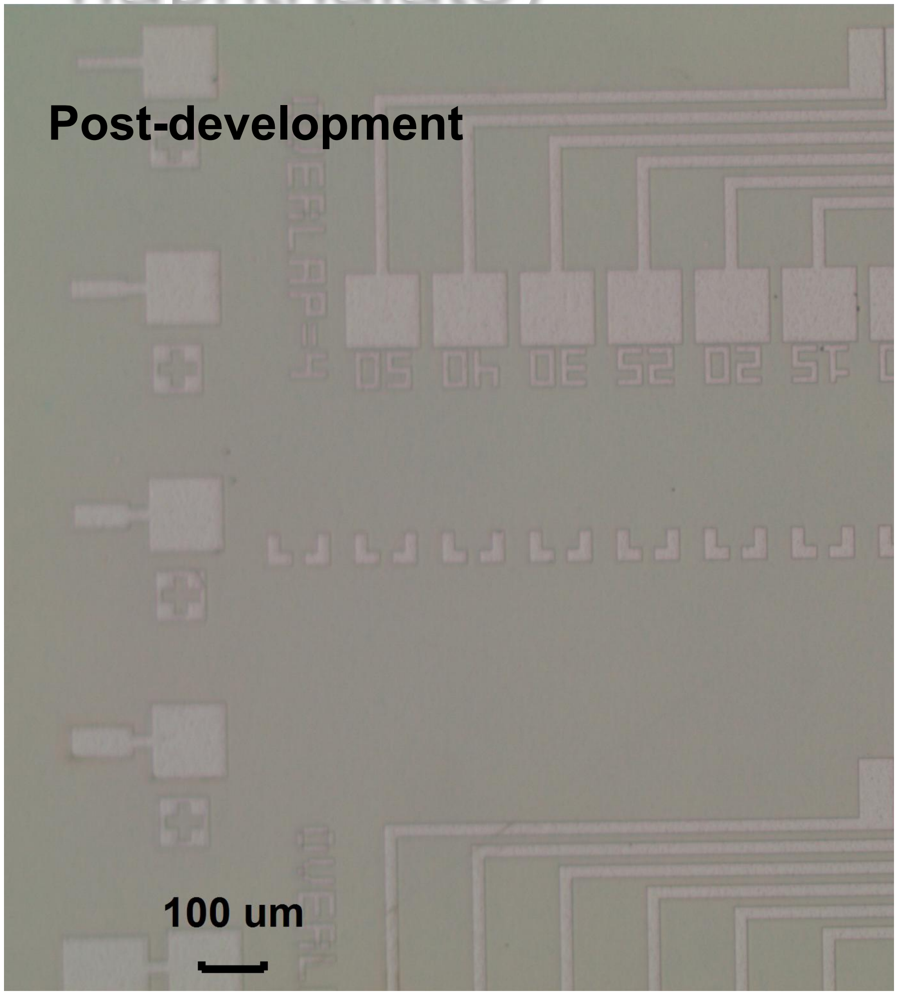
PDMS + High-κ Buffer Layer

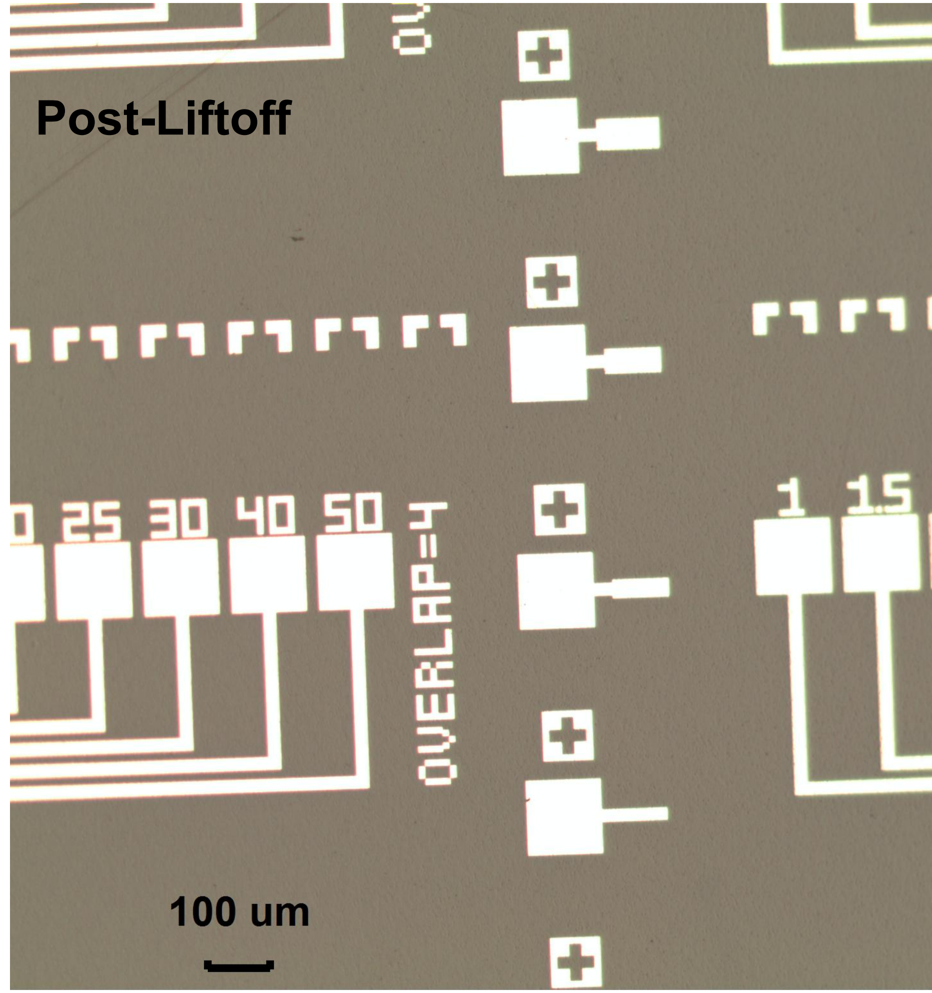




- Wrinkles visible on metal for 150 °C oxides.
- Also happens for 125 and 100 °C oxides.

Cap Pads on PEN (polyethylene naphthalate)

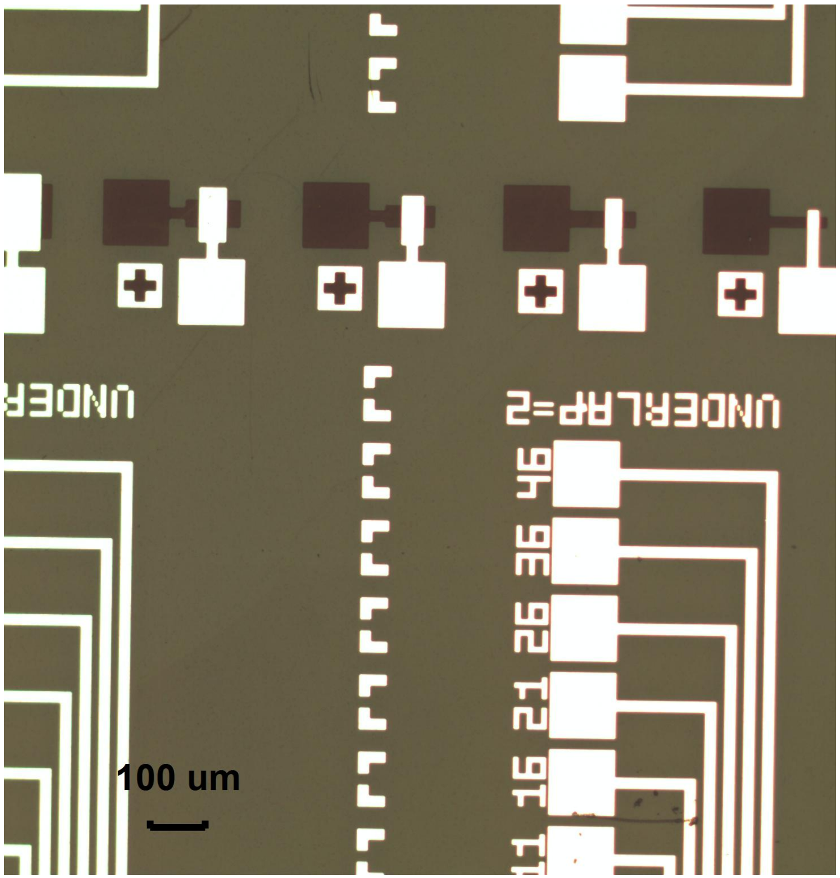




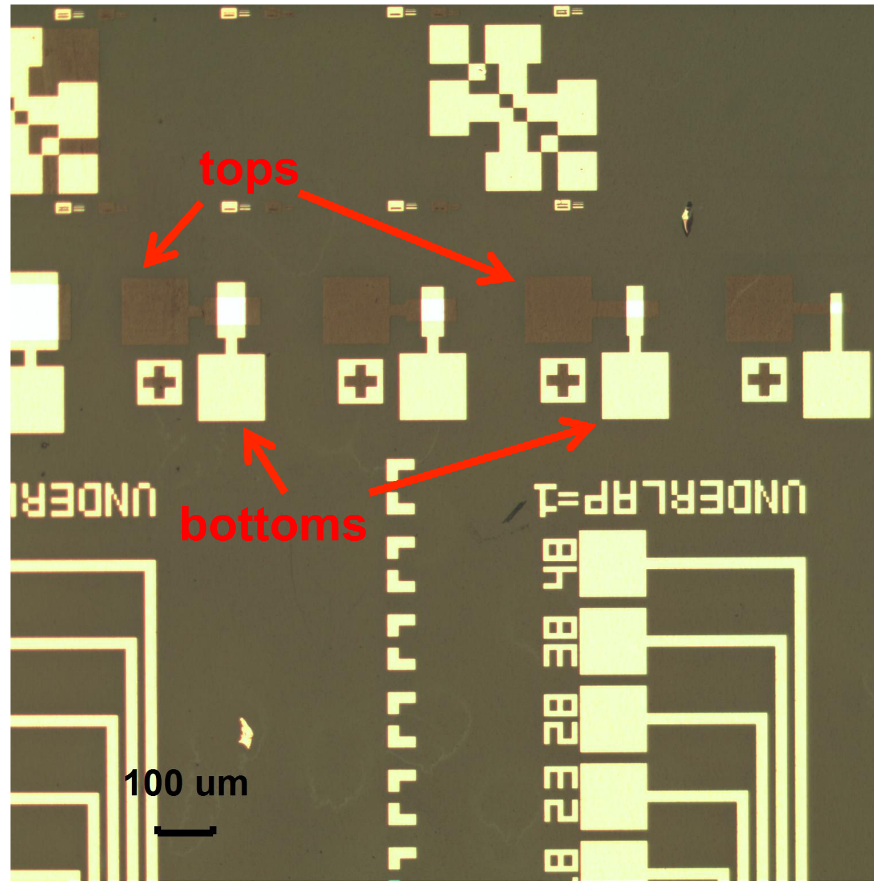
- PMGI spun on at 3000 rpm + 150 °C bake on hot plate (10 mins)
- SPR 3612 spun on at 5000 rpm + 90 °C bake on hot plate

Caps on PEN – 100 °C MVD Oxides

100 °C: PEN/Ti/Au/Al_2O_3/Ti/Au post-liftoff

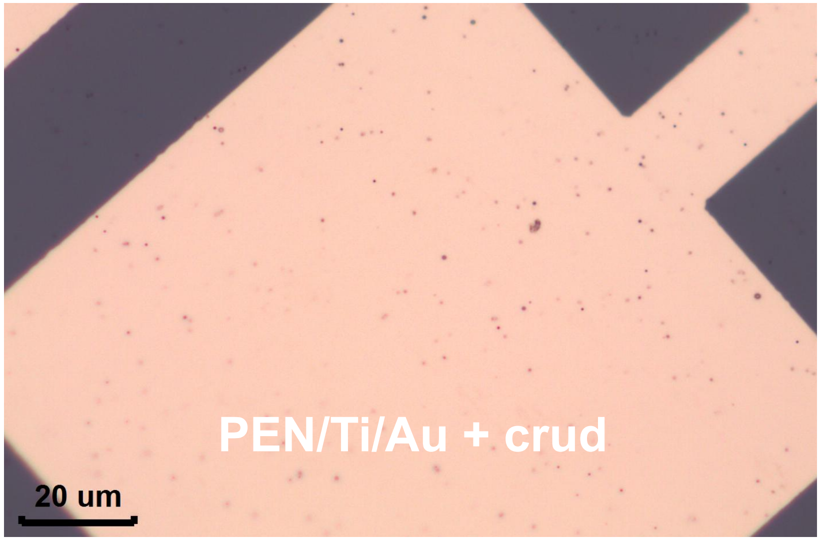


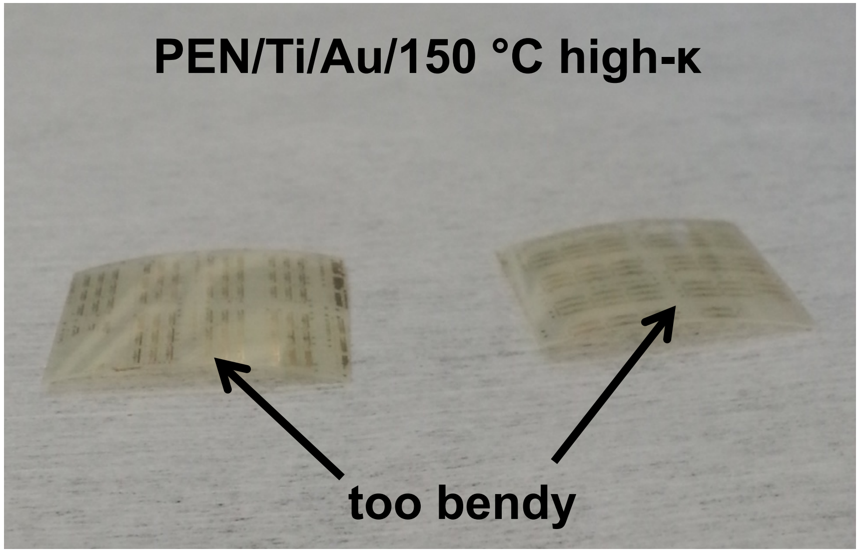
100 °C: PEN/Ti/Au/HfO_2/Ti/Au post-liftoff



- No cracks after metallization!
- Similar to PDMS, Au did not stick to Ti.

Caps on PEN – Other Processing Issues





- 10 mins on 150 °C hotplate is fine, but an hour at 150 °C in the MVD causes plastic deformation of PEN. The Headway is consequently unable to achieve vacuum. Resist gluing and kapton tape do not work to fasten it to a carrier wafer.
- ALD oxides deposited at 125 °C cause some bending, but substrates are still spinnable in the Headway. Alignment is very tricky, however. A quartz suppression wafer will be used in the future.

Observations - Processing on PDMS & PEN

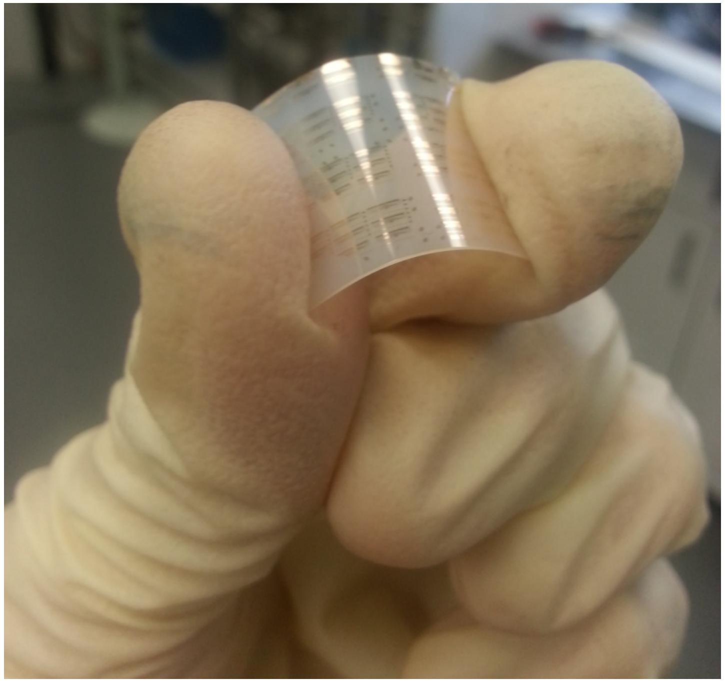
- Films of any kind on PDMS do not fare well above 100 °C.
- An initial layer of high-κ oxide is essential for resist adhesion, and helps prevent crud from sticking to the surface.
- It is beneficial to forgo LOR and sonicate during liftoff to minimize the thermal budget.
- Optical resist must be cured in the 90 °C oven.
- PDMS is a sub-optimal substrate for device processing

- PEN acquires an irreversible bend if processed for long at elevated temperatures (≥150 °C), but remains flat at 125 °C.
- Off-the-shelf PEN is very dirty, rough, and has scars. Microelectronics grade PEN is recommended for devices.
- PEN is much more robust to thermal expansion and processing abuse than PDMS.

Conclusions and Future Work

Observations

- Savannah and MVD oxides show very similar characteristics.
- ALD Al_2O_3 (HfO_2) is a stable process down to 125 °C (100 °C).
- PDMS is very tricky for lithography due to stickiness, thermal expansion, and hydrophobicity.
- PEN is an alternative substrate that is much easier to work with.



Immediate Future Work

- Order microelectronics grade PEN.
- Fabricate caps with 125 °C oxides in MVD.
- Continue to smooth out processing issues.

Thanks for listening!

Many thanks are due to Dr. Howe, Dr. Rincon, and Dr. Chen for training, guidance, and support!

Backup Slides

Process Flow - Details

- Begin with clean SiO_2/Si wafer pieces

Lithography:

- PMGI SF6 @ 3000 rpm for 60 seconds + hotplate
- SPR 3612 @ 5000 rpm for 40 seconds + 90 °C hotplate
- Define bottom electrode with KarlSuss
- Develop for 45 seconds

Metallization:

- Ebeam evaporate 2/38 nm Ti/Au
- Soak in Remover PG for 3 hours
- Spray with acetone, IPA
- Sonicate if necessary

Process Flow - Details

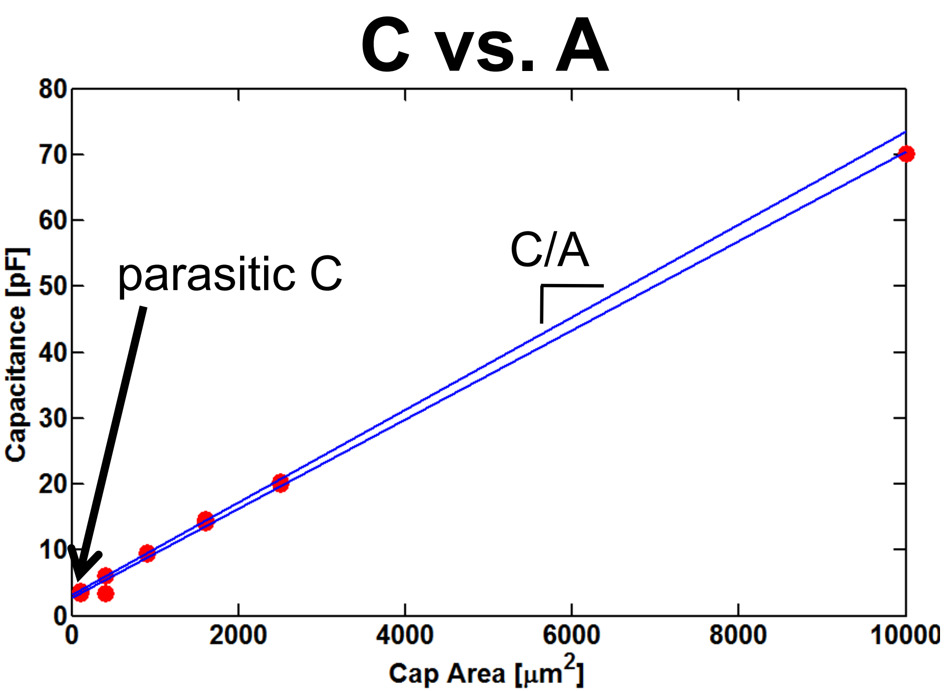
- Precondition ALD chamber with recipe to be used
- O_2 plasma in MRC: 20 mTorr, 20 sccm, 50 W, 2 mins
- Immediately transfer chips to ALD chamber, deposit oxide
- FGA in AllWin_r and fit thickness with Woollam

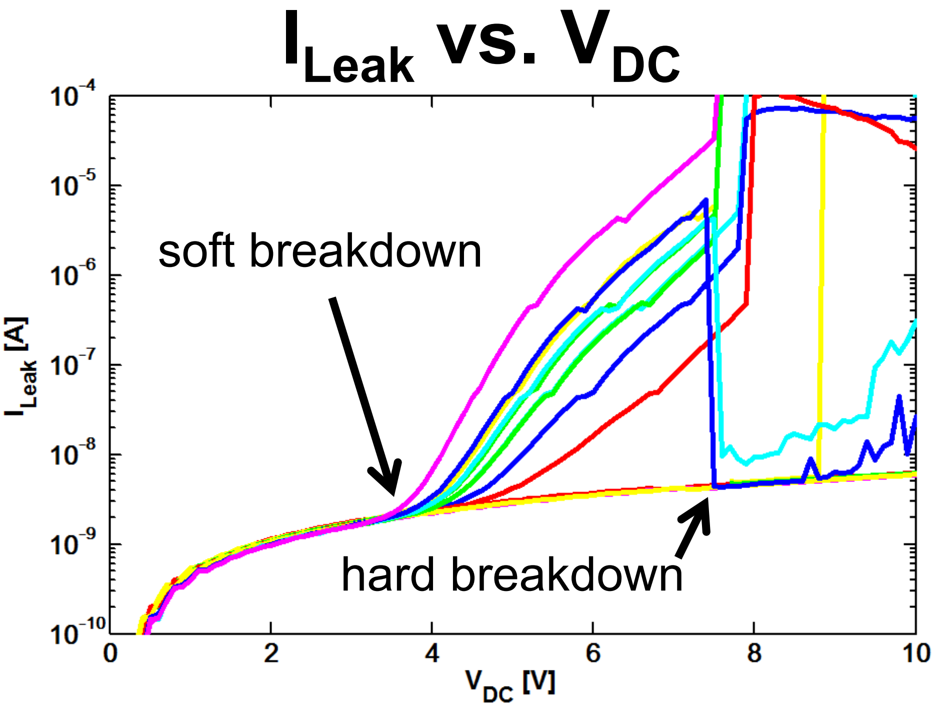
- Repeat lithography for top electrode

- Repeat metallization for top electrode

- Measure devices

Savannah - 200 °C Alumina, FGA





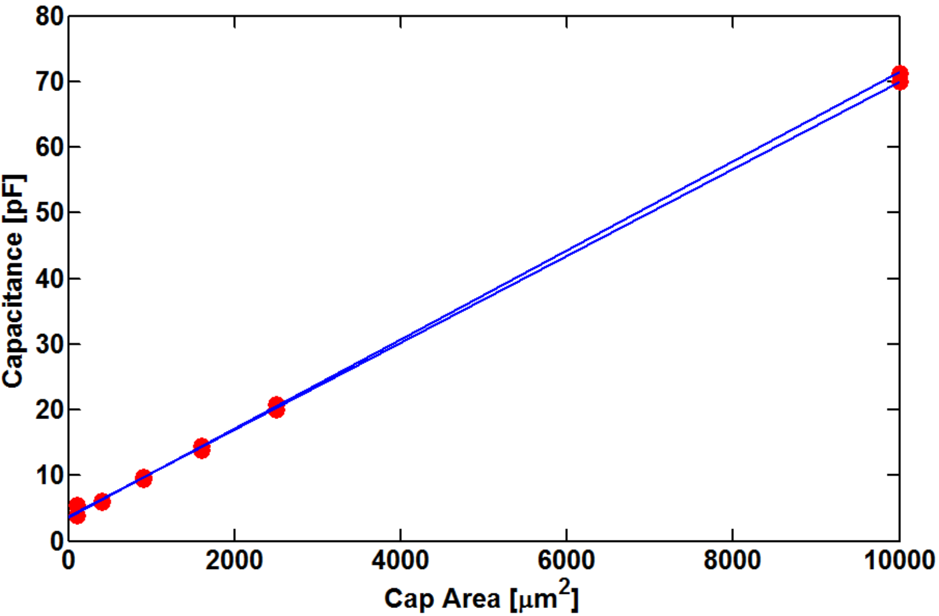
- C = 0.703 ± 0.060
- 0.677 ± 0.037 μF/cm^2
- R^2 = 0.998, 0.998
- d = 10.0 nm
- κ = 7.94 ± 0.68, 7.65 ± 0.42

note: κ values change by <1% for ±1 V_{DC}

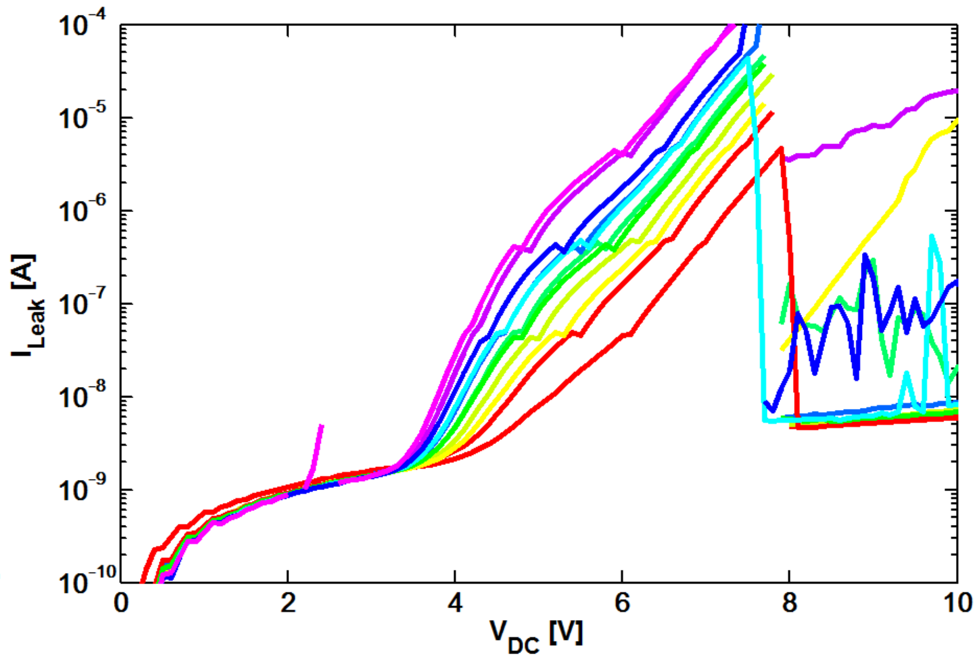
- I_{Leak} ~ nA
- $V_{BD,soft}$ ~ 3.5 V
- $E_{crit,hard}$ ~ 0.35 V/nm
- $V_{BD,soft}$ ~ 7.5 V
- $E_{crit,soft}$ ~ 0.75 V/nm

Savannah - 200 °C Alumina, O_2 anneal

C vs. A



I_{Leak} vs. V_{DC}

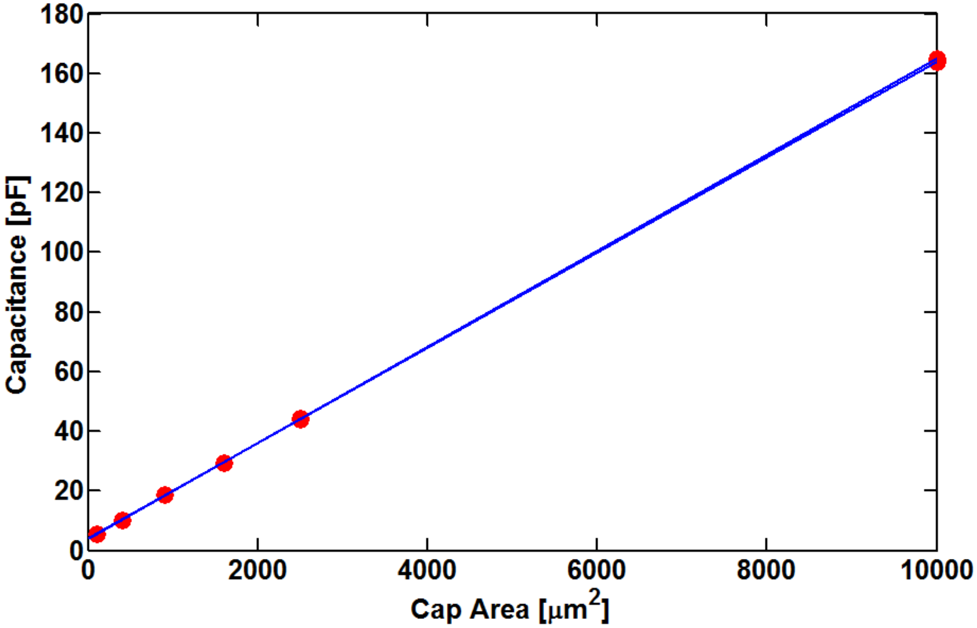


- C = 0.662 ± 0.021
- 0.679 ± 0.009 μF/cm²
- R^2 = 0.999, 1.000
- d = 10.0 nm
- κ = 7.48 ± 0.23, 7.67 ± 0.10

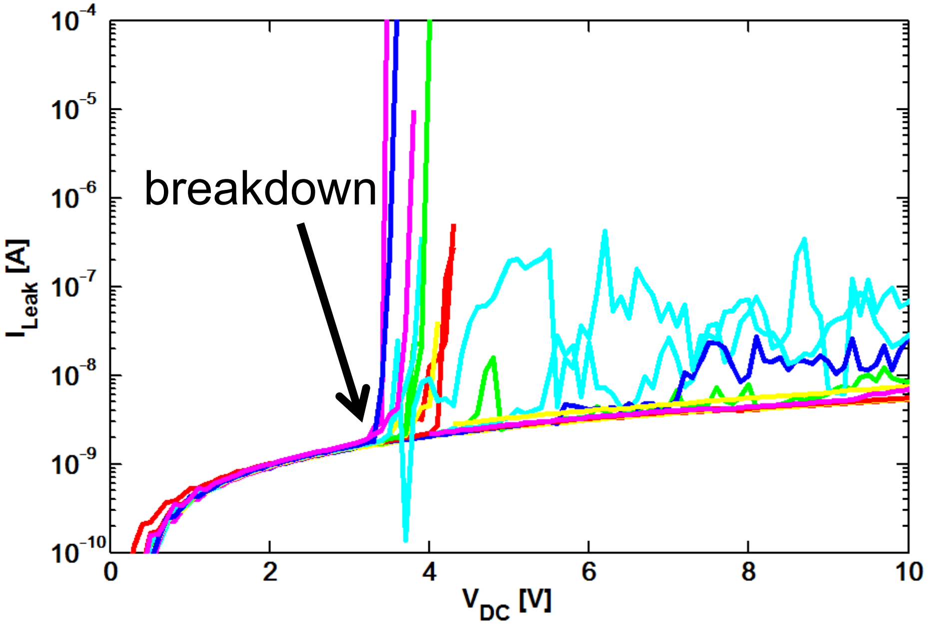
- I_{Leak} ~ nA
- $V_{BD,soft}$ ~ 3.5 V
- $E_{crit,hard}$ ~ 0.35 V/nm
- $V_{BD,soft}$ ~ 7.8 V
- $E_{crit,soft}$ ~ 0.78 V/nm

Savannah - 200 °C Hafnia, FGA

C vs. A



I_{Leak} vs. V_{DC}

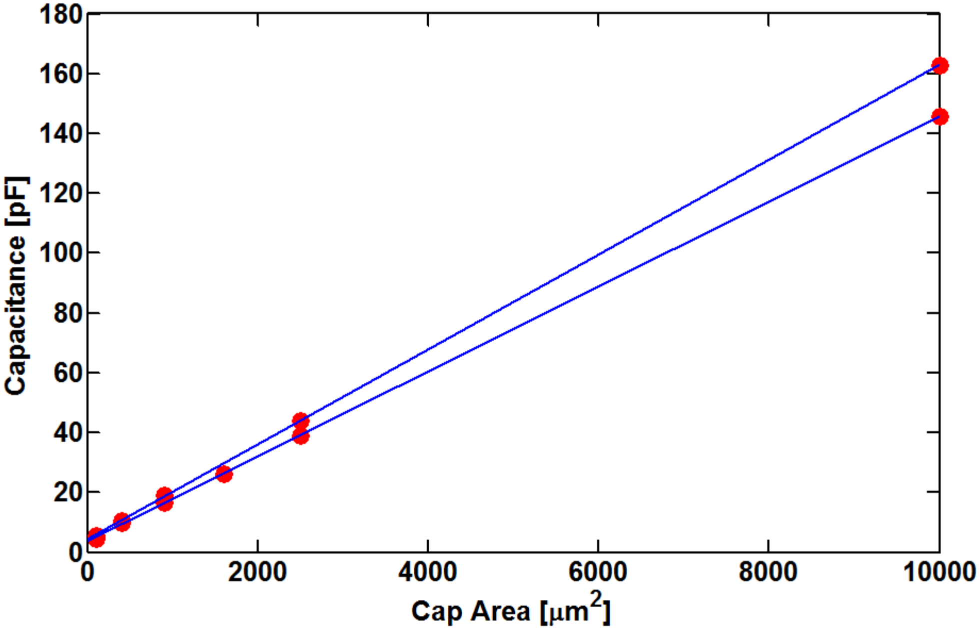


- C = 1.60 ± 0.007
- 1.61 ± 0.004 μF/cm^2
- R^2 = 1.000, 1.000
- d = 8.7 nm
- κ = 15.70 ± 0.07, 15.84 ± 0.04

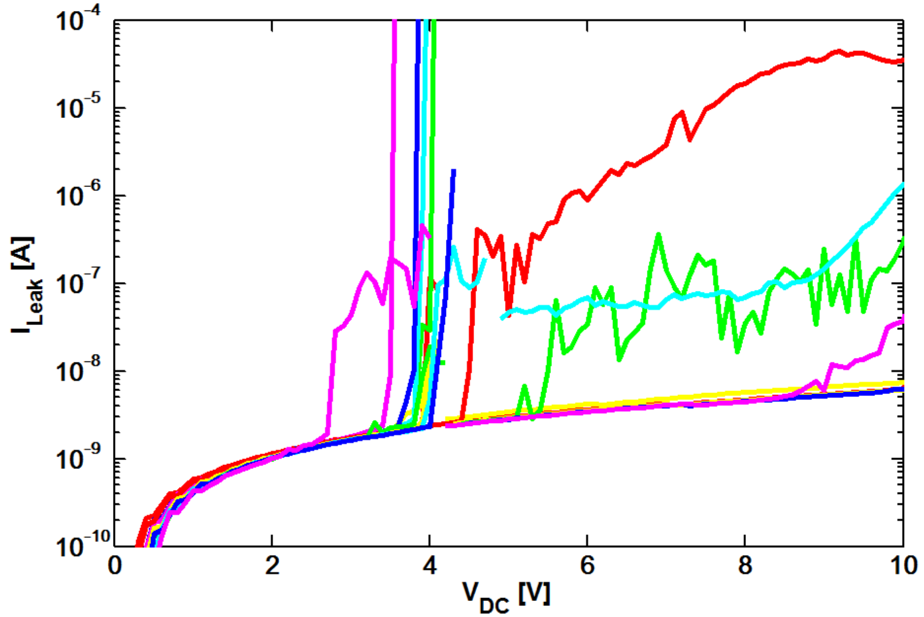
- I_{Leak} ~ nA
- V_{BD} ~ 3.2 V
- E_{crit} ~ 0.37 V/nm

Savannah - 200 °C Hafnia, O_2 anneal

C vs. A



I_{Leak} vs. V_{DC}

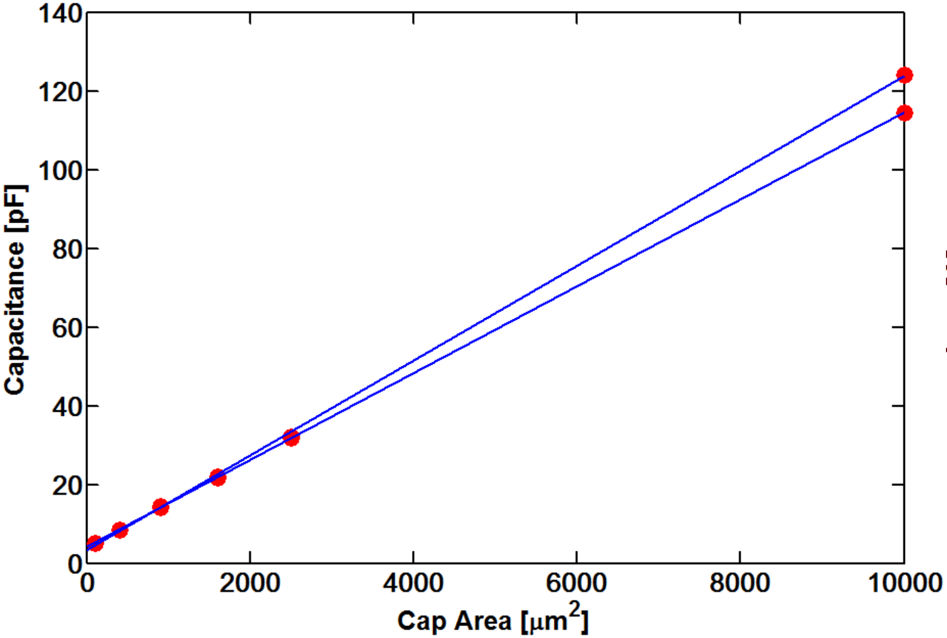


- C = 1.59 ± 0.011
- 1.42 ± 0.014 μF/cm²
- R^2 = 1.000, 1.000
- d = 8.7 nm
- κ = 15.59 ± 0.11, 13.95 ± 0.14

- I_{Leak} ~ nA
- V_{BD} ~ 3.2 V
- E_{crit} ~ 0.37 V/nm

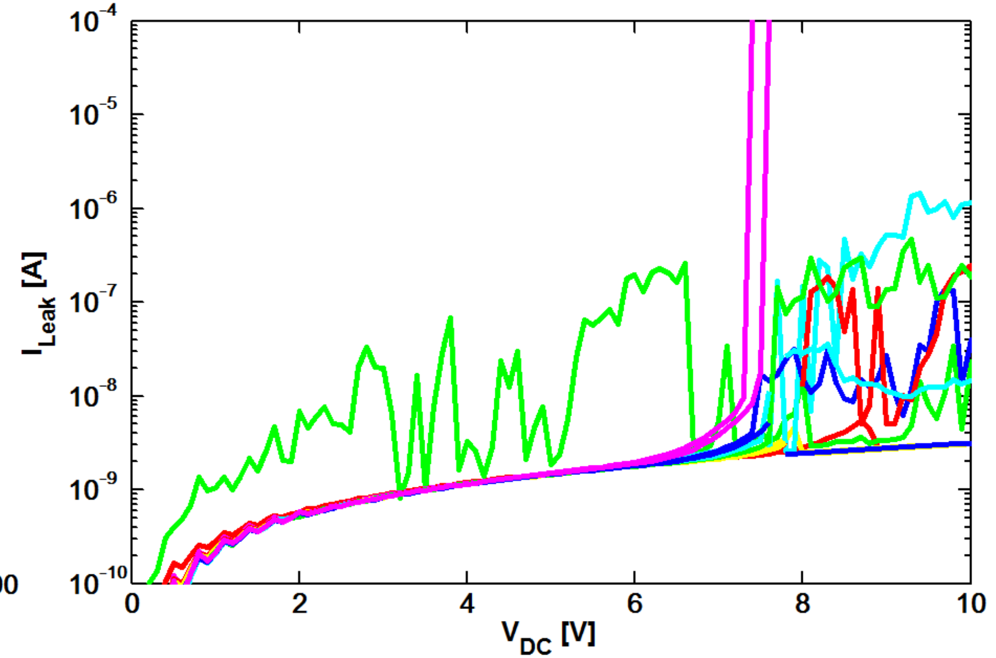
Savannah - 100 °C Hafnia, 150 °C FGA

C vs. A



- C = 1.20 ± 0.03
- 1.10 ± 0.01 μF/cm^2
- R^2 = 1.000, 1.000
- d = 11.9 nm
- κ = 16.2 ± 0.4, 14.8 ± 0.1

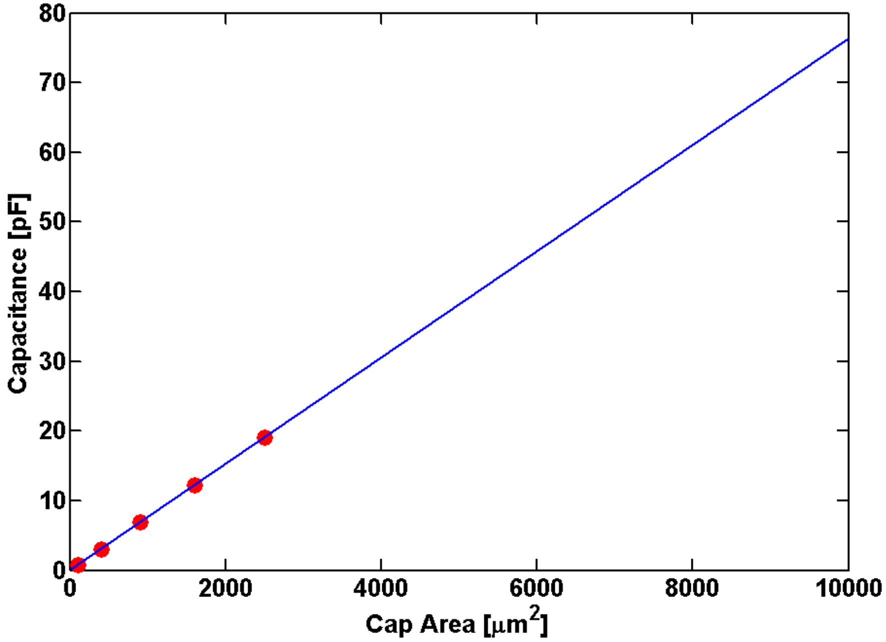
I_{Leak} vs. V_{DC}



- I_{Leak} ~ nA
- V_{BD} > 6.0 V
- E_{crit} ~ 0.50 V/nm

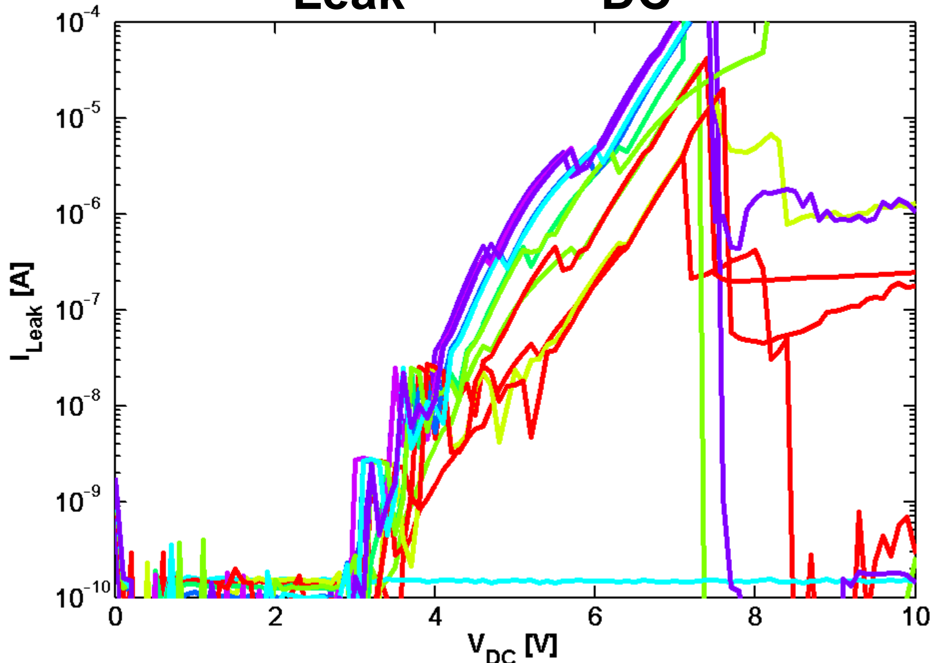
MVD - 125 °C Alumina + 125 °C FGA

C vs. A



- C = 0.762 ± 0.001 µF/cm²
- R^2 = 1.000
- d ≈ 8.9 nm
- κ ≈ 7.7 ± 0.02

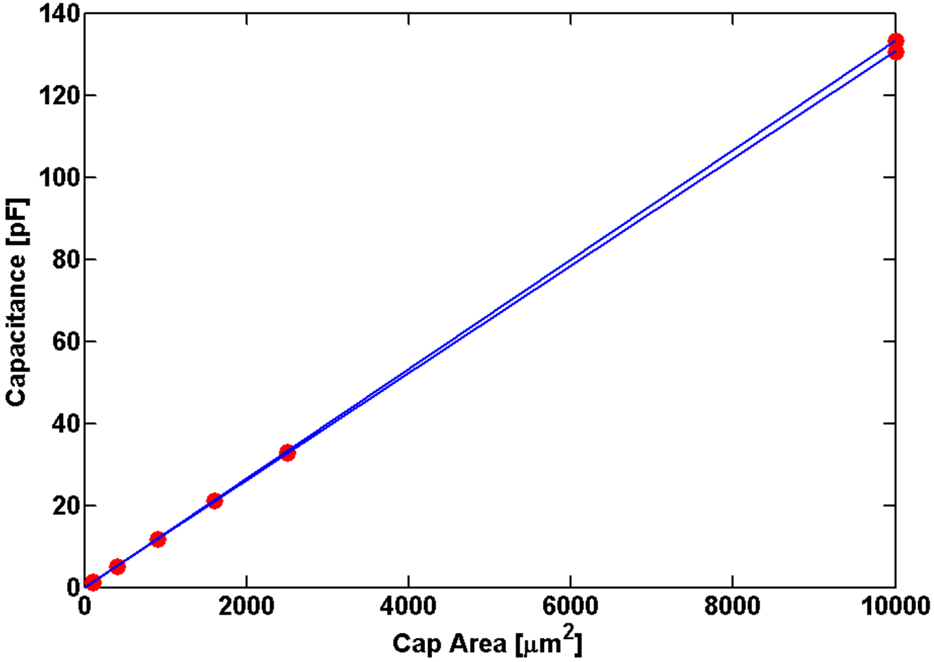
I_{Leak} vs. V_{DC}



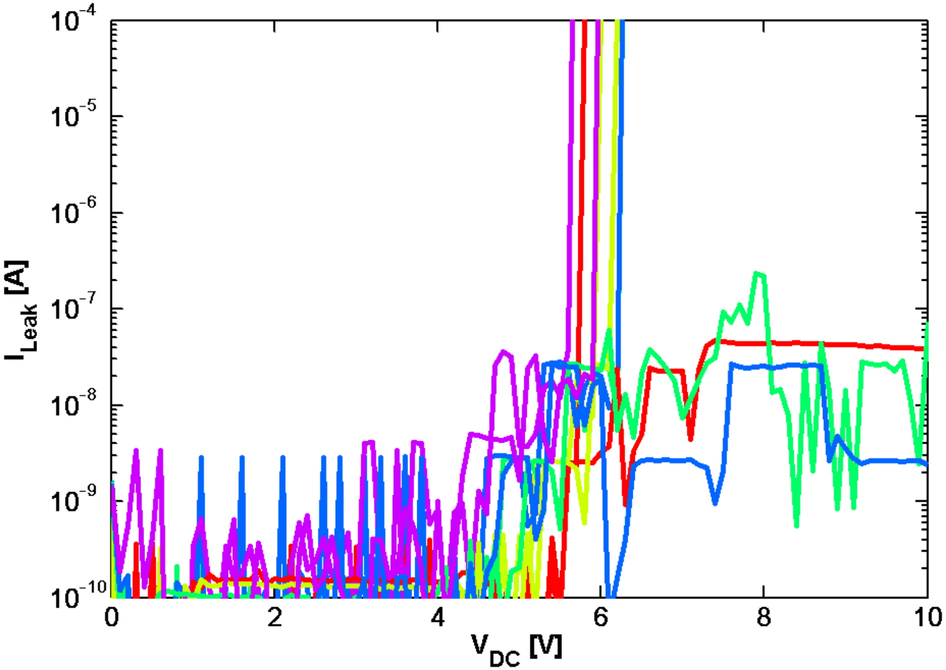
- I_{Leak} < nA
- V_{BD} > 3.0 V
- E_{crit} ~ 0.34 V/nm

MVD - 100 °C Hafnia + 100 °C FGA

C vs. A



I_{Leak} vs. V_{DC}

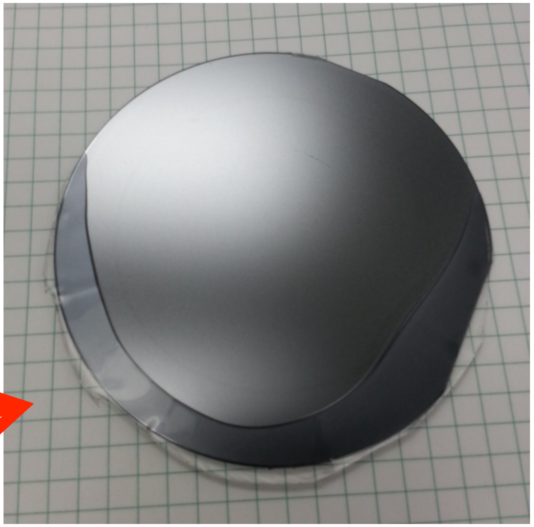


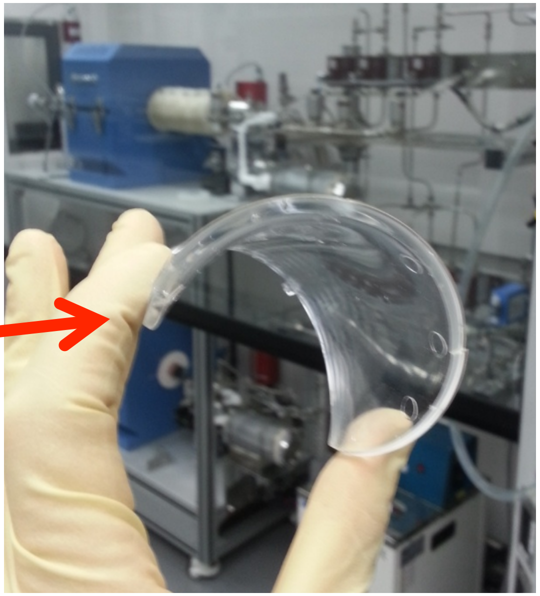
- C = 1.33(4) ± 0.004
- 1.30(7) ± 0.003 μF/cm²
- R^2 = 1.000, 1.000
- d = 11.3 nm
- κ = 17.03 ± 0.0(5), 16.6(9) ± 0.03

- I_{Leak} < nA
- V_{BD} > 5.5 V
- E_{crit} ~ 0.49 V/nm

First PDMS Thickness Experiments

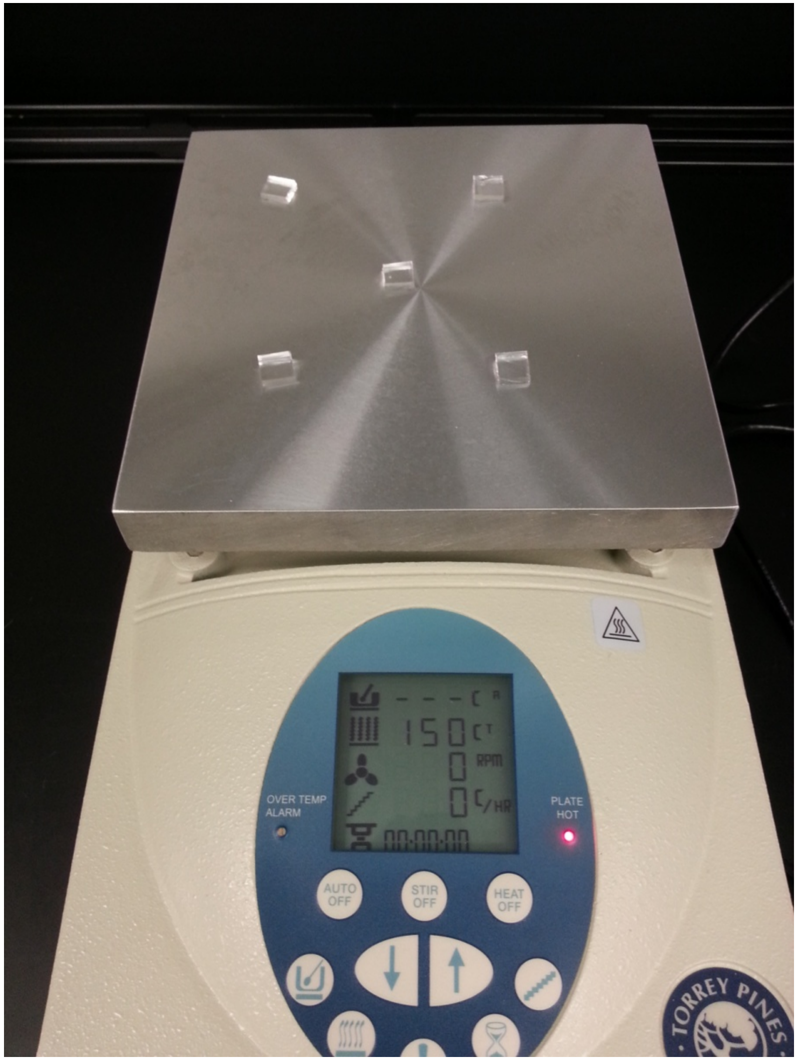
- Si wafer – 500 rpm for 30 s
  - μ = 0.75 mm, σ = 0.06 mm
- Si wafer – 500 rpm for 15 s
  - μ = 0.79 mm, σ = 0.02 mm
- Si wafer – 100 rpm for 15 s
  - Could not accurately measure
- Pyrex dish – let sit
  - μ = 3.67 mm, σ = 0.52 mm
  - Could not remove from mold
- Fluoroware lid – let sit
  - μ = 3.46 mm, σ = 0.16 mm



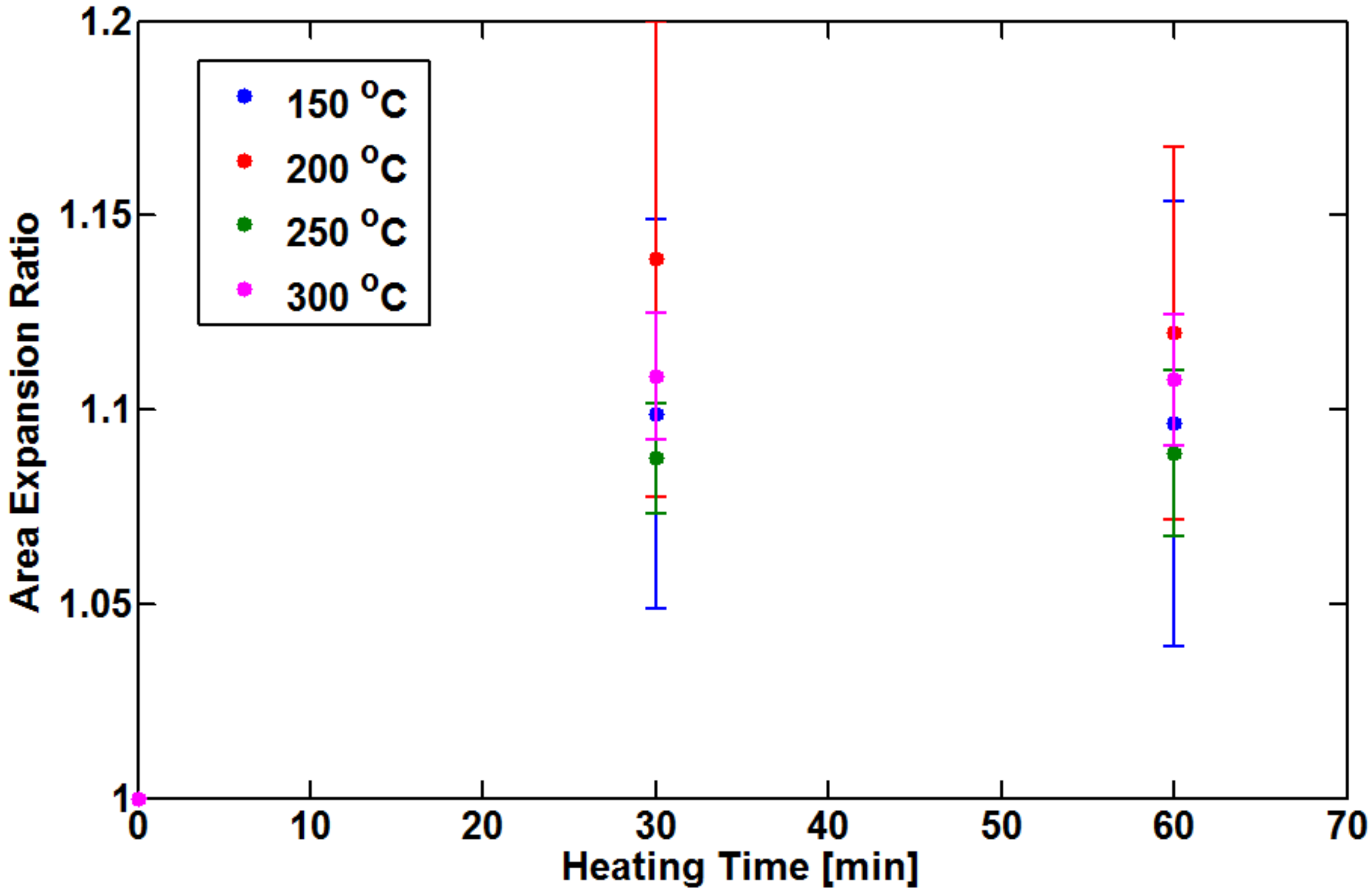


PDMS Thermal Integrity

- Five squares approximately 10x10 mm^2 were cut and heated.
- Height and width were measured with calipers at 30 and 60 minutes of heating for various temperatures.
- PDMS was fine up through an hour at 300 °C.



PDMS Thermal Integrity



- Data points → average area ratio
- Error bars → one standard deviation
- PDMS also able to withstand 300 °C H_2/Ar anneal for 1 hour