SiNWs Thermoelectric Device Process Development

ENGR 241 Autumn 2019

FINAL PRESENTATION

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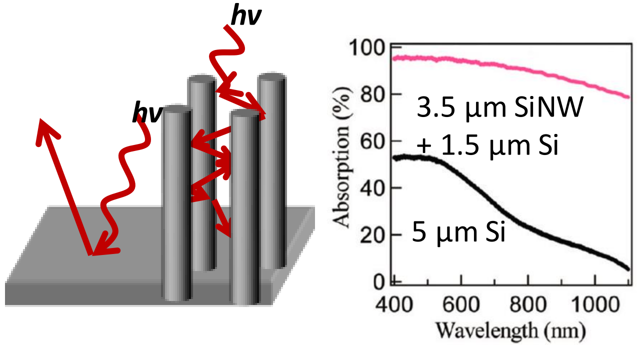
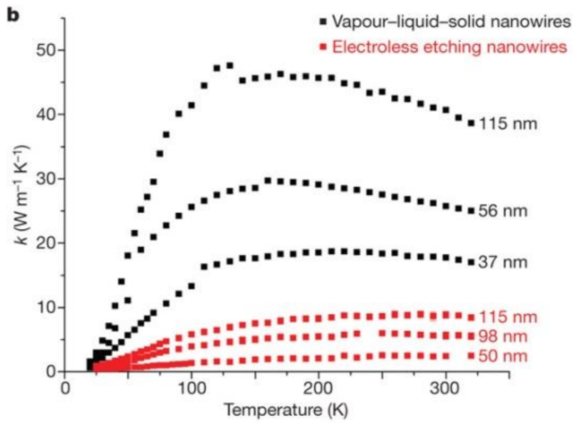
Contents

Objectives and Background

- **Goal**
  - To develop porous Silicon nanowires (SiNWs) thermoelectric (TE) devices with high ZT and optimal amount of porosity using metal assist chemical etching (MACE) or metal assisted anodic etching (MAAE) method
  - To develop sub-micron nanoimprint lithography (NIL) and photo lithography (PL) patterning SOPs for SNF.
- TE figure of merit: $ZT = \frac{\sigma S^2 T}{k}$ (vapor-compression cycle refrigerator ZT ~ 3.0)
  - Density of carriers↓, S↑, k dominated by phonons, decoupled σ and k
- SiNWs Thermoelectric device:
  - 100-fold ZT over bulk Si
- Nanowire advantages:
  - Quantum confinement: size ~ electron & phonon wavelength ⇢ $S^2\sigma$↑
  - Boundary scattering: e mean free path < size(~300nm) < phonon mean free path ⇢ k↓

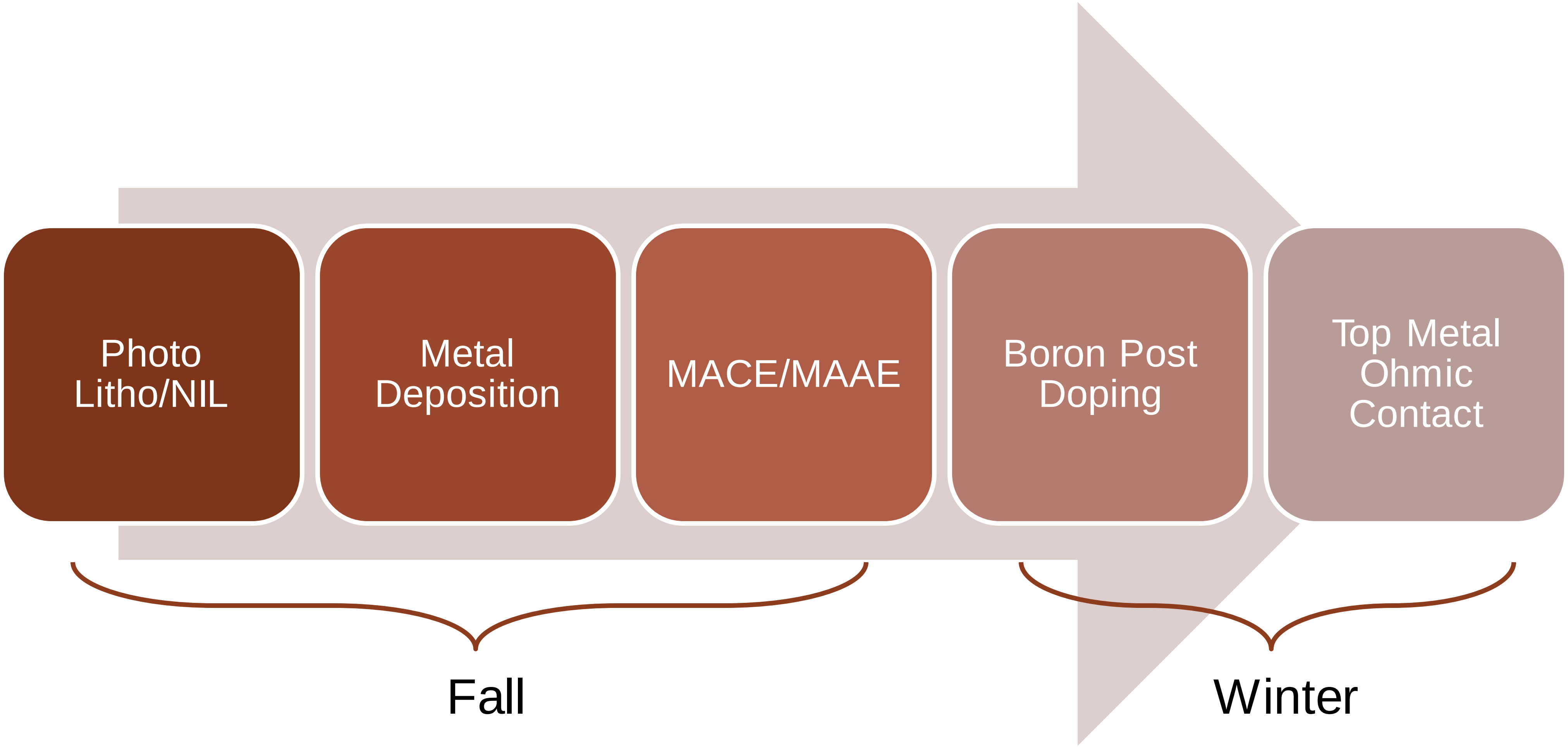


Kayes, B.M., *et. al.*, PVSC '08. 33rd IEEE, 2008

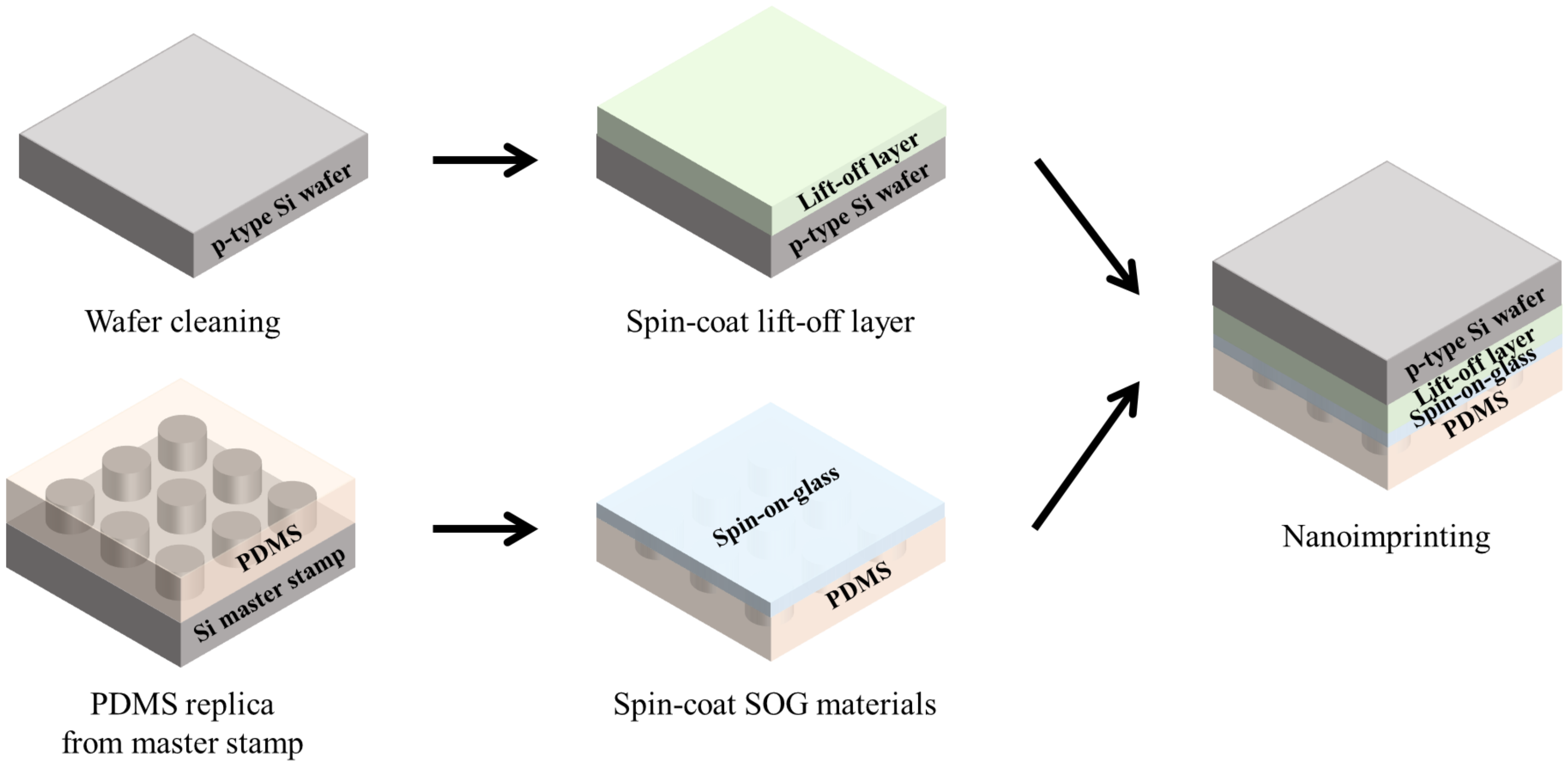


Hochbaum, A. I., *et. al.*, Nature 2008, 451, 163-168

Process Overview

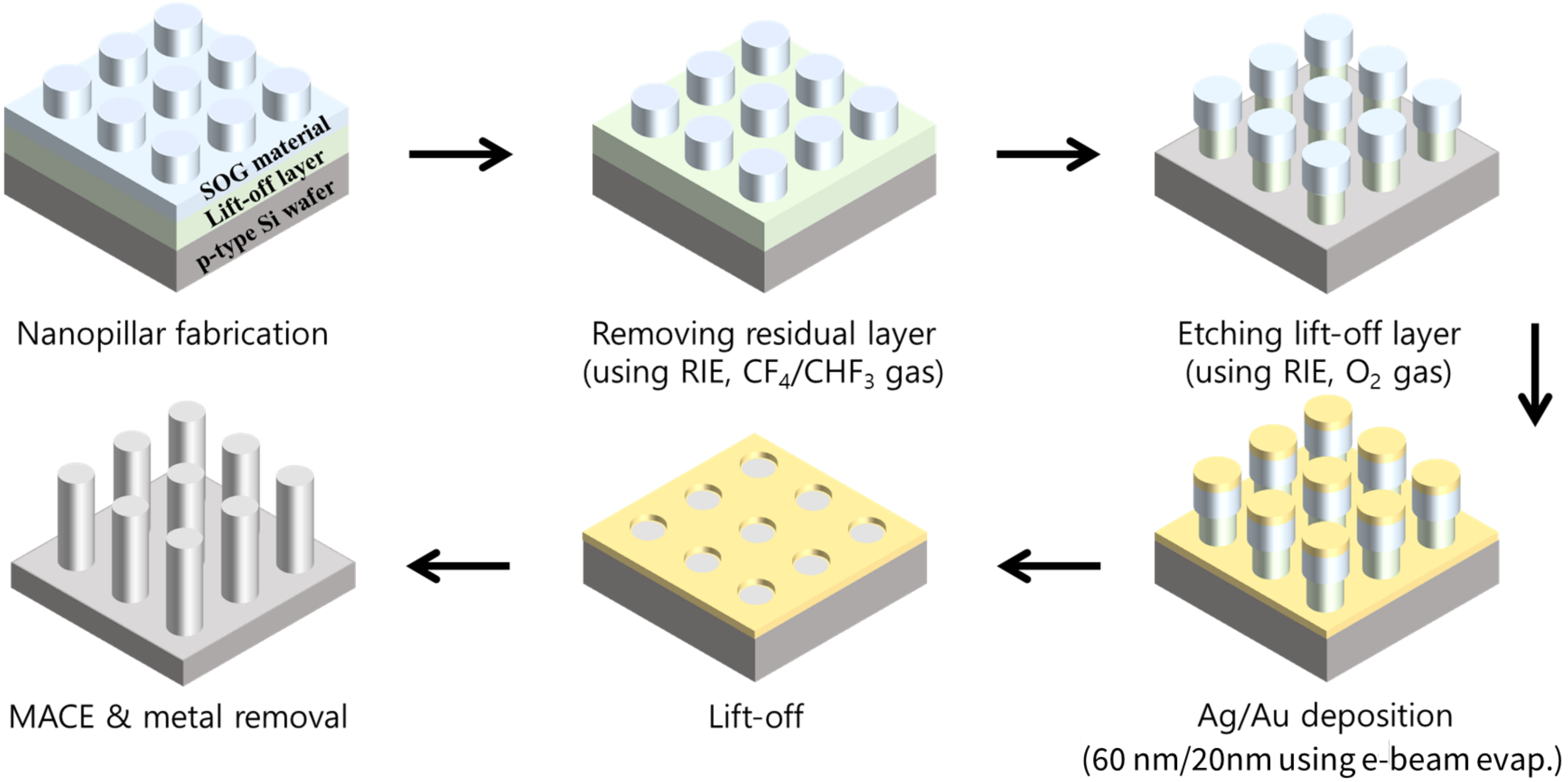


Method (Nanoimprint Lithography)

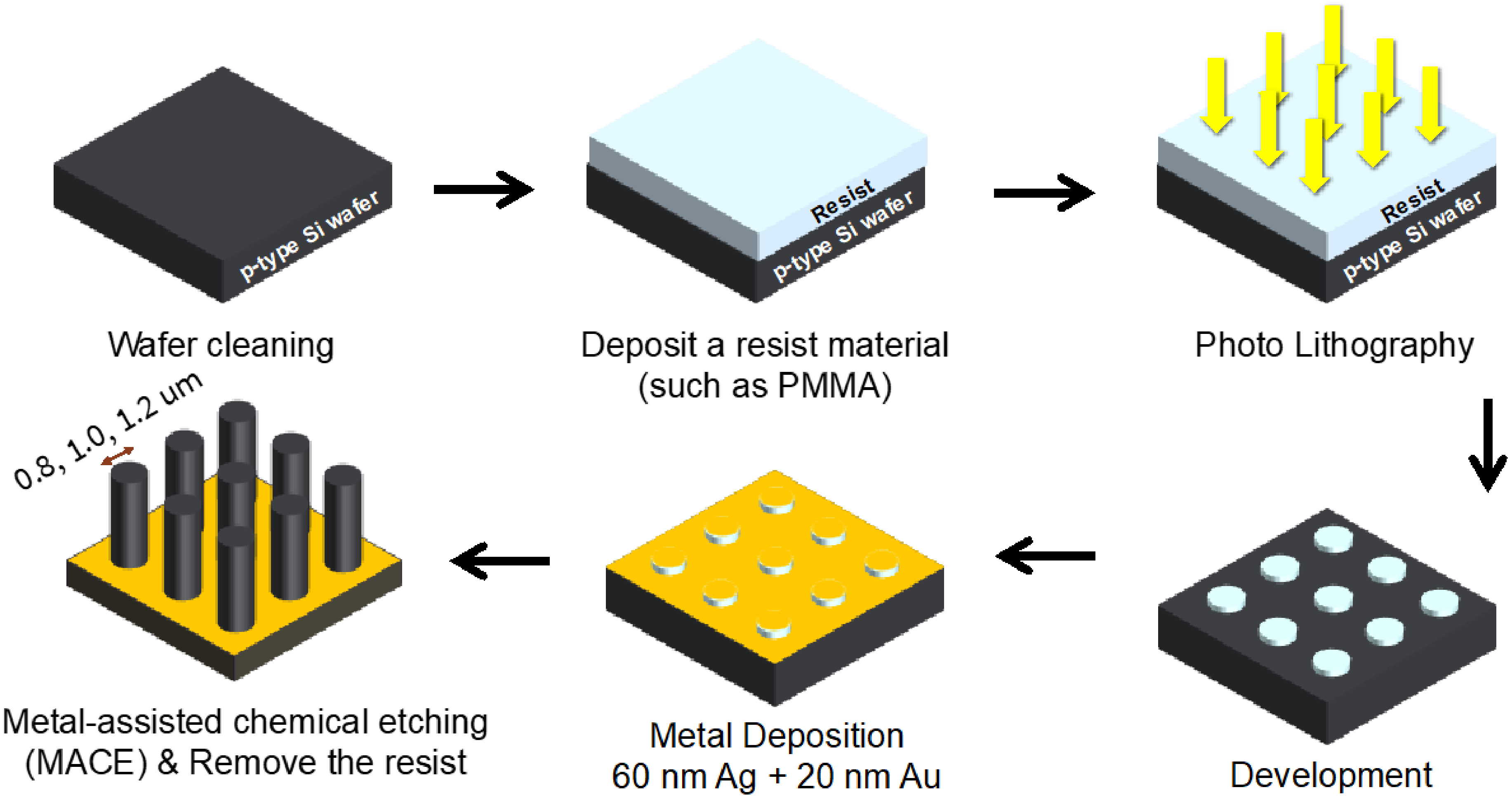


Circle Pattern Diameter: < 300 nm

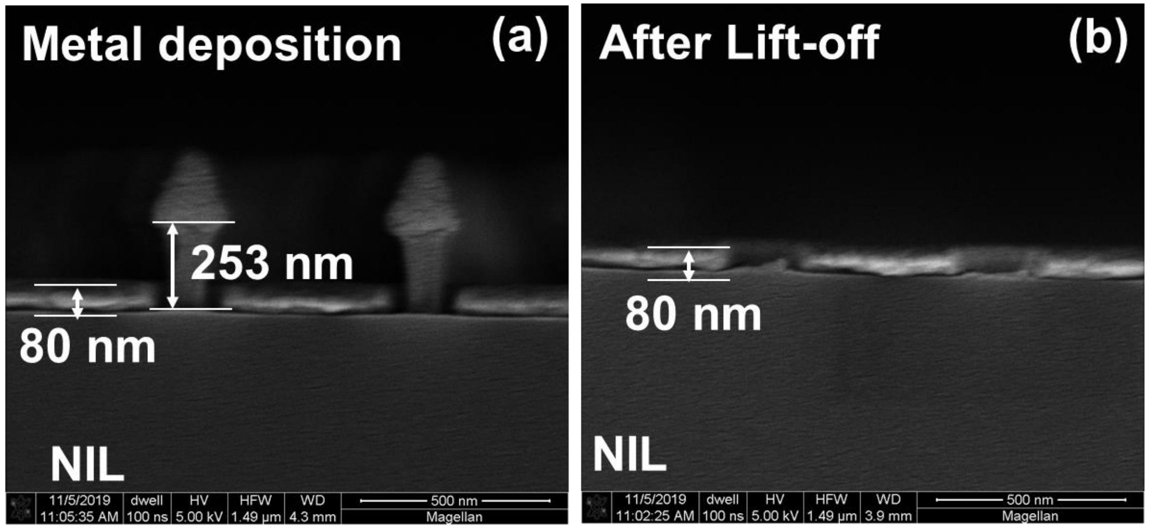
Method (Nanoimprint Lithography)



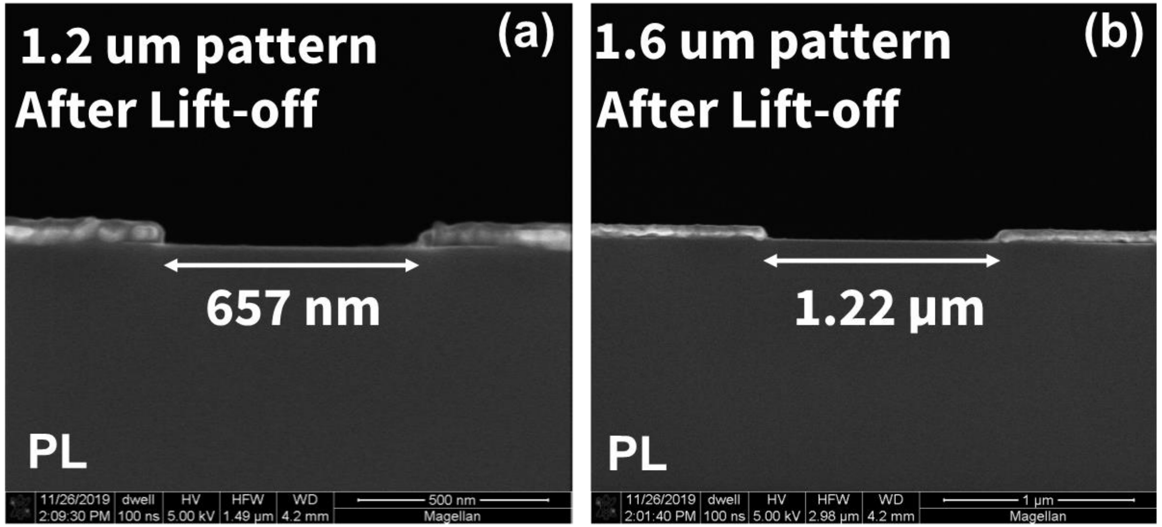
Method (Photolithography)



Results



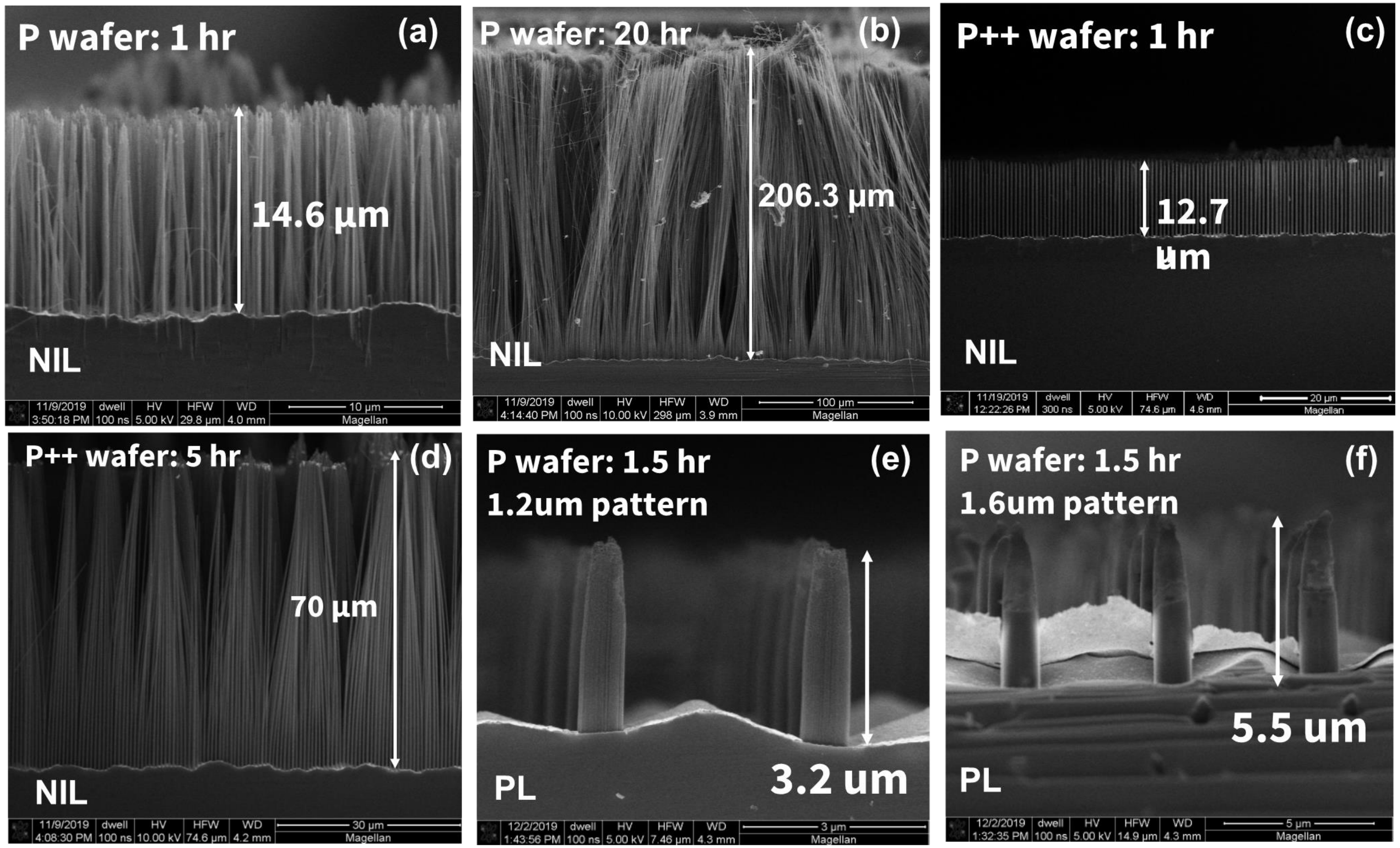
SEM images of the NIL patterned metal layer (a) before and (b) after lift-off.



SEM images of the PL patterned metal layer with (a) 1.2 μm and (b) 1.5 μm square mask dimensions after lift-off.

- Pattern: achieved sub micron features using both patterning methods
  - NIL: achieved ~ 150-200 nm pattern by NIL and RIE process.
  - PL: achieved ~ 650 nm pattern by 1.2 μm square mask dimension; achieve ~ 1.2 μm pattern by 1.5 μm square mask dimension.

Results



SEM images of SiNWs fabricated by NIL patterned p type wafer with (a) 1 hr MACE, (b) 20 hr MACE; NIL patterened p++ type wafer with (c) 1 hr MACE, (d) 5 hr MACE; (e)1.2 um, (f) 1.6 um square array PL patterned p type wafer with 1.5 hr MACE.

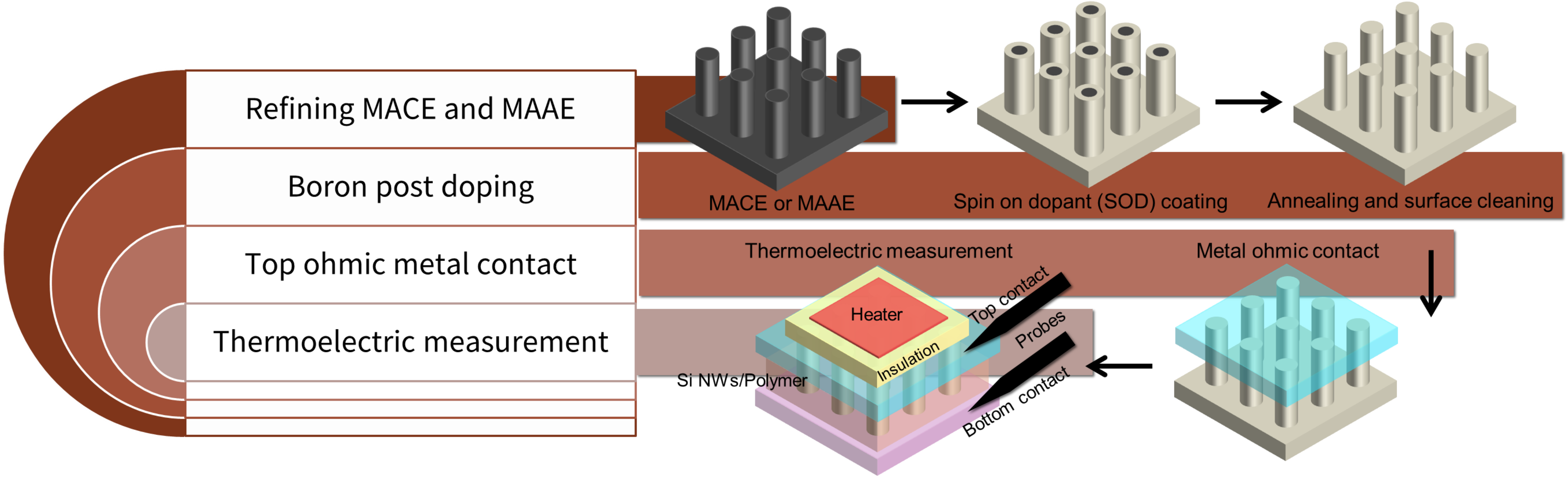
- MACE:
  4.8M HF + 0.3M H_2O_2
  - NIL: fabricated SiNWs using p (5-10 Ωcm) type and p++ (0.005 Ωcm) type of Silicon wafers.
  - PL: fabricated SiNWs using p type Silicon wafer.

Discussions

- Array of SiNWs with **high aspect ratio (> 900)** was fabricated using NIL, RIE and MACE.

- Findings:
  - Effective NIL+RIE and PL SOPs were developed to pattern uniform lift-off layer on p, and p++ Si wafers.
  - Optimal etching conditions for MACE of p and p++ Si wafers were found. Etch rates under these conditions were obtained.

Future Plan (Winter quarter)



- Refine MACE and explore MAAE process for better controllability of SiNWs fabrication.
- Boron post doping of the fabricated SiNWs.
- Create top ohmic metal contact of the SiNWs array.
- Thermoelectric performance measurement.

Budget

Budget			
Detailed Cost ($)	Training	Equipment Usage	Materials
	1060	3025.34	333.2
Overall Cost ($)	4418.54		
Proposed Budget ($)	4985		
Remaining ($)	566.46		