A quick turnaround device process
EE410 redesign

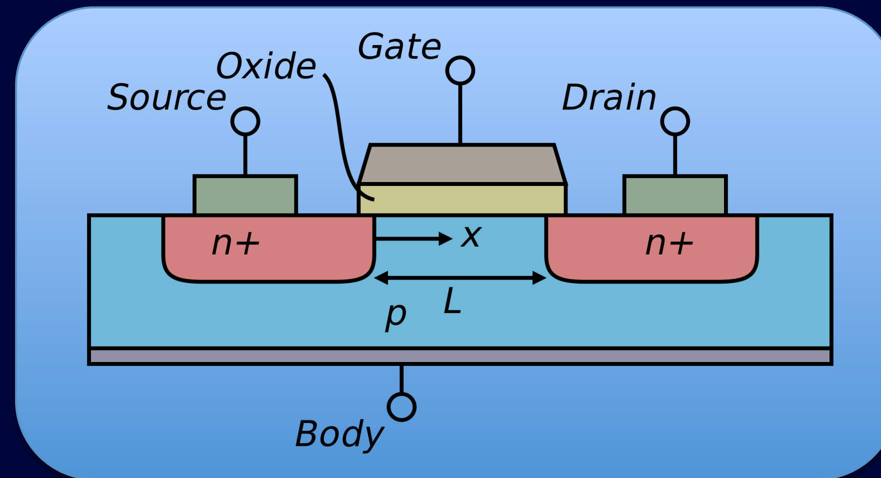
Max Shulaker, Rebecca Park

Prof. Roger Howe, Usha Raghuram

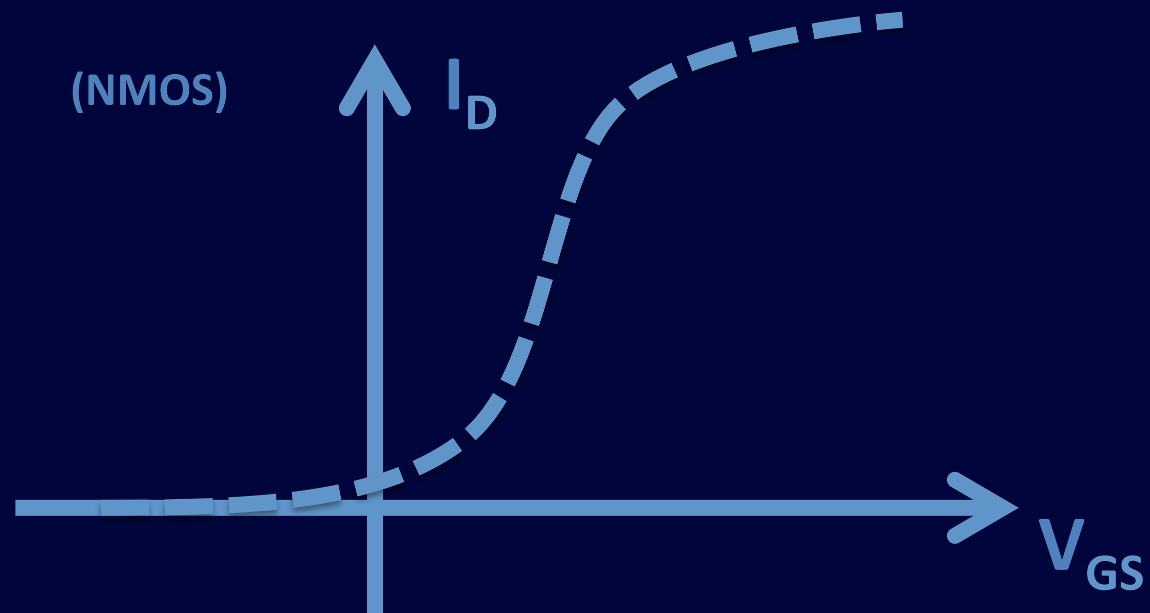
Key Points

- Target yield: >99.9999%
- Clean + Gold Contaminated Process Flows
- Total flow time: <5 days
- Depletion mode logic (NMOS)
- SNF Standard Cell Library
  - Digital logic cells (inv, nand2, nor2, etc.)
  - Simple analog amplifiers

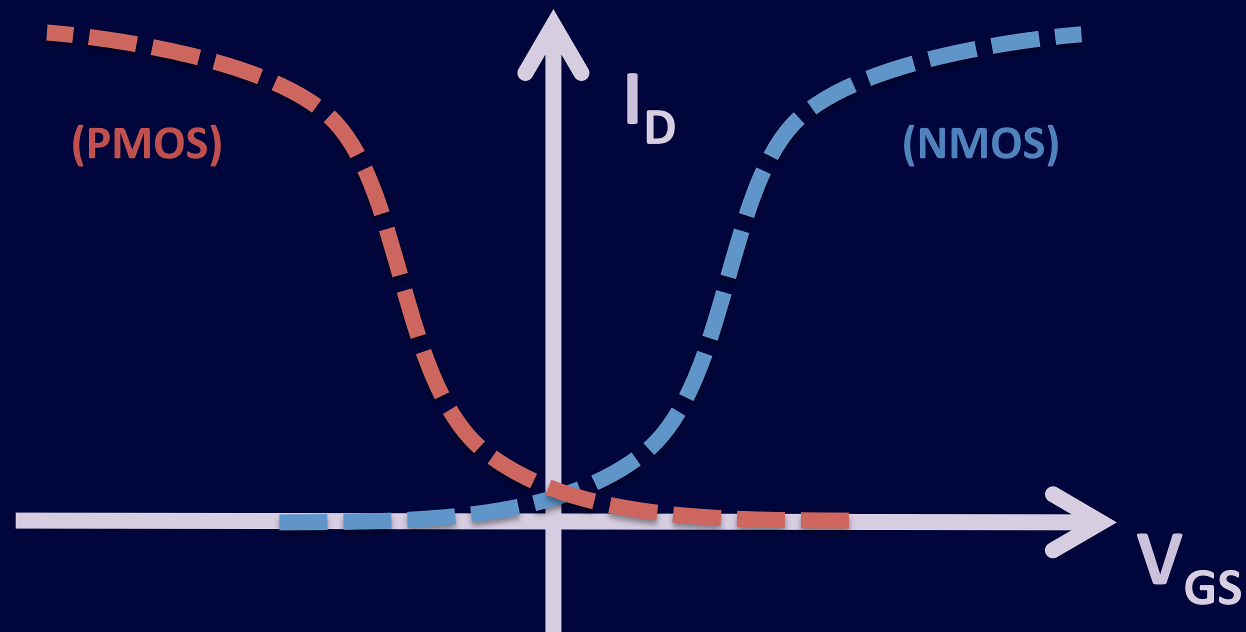
What is a transistor?



(NMOS)

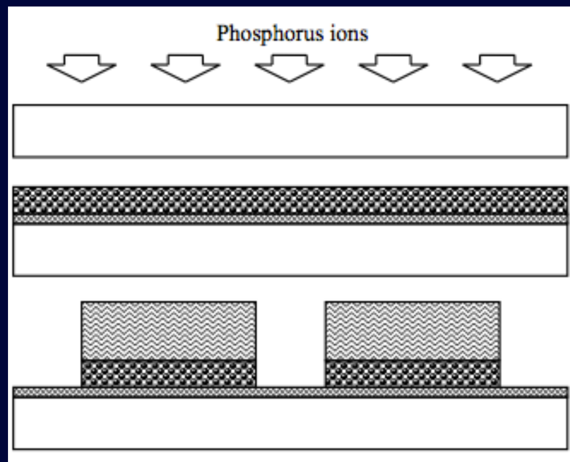


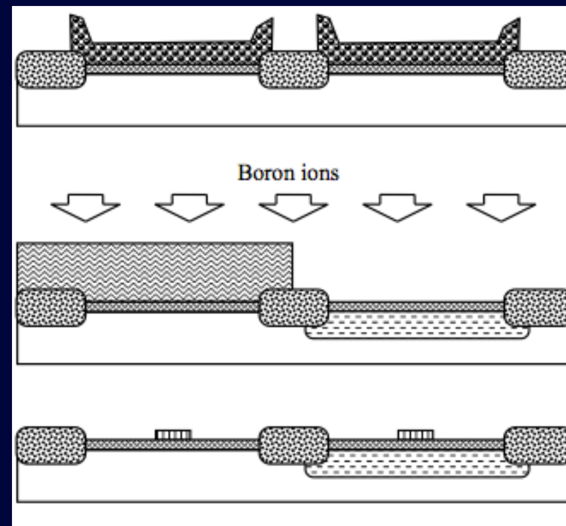
For CMOS processing, we need both

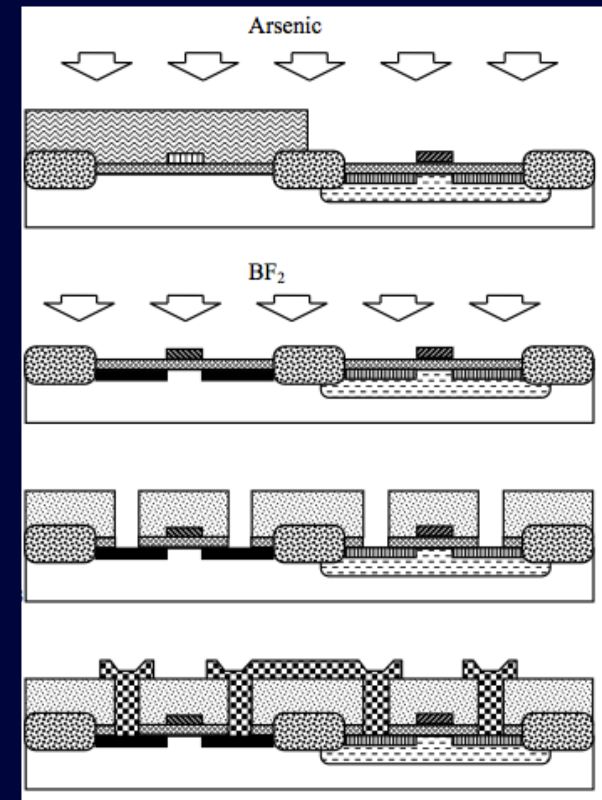
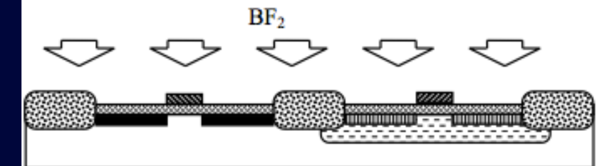


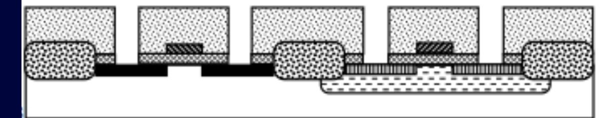
CMOS-LOCOS (EE410)

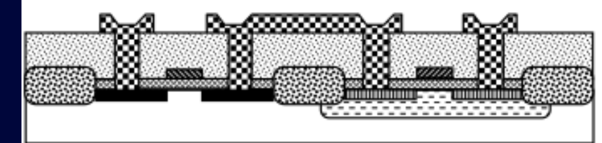
Process	CMOS-LOCOS
Implantation	4
Photolithography Layers	7
Deposition	4
Furnace (Oxidation + Anneal)	4
Contact Hole Etch	1



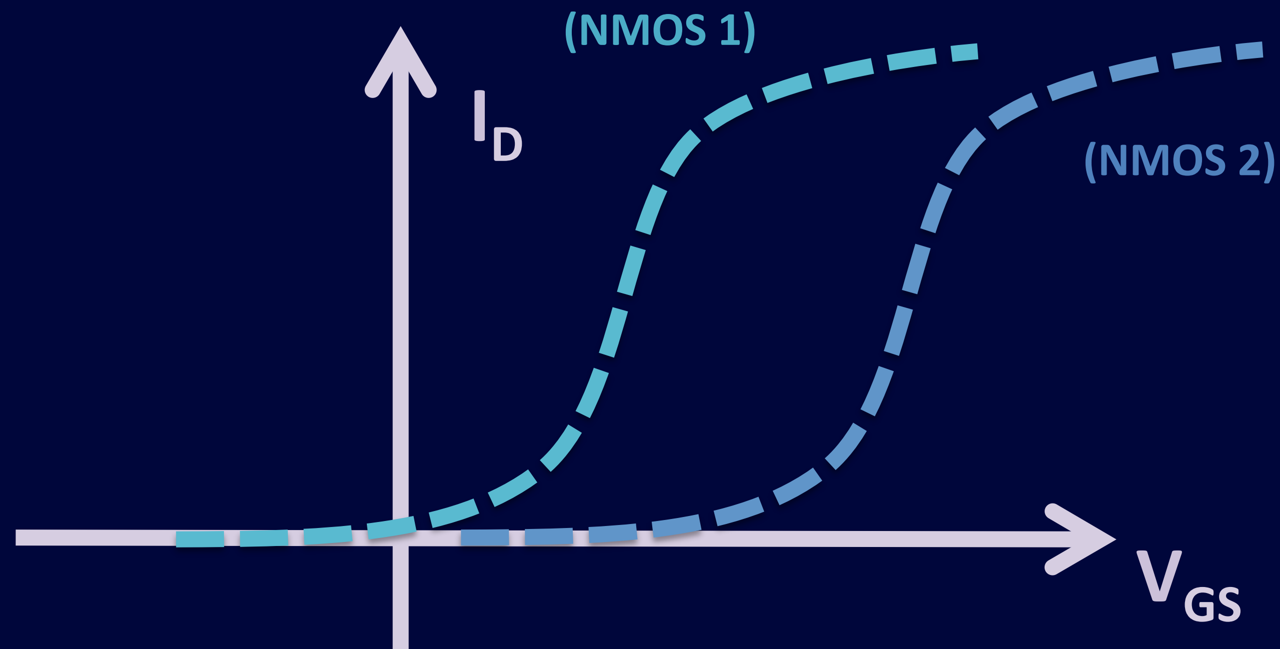






Or, we can do something like…



NMOS-Depletion (new EE410)

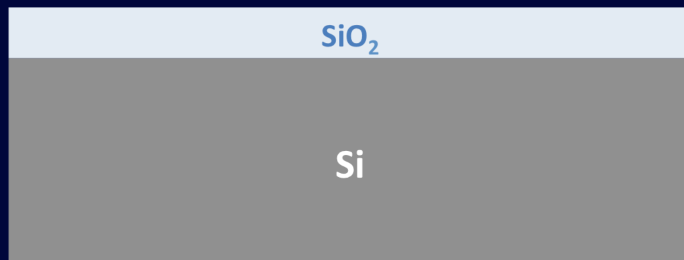
Process	CMOS-LOCOS	NMOS-Depletion
Implantation	4	3
Photolithography Layers	7	5
Deposition	4	1
Furnace (Oxidation + Anneal)	4	1
Contact Hole Etch	1	1

Main advantage of NMOS-Depletion mode:

Due to the ***simplified*** silicon process, EE410 students gain ***hands-on*** fabrication experience.

NMOS-Depletion Process Flow

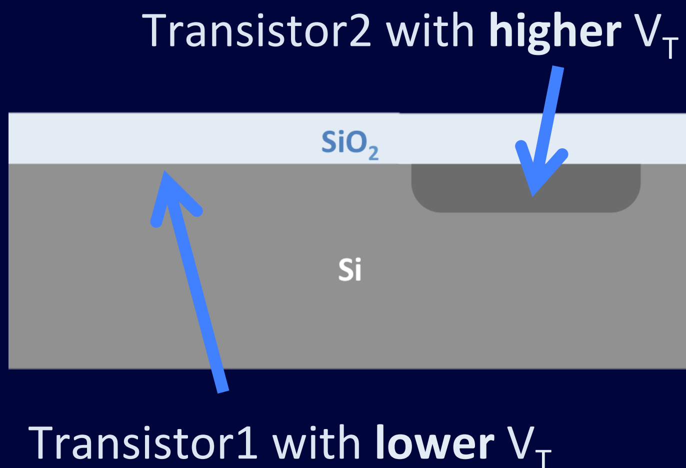
Thermal Oxidation



	Equipment	Purpose	Processing Details
1	wbnonmetal	wafer cleaning	i. Piranha (9:1 H2SO4:H2O2) 120°C for 20 minutes ii. Water dump rinser iii. 50:1 HF dip for 30 seconds iv. Water dump rinser v. SRD
2	wbclean		i. RCA clean (bath 1) 50°C for 10 minutes ii. Water dump rinser iii. 50:1 HF dip for 30 seconds iv. Water dump rinser v. RCA clean (bath 1) 50°C for 10 minutes vi. Water dump rinser vii. 50:1 HF dip for 30 seconds viii. Water dump rinser ix. SRD
3	Thermco1	thermal oxidation	900°C, 2hr:40min:00sec, dry oxidation Oxide thickness target ~30nm (If oxide is too thick, etch bath in 50:1 HF in wbclean. Etch rate is ~ 4nm/min.)
		Check oxide thickness using Nanospec or Woollam.	

High V_T well implant

Transistor2 with **higher** V_T



Transistor1 with **lower** V_T

	Equipment	Purpose	Processing Details
1	YES Oven	prime wafers	
2	SVG Resist Coat	coat photoresist	Program 7 - PR 3612 1um w/o VP backside EBR only
3	ASML	expose	**wafers must be cleaned in SRD to minimize particle contamination in ASML* Mask: Jobfile: Exposure dose: 50
4	SVG Developer	bake and develop	(Initial bake) Developer 9 / Hot plate 1 (Develop + post bake) Developer 3 / Hot plate 1
	Check developed region under microscope.		
5	Oven 110°C	harden the resist so that it withstands the implantation	Bake for 30 minutes
6	Drytek2	descum (to remove residual photoresist before implantation)	**season chamber for 10 minutes* **make sure to use clean slots* Program 1 - pressure 150mTorr, oxygen flow 100sccm, power 250W (~0W reflected) for 40 seconds
7	Send out for Implantation	High V_T well implant	**The implantation is done outside of SNF* Boron 1e13 cm^{-2}, 60 keV, 7° tilt
8	gasonics	remove photoresist	Program 016
9	wbnonmetal	wafer cleaning	i. Piranha (9:1 H2SO4:H2O2) 120°C for 20 minutes ii. Water dump rinser iii. SRD

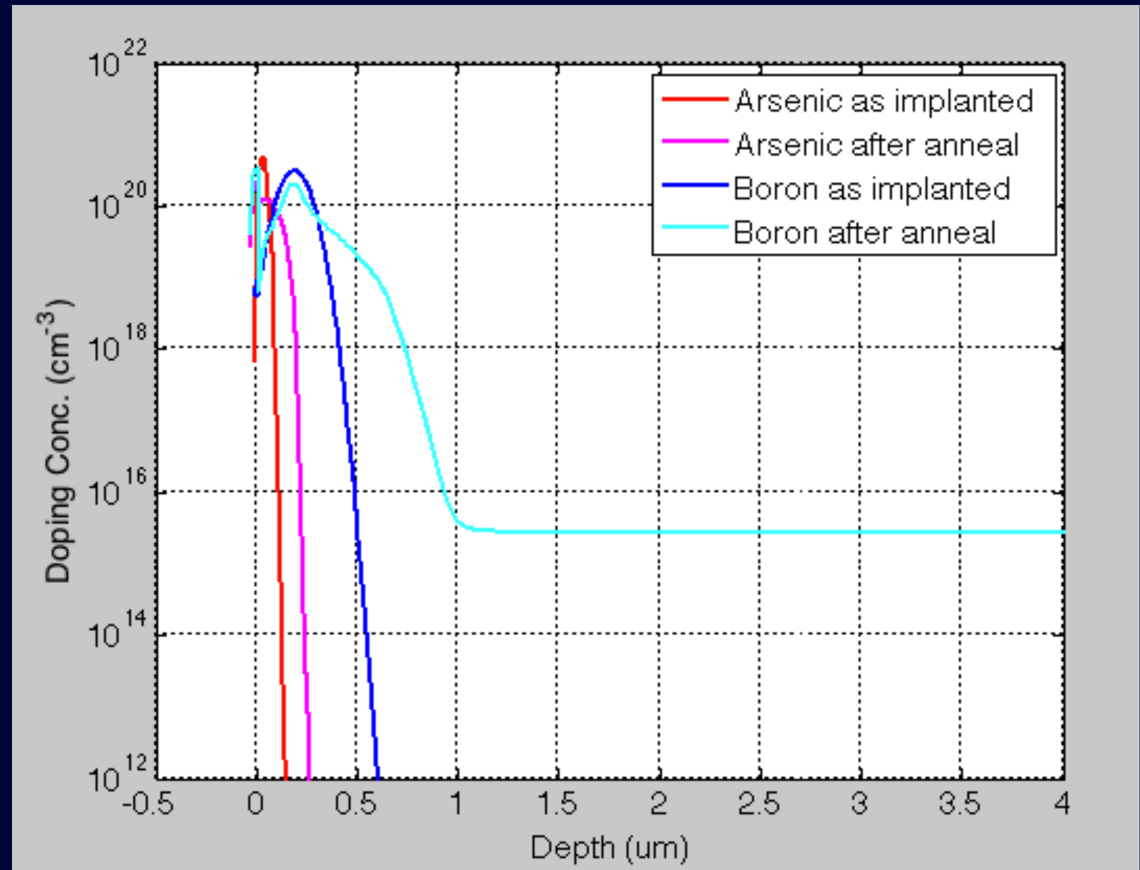
Isolation P+ implant

	Equipment	Purpose	Processing Details
1	YES Oven	prime wafers	
2	SVG Resist Coat	coat photoresist	Program 7 - PR 3612 1um w/o VP backside EBR only
3	ASML	expose	**wafers must be cleaned in SRD to minimize particle contamination in ASML* Mask: Jobfile: Exposure dose: 50
4	SVG Developer	bake and develop	(Initial bake) Developer 9 / Hot plate 1 (Develop + post bake) Developer 3 / Hot plate 1
Check developed region under microscope.			
5	Oven 110°C	harden the resist	Hard bake for 30 minutes
6	Drytek2	descum	**season chamber for 10 minutes* **make sure to use clean slots* Program 1 - pressure 150mTorr, oxygen flow 100sccm, power 250W (~0W reflected) for 40 seconds
7	Send out for Implantation	Isolation P+ implant	**The implantation is done outside of SNF* Boron 5e15 cm^{-2}, 60 keV, 7° tilt
8	gasonics	remove photoresist	Program 017
9	wbnonmetal	wafer cleaning	i. Piranha (9:1 H2SO4:H2O2) 120°C for 20 minutes ii. Water dump rinser iii. SRD
8	gasonics	remove photoresist	**Reason for performing a more thorough clean: It is difficult to clean the photoresist after implanting boron with high dose of 5e15 cm^{-2}. Therefore, we make sure by running the clean in gasonics once more.* Program 013

S/D N+ implant

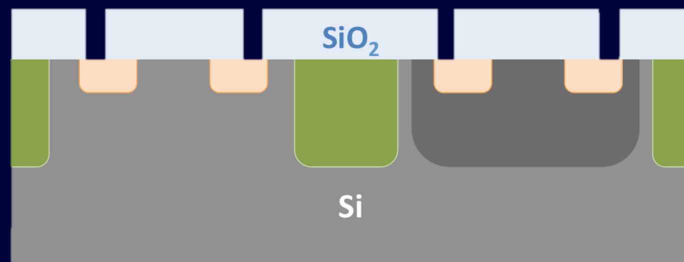
	Equipment	Purpose	Processing Details
1	YES Oven	prime wafers	
2	SVG Resist Coat	coat photoresist	Program 7 - PR 3612 1um w/o VP backside EBR only
3	ASML	expose	**wafers must be cleaned in SRD to minimize particle contamination in ASML* Mask: Jobfile: Exposure dose: 50
4	SVG Developer	bake and develop	(Initial bake) Developer 9 / Hot plate 1 (Develop + post bake) Developer 3 / Hot plate 1
Check developed region under microscope.			
5	Oven 110°C	harden the resist	Hard bake for 30 minutes
6	Drytek2	descum	**season chamber for 10 minutes* **make sure to use clean slots* Program 1 - pressure 150mTorr, oxygen flow 100sccm, power 250W (~0W reflected) for 40 seconds
7	Send out for Implantation	Source/Drain implant	**The implantation is done outside of SNF* Arsenic 2e15 cm^{-2}, 60 keV, 7° tilt
8	gasonics	remove photoresist	Program 017
9	wbnonmetal	wafer cleaning	i. Piranha (9:1 H2SO4:H2O2) 120°C for 20 minutes ii. Water dump rinser iii. SRD
10	gasonics	remove photoresist	**Reason for performing a more thorough clean: It is difficult to clean the photoresist after implanting boron with high dose of 5e15 cm^{-2}. Therefore, we make sure by running the clean in gasonics once more.* Program 013

Anneal



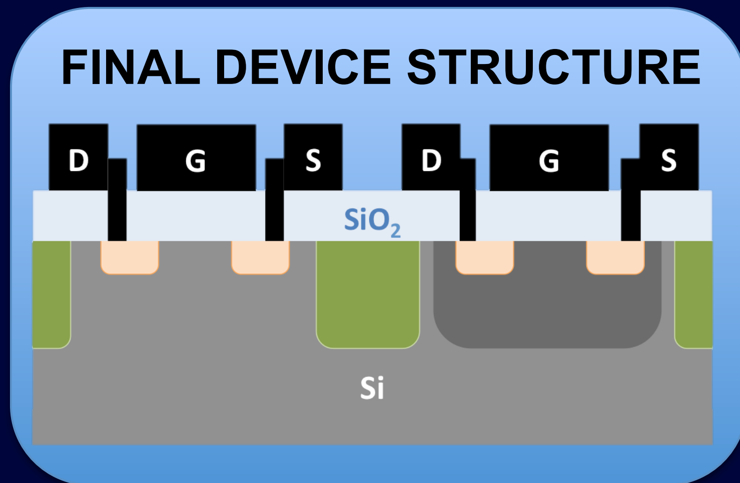
	Equipment	Purpose	Processing Details
1	RTA-L	drive-in & oxide heal	Anneal 15 seconds, 1050°C 10 Argon flow + 1 Oxygen flow

Etch Contact Hole



	Equipment	Purpose	Processing Details
1	YES Oven	prime wafers	
2	SVG Resist Coat	coat photoresist	Program 7 - PR 3612 1um w/o VP 2mm EBR
3	ASML	expose	**wafers must be cleaned in SRD to minimize particle contamination in ASML* Mask: Jobfile: Exposure dose: 50
4	SVG Developer	bake and develop	(Initial bake) Developer 9 / Hot plate 1 (Develop + post bake) Developer 3 / Hot plate 1
Check developed region under microscope.			
6	Drytek2	descum	**season chamber for 10 minutes* **make sure to use clean slots* Program 1 - pressure 150mTorr, oxygen flow 100sccm, power 250W (~0W reflected) for 40 seconds
8	P5000	etch contact holes	**make sure the conditions are correct. People make changes to the recipes.* Program surromed, 160 seconds, chamber B
9	wbnonmetal	wafer cleaning	i. Piranha (9:1 H2SO4:H2O2) 120°C for 20 minutes ii. Water dump rinser iii. 50:1 HF dip for 20 seconds iv. Water dump rinser v. SRD
Check etched region under microscope.			

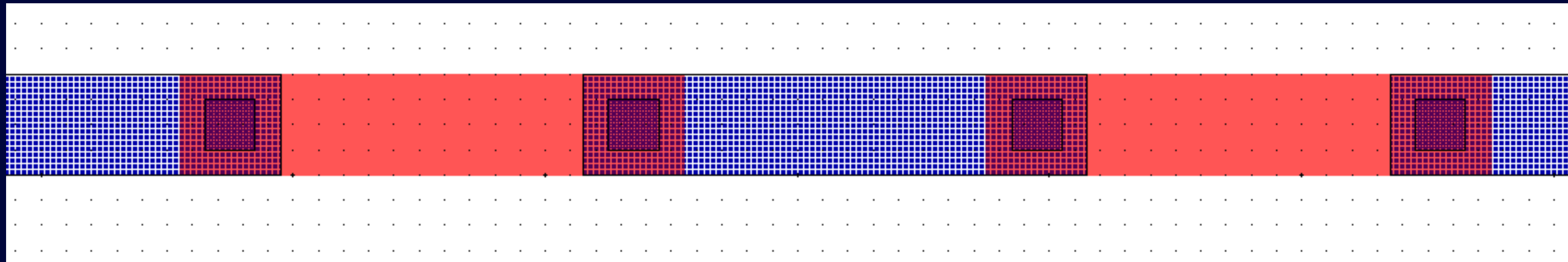
Metal Deposition



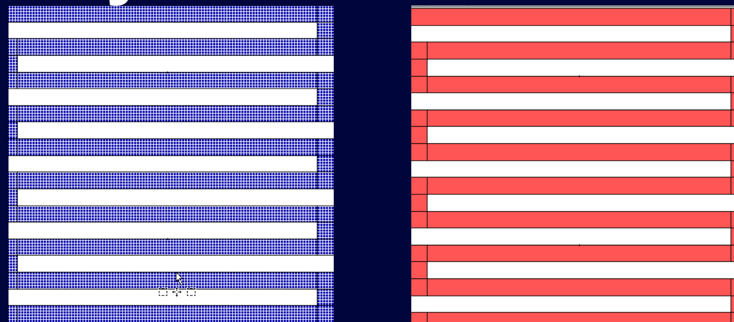
	Equipment	Purpose	Processing Details
1	Headway2	coat LOL2000	**use a filter to make sure the LOL2000 spun on the wafers is clean. Also, remove any large particles on the wafers using nitrogen blowgun.* 3000 rpm, 60 seconds
2	"White" oven	bake LOL2000	**This is a critical step, as the temperature determines the amount of undercut.* **"White" oven is actually green.* Load at 125°C, and after closing the door, set the temperature to 195°C. The total time the wafer is in the oven should be timed 23 minutes.
3	SVG Resist Coat	coat photoresist	Program 7 - PR 3612 1um w/o VP 2mm EBR
4	ASML	expose	**wafers must be cleaned in SRD to minimize particle contamination in ASML* Mask: Jobfile: Exposure dose: 50
5	SVG Developer	bake and develop	(Initial bake) Developer 9 / Hot plate 1 (Develop + post bake) Developer 5 / Hot plate 1 - Change program 5 steps 4 and 7 from 22 seconds to 21 seconds. (Don't forget to change it back!)
		Check developed region under microscope.	
6	Drytek2	descum	**season chamber for 10 minutes* Program 1 - pressure 150mTorr, oxygen flow 100sccm, power 250W (~0W reflected) for 40 seconds
7	Innotec	metal deposition	**right before loading wafers in Innotec, immerse the wafers in 50:1 HF dip for 30 seconds, followed by water bath, then hand-dry with nitrogen blowgun. This is to remove any oxide that was formed from the oxygen plasma (Drytek2).* 5 nm Titanium and 40 nm Platinum
8	wbsolvent	lift-off	i. Acetone: 5 minutes (with sonication) ii. Remover PG: 20 minutes iii. IPA: 5 minutes iv. Blowdry with nitrogen gun
		Check metal lift-off under microscope.	
9	RTA-R	anneal defects	Anneal 10 minutes, 350°C, 10 forming gas flow
		Measure!	

Test Structures

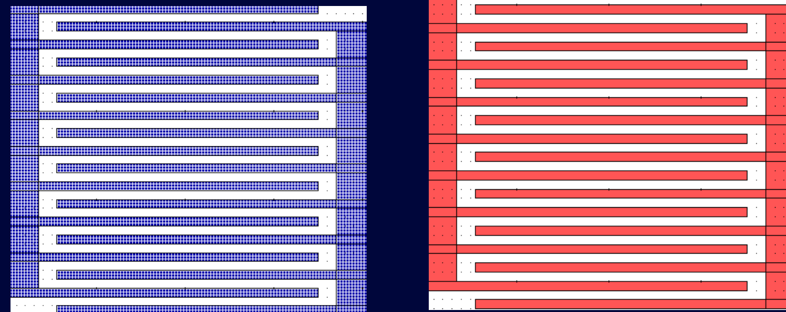
- **Contact chains (M1-M2)**



- **Continuity Structures**

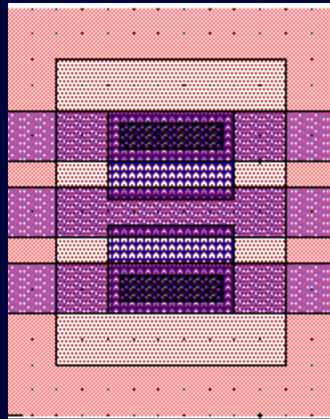


- **Isolation Structures**

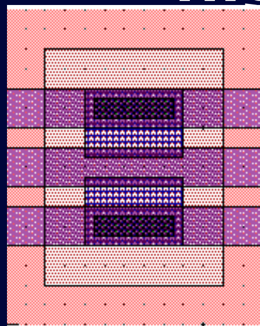
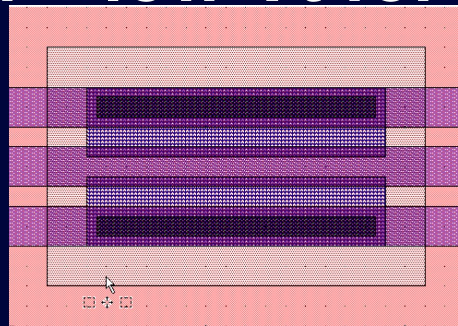
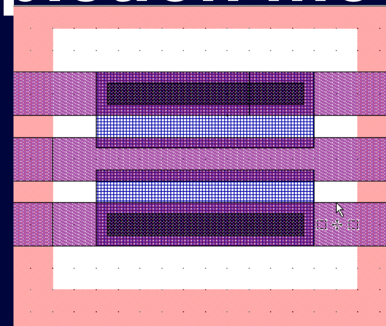


Transistor Sweep

- Transistor standard cell

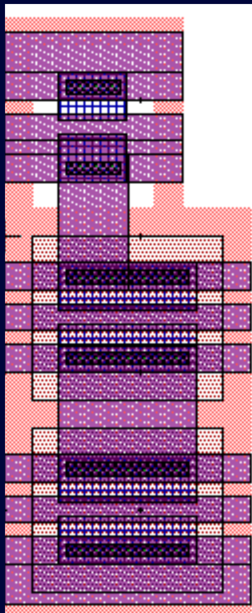
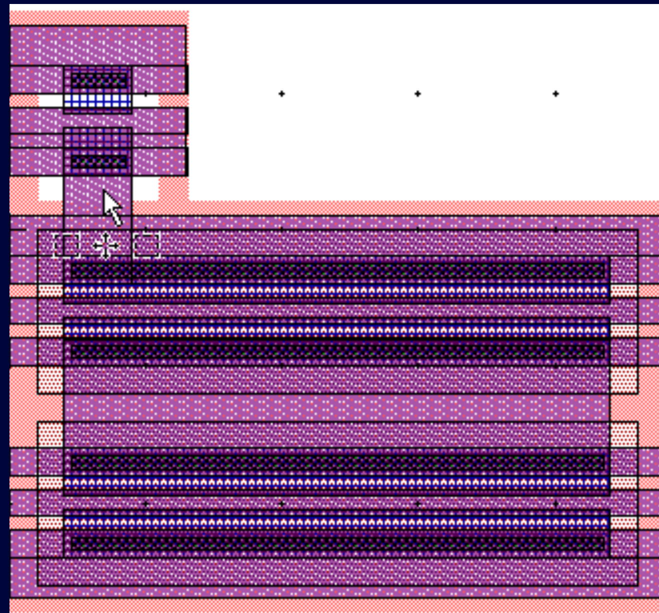
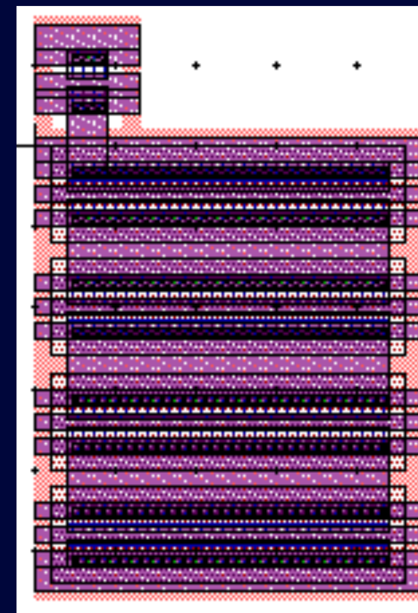


- Sweep sizing + doping
  - high + low Vt for depletion mode logic

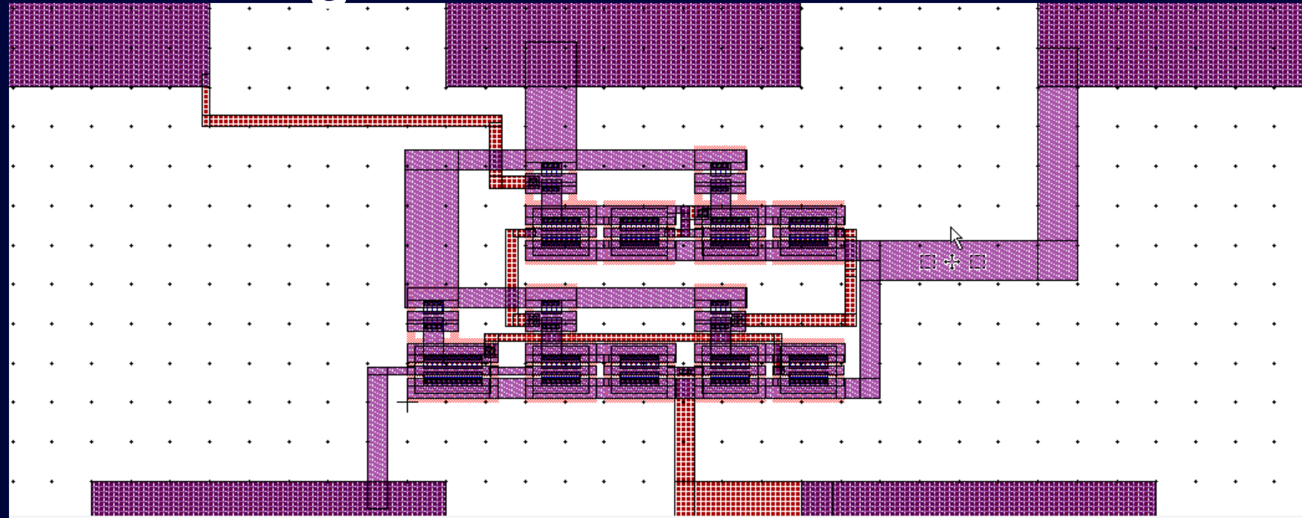
Logic

- Inverters, NANDs, NORs, etc.
  - Sweep sizing + fanin

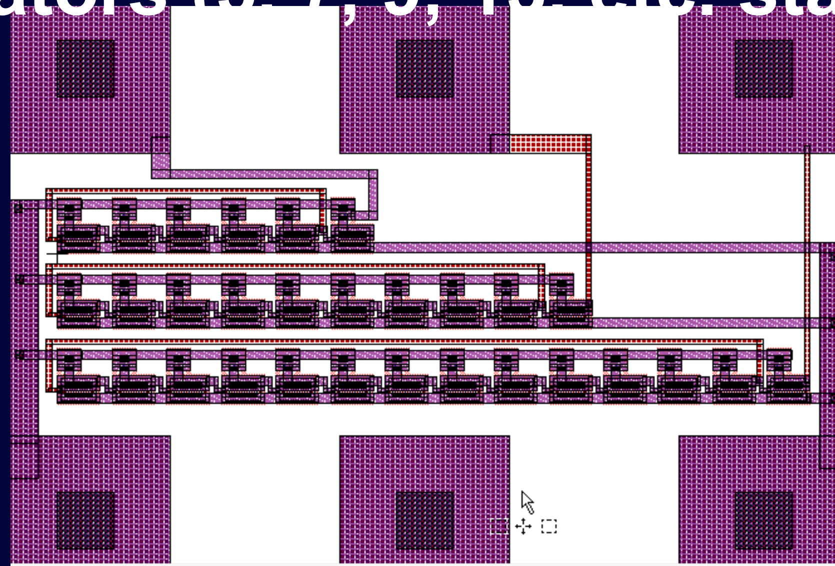




Complex Logic

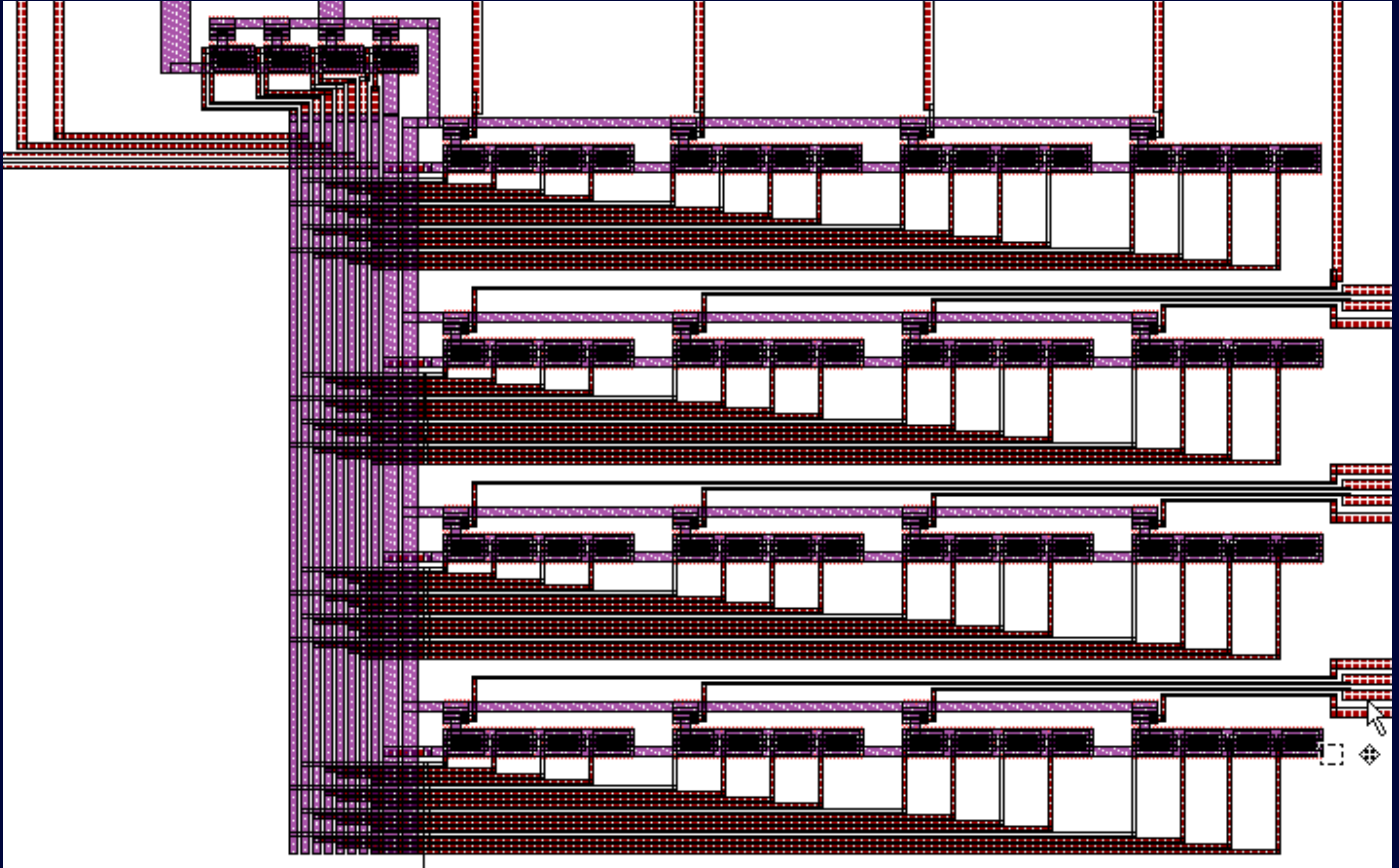
- **Sequential logic: dlatch**



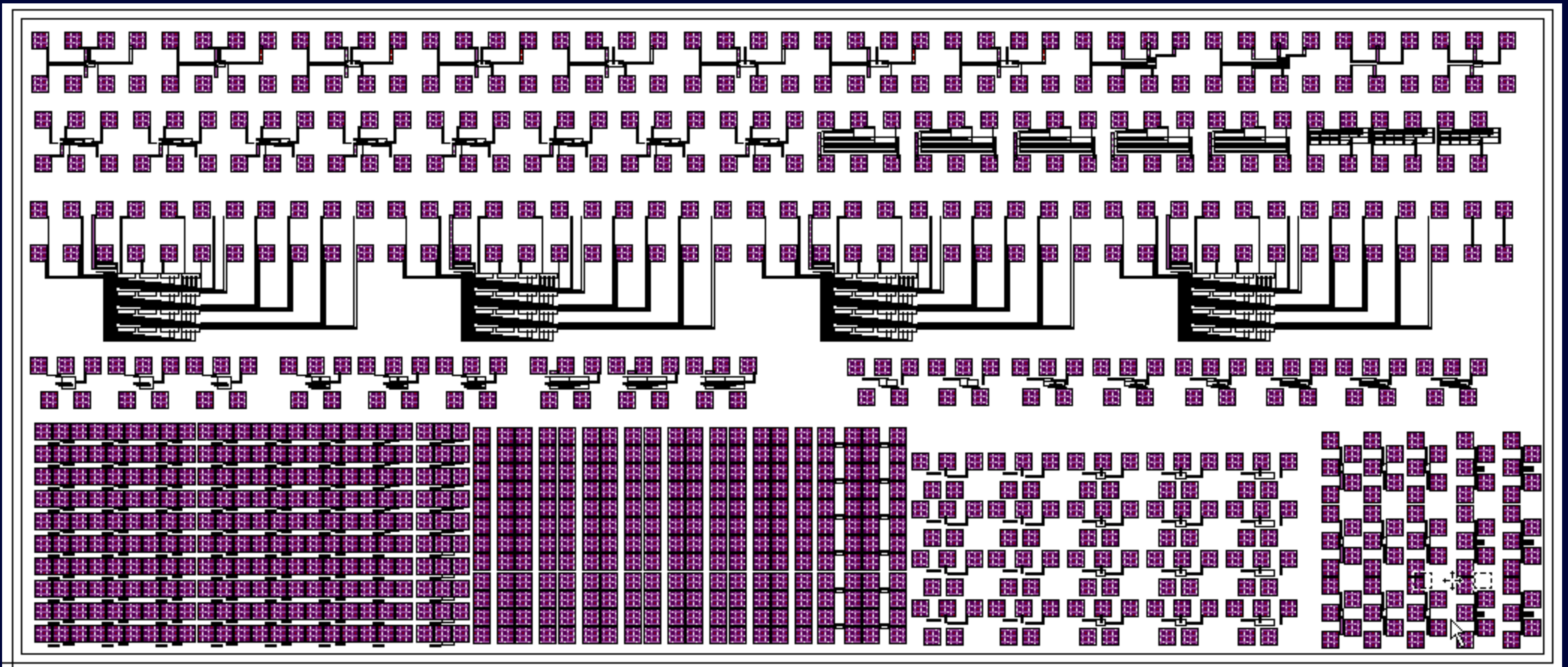
- **Ring oscillators (5, 7, 9, 13, etc. stages)**



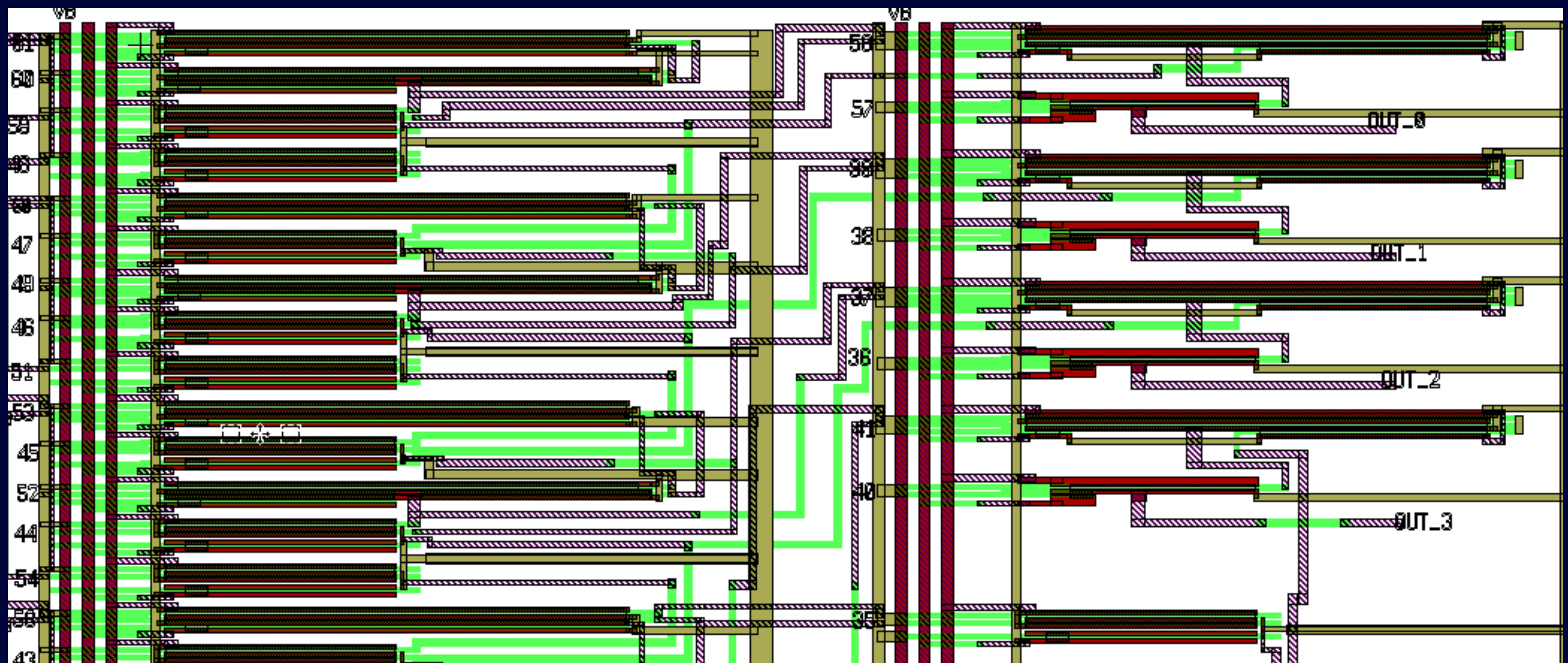
Decoder



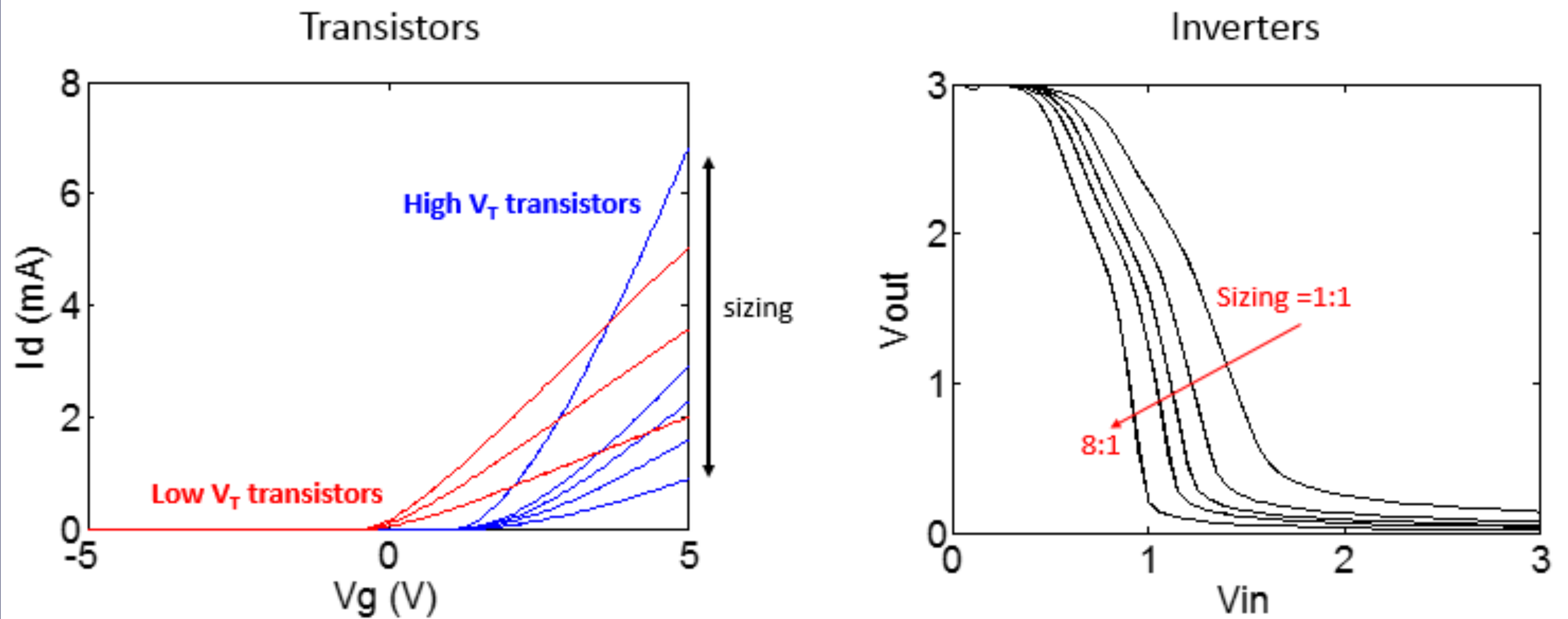
Full Layout



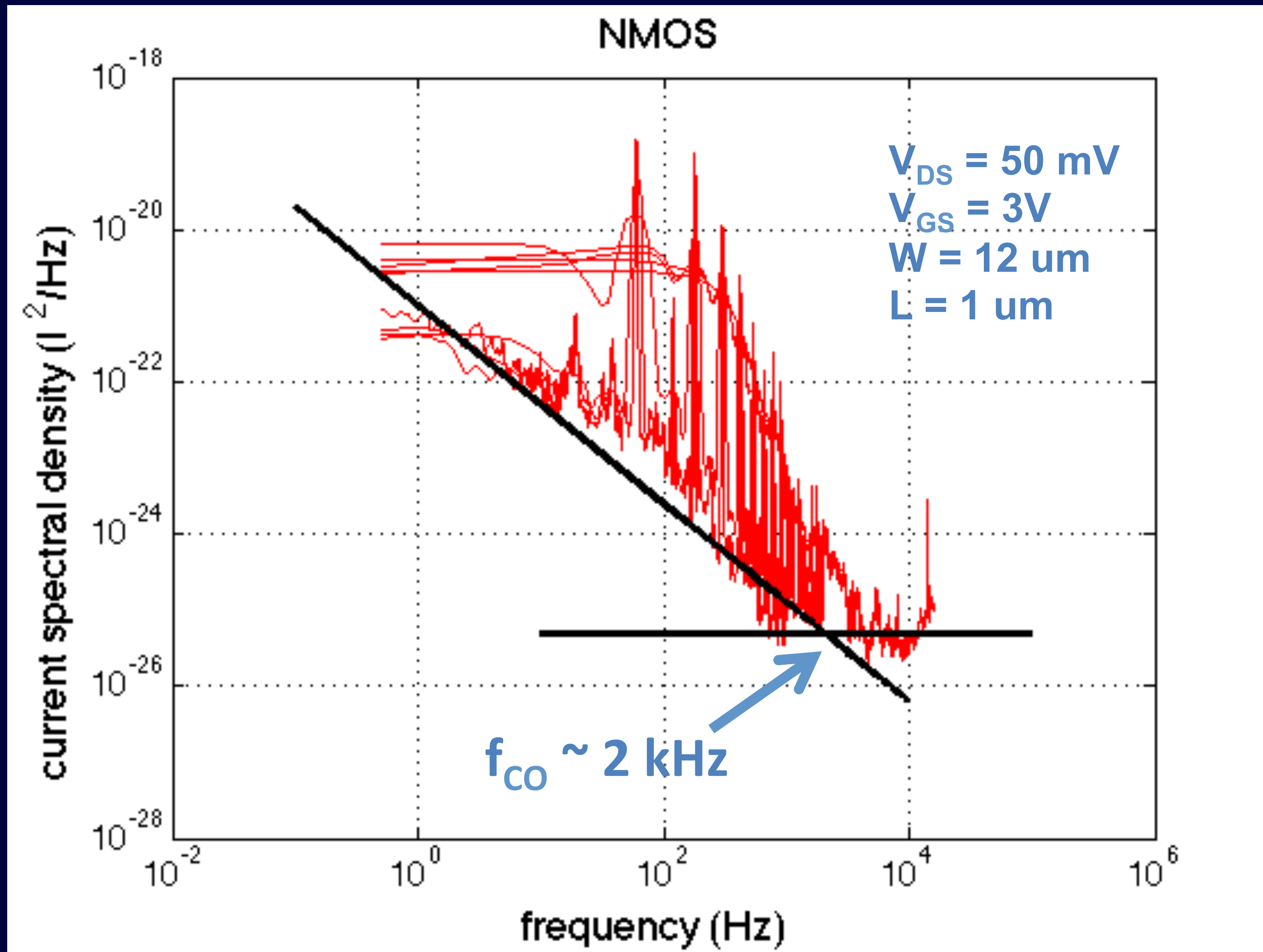
Example Standard Cell Design



Sample Experimental Results



1/f noise measurement



1/f noise measurement

$$f_{co} = \frac{K_f}{4kT\gamma} \frac{1}{C_{ox}} \frac{g_m}{W \cdot L}$$

$\rightarrow$ **$K_f \sim 0.365 \times 10^{-25}\ V^2F$**

$f_{CO} \sim 2$ kHz
$g_m \sim 8.7087e\text{-}06$ S
$T \sim 300$ K
$k \sim 1.38e\text{-}23$ J/K
$C_{ox} \sim 0.0012\ F/m^2$
$\Upsilon \sim 2/3$
$W \sim 12$ um
$L \sim 1$ um