# TESTCHIP SNF410:

## AN OPTIONAL PWELL ADDER TO DEPLETION NMOS FLOW (EE312)

by

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# SECTION 1: INTRODUCTION

The testchip "SNF410" was developed with the purpose of enhancing the DEPLETION NMOS process flow for EE312 testchip by adding a Pwell. The initial motivation was to enhance and/or fix the functionality of some test structures which were lacking a low resistance ground path through using a top side substrate connection.

The project was first advised by Usha R. to provide some calibration silicon for CV measurement on 300A oxide and also for a general improvement of performance by providing a well to the core process. Later on, a group of "free devices" (which could be available with Pwell) were added to the list.

This test chip used two ASML reticles: SNF410 A001 & SNF410 B001. In addition to the enhanced flow, the reticles also provided Metal 1 Etching mask & Solder Bump mask for Flip Chip bonding process.

The following Figure 1 shows an overview of the SNF410 Mask layout. The top part ("Module 1") is copy over of the testchip EE312, designed by Max Shulaker & Rebecca Park for Dr. Roger Howe. The bottom part ("Module 2") was designed by the author of the report. A more detailed figure introducing the structures in Module 2 is included in the next page. It is pointed out that this report mainly focused on the Module 2 devices (except where necessary to refer back to Module 1 devices) and talked about the trade-offs of original process and possible methods of improvements. Readers are highly encouraged to read about the original works [1], [2], and [3], prior to reading this report.

Fig 1: Overview of the Testchip SNF410:

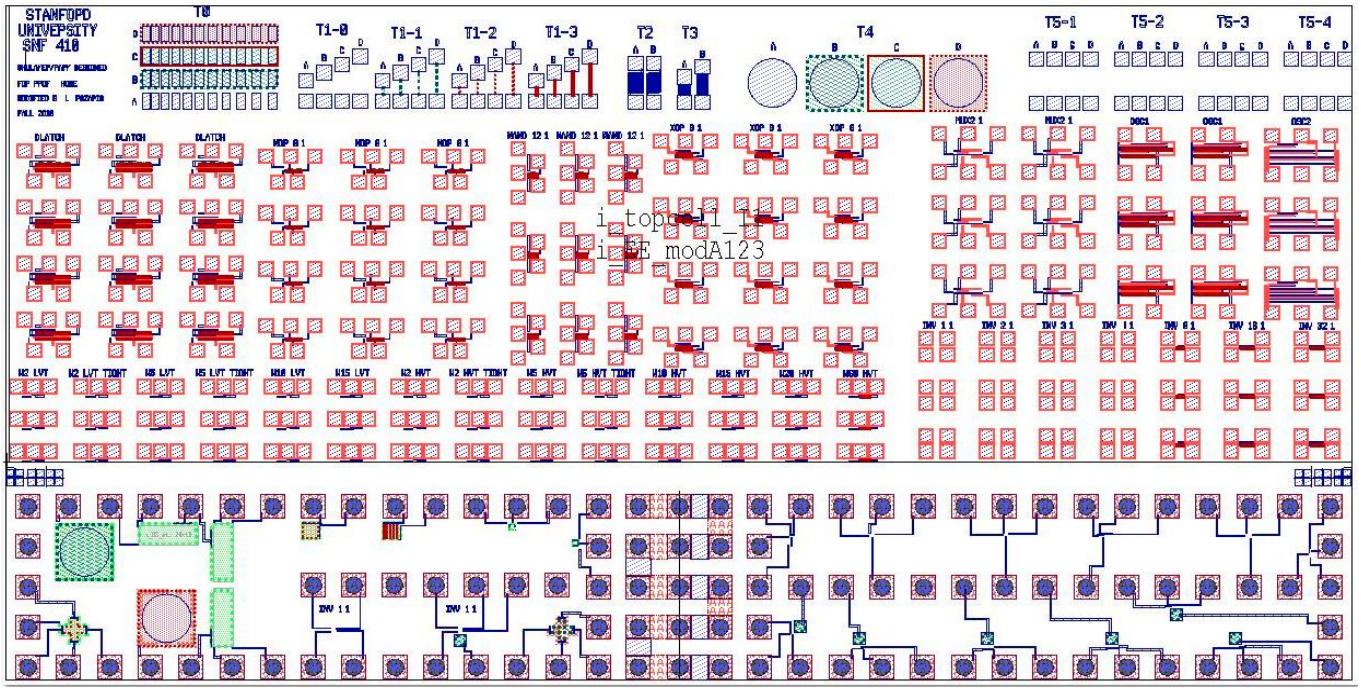
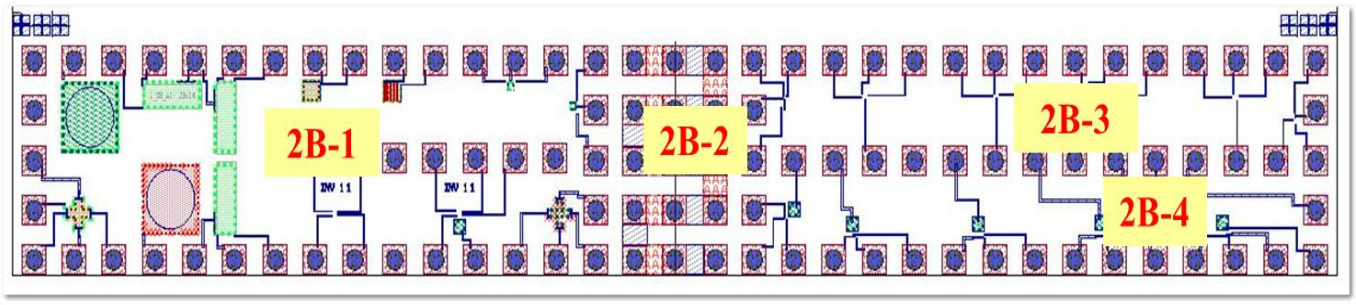


Fig. 2 shows an overview of Module 2 structures. Individual details of these structures, and measurement results were discussed in Section 3 & Appendix E of this report. Some more new devices that could have been introduced to this modified process are discussed at the end of this section 3. Initially the real estate area in the design was used up carefully so that all the necessary masks could be fitted within two reticles. However, when the ASML reticle file was being worked out, it was realized that Module 2 had more room to increase in Y-direction.




A1. Capacitors
A2. Contact Chains
A3. Diodes
A4. LNPN
A5. VDPs
A6. Inverters

**2B-1**

B. Daisy Chain for Flip Chip Bonding

**2B-2**

C1. LVT (w=2, 5, 10um), Configuration 1
C2: HVT (w=2, 5, 10um), Config 1

**2B-3**

D1: LVT, Configuration 2
D2: HVT, Config 2

**2B-4**

It might be worth mentioning that the whole of EE312 reticle is retained as a part of SNF410 reticle as Module 1. Module 2 Test structures are newly added devices and test structures. The original EE312 reticle has process characterization test structures (resistors, bridging, serpentines, MOS capacitors and contact chain), transistors (LVT & HVT), digital gates (NAND, NOR, XOR, D-Latch, Multiplexer, Inverter, Ring Oscillator), Decoder and

Amplifier. The SNF410 reticle Module 1 had retained all these test structures and circuit blocks without any modification. The layout database was extracted from mask shop as a gds file, streamed in and instantiated. Therefore, this part of test structure would give same results as EE312 reticle set with standard process flow or with pwell option.

Module 2 offers new test structures (van der pauw sheet rho, three contact chains), devices (diode, lateral NPN-bipolar) and MOS transistors with layout modification for p-substrate connection from front side. Module 2 also offers two Inverter circuits with layout modification to improve performance.

Whether it is reported here or not, all the process characterization test structures and most size transistors from EE312 reference silicon from last year (Winter, 2016) had been tested prior to starting layout works of the SNF410 test chip. This was done in order to understand the performance, capability, and limitations of the original depletion-load nmos process. Module 2 test structures were made in order to improve the performance and overcome the limitations of the original test structures with the added Pwell. All the new structures and devices in Module 2, except the inverters, had been tested in SNF410 silicon. This also includes the flip chip bonding capability, using the Module 2 pad frame and Indium bump bonds with a Finetech Lambda flip chip bonder.

The Logic gates of EE312 are connected using metal2 and via. SNF410 reticle has metal2 and Via masks, however, current EE312 & SNF410 both run-sheet has unit process developed upto metal 1. All the individual transistors and process characterization test structures are testable at metal 1 for both EE312 & SNF410. If in next batches of silicon, the process is developed upto metal2 and the wafers are pulled after metal 2, then most of these logic gates could be tested in a standard digital logic test lab; The logic gates or circuit blocks need to be wire-bonded and mounted on printed circuit boards. However, it might be worth noting that the yield of the very wide transistors in EE312 is poor due to gate oxide integrity problem (discussed in details in section 3A). This problem coupled with the lack of stable ground reference (in absence of a pwell tap and vertical isolation) may make logic gates with large fan-in and fan-outs perform poorly for maintaining stable logic zero reference and noise margin. For these reasons, the Module 2 test structure included 2 versions of Inverter layouts with ground connection and improved parasitic. The performance comparatives remain to be tested in digital logic lab. Once the functionality of a logic level and its inverted level can be demonstrated using an inverter, basically all other logic circuits would be functionally okay.

It is understood that although the yield of the logic gates may be poor, however, successful operation of circuit level has been demonstrated by Max Shulaker for his research works using the original depletion nmos process. Therefore, with suggested improvements in the process flow and device layouts, the success is guaranteed for circuit functionality

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## SECTION 2: ADVANTAGES OF THE DEPLETION NMOS FLOW (EE312)

As was pointed out by Ref [1], the EE312 depletion nmos flow greatly simplifies the fabrication process. Within the limited timeline of a quarter, the students get a hands-on experience on most of the clean room processes and electrical characterization method. This process uses only 5 photolithographic layers, 3 implantation layers, 1 furnace oxidation layer and 1 metal deposition layer. With a few processing steps (compared to conventional cmos steps), the process allows depletion and enhancement nmos devices. Using this depletion nmos logic, different logic gates could be made and demonstrated successfully.

There are some reasonable trade-offs made to achieve these great advantages. Section 3 of this report discussed these observations in detail. During the course of characterization of the silicon, it was realized that the performance of the original process and the number of supported devices would be greatly enhanced by adding a Pwell to the flow. Furthermore, there will be scope for adding more devices in future. This would also allow the flow to be used in simple analog circuit design domain, as well as currently demonstrated digital logic domain.

The process flow simulation necessary for the unit processes related to Pwell is given in Appendix A. As is pointed out in the simulation codes, the Pwell implant and drive-in occurs through its own 750 Ang wet oxide, which is sacrificed prior to growing the 300 Ang dry oxide required by the original flow. Therefore, the Pwell implant and drive-in do not affect the thermal budget of the core flow. The 750 Ang Pad oxide becomes a sacrificial oxide for 300 Ang oxide. Therefore, the comparatively higher energy Pwell implant does not affect the quality and reliability of the 300 Ang oxide. Also the Pwell drive in can be independently controlled. This can be further optimized to get a better performance lateral bipolar (N+/pwell/N+) in future.

In short, the depletion nmos process flow offers a gamut of devices and logic blocks for demonstrating digital logics and simple amplifiers. With addition of pwell, additional analog capabilities can be pursued. Therefore, the process could be considered for quick turn-around, very simple, low budget flow for demonstration of new device or circuit concepts with modest yield. Additional performance could be bought with introduction of Locos isolation and active mask in the process.

# SECTION 3: MEASUREMENT RESULTS & DISCUSSIONS

## Section 3A: Gate Oxide Integrity

The gate oxide was tested with Fowler-Nordheim (F/N) tunneling current, with bi-directional sweep to make sure both accumulation and inversion domain show low leakage. Where possible, multiple sweeps have been applied to make sure the oxide can sustain repeated F/N stress before rupture. Many sites were tested around the wafers from 2 batches out of clean room.

**Fig. 10** shows F/N tunneling curve in large MOS Cap without any contact in the vicinity of the MOS structure has Vbd=30V, as expected for this gate oxide thickness. This cap uses the backside of the chuck as substrate connection. For a 300 Ang Oxide, this 30V rupture voltage indicates a 10 MV/cm rupture field. For a circular area of 70,686 $um^2$ (radius = 150 um) MOS structure, this rupture voltage Vbd shows that the gate oxide quality is pretty good, as evidenced by large intrinsic size of the measured oxide area relative to nominal test structures (Typical intrinsic structure dimensions = 100 um*100 um = 10,000 $um^2$).

However, for a same MOS structure with a couple of minimum sized contacts in close vicinity to the above-mentioned structure (within ~10 to 20 um), the Vbd reduces to 15V. For actual MOSFETs with very small intrinsic sized gate oxide area, the Vbd numbers are all over, from 0V to about 20V; this is indicative of various defect dominated extrinsic breakdown mechanisms. **Fig 11** shows the F/N tunneling data for a MOS device and **Fig. 12A & B** gives the statistical distribution of measured data. The most probable reasons for this progressive degradation in Vbd data on MOSFET devices are discussed in the next paragraphs.

Within the VDD=VGG=5.0V domain, 8 out of 10 transistors work for upto width of 15 um. The widest HVT transistor (W=60um) show GOI short on 10 out of tested 10 devices. So, a maximum of 5V (**VDD = VGG < or = 5V**) is recommended for testing/ using these devices for future applications. All studies in this report are also restricted to a max Vdd of 5V for the same reason.

As was pointed out earlier, this process is a very short students' demo version to enable fast turn-around for producing functional transistors and small devices for easy understanding, testing and integration. The main trade off is the gate oxide breakdown voltage compared to CMOS devices with similar gate oxide thickness.

**Fig 10**: F/N Tunneling current of gate oxide in MOS without any contacts in vicinity: shows gate oxide rupture at 30V.

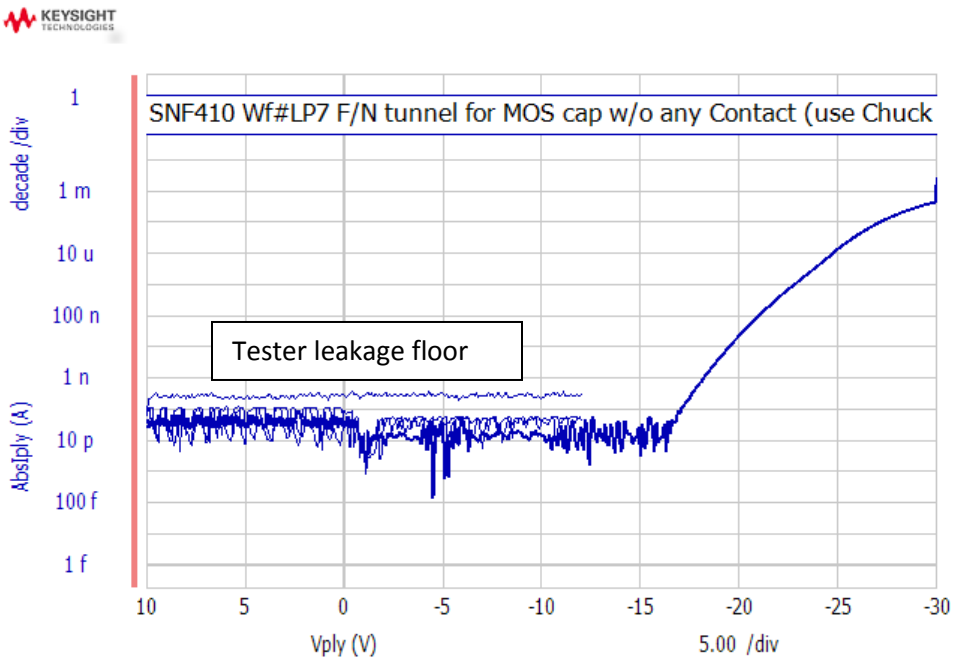



**Fig 11**: F/N Tunneling current of gate oxide in MOSFET, Width=2 um: gate oxide ruptures at 8V.

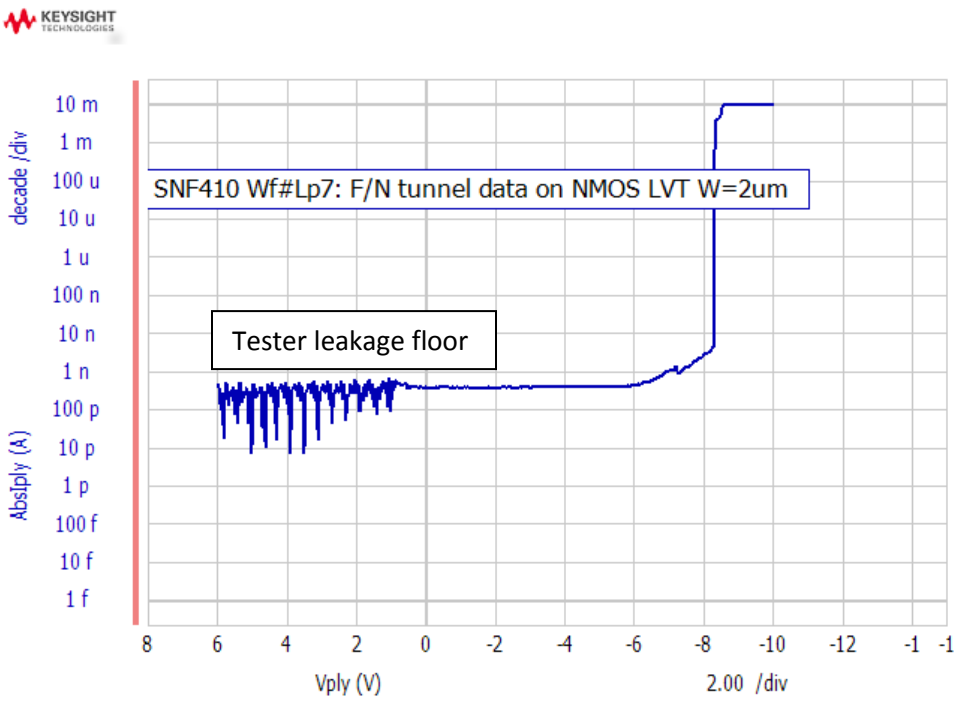


**Fig. 12A**: Statistical data showing the distribution of Breakdown Voltage VBD on various MOS structure & MOSFETs.: Note Intrinsic Vbd 30V vs. MOSFET gate to Drain (or Source) Vbd shows wide variability from 0V to 20V.

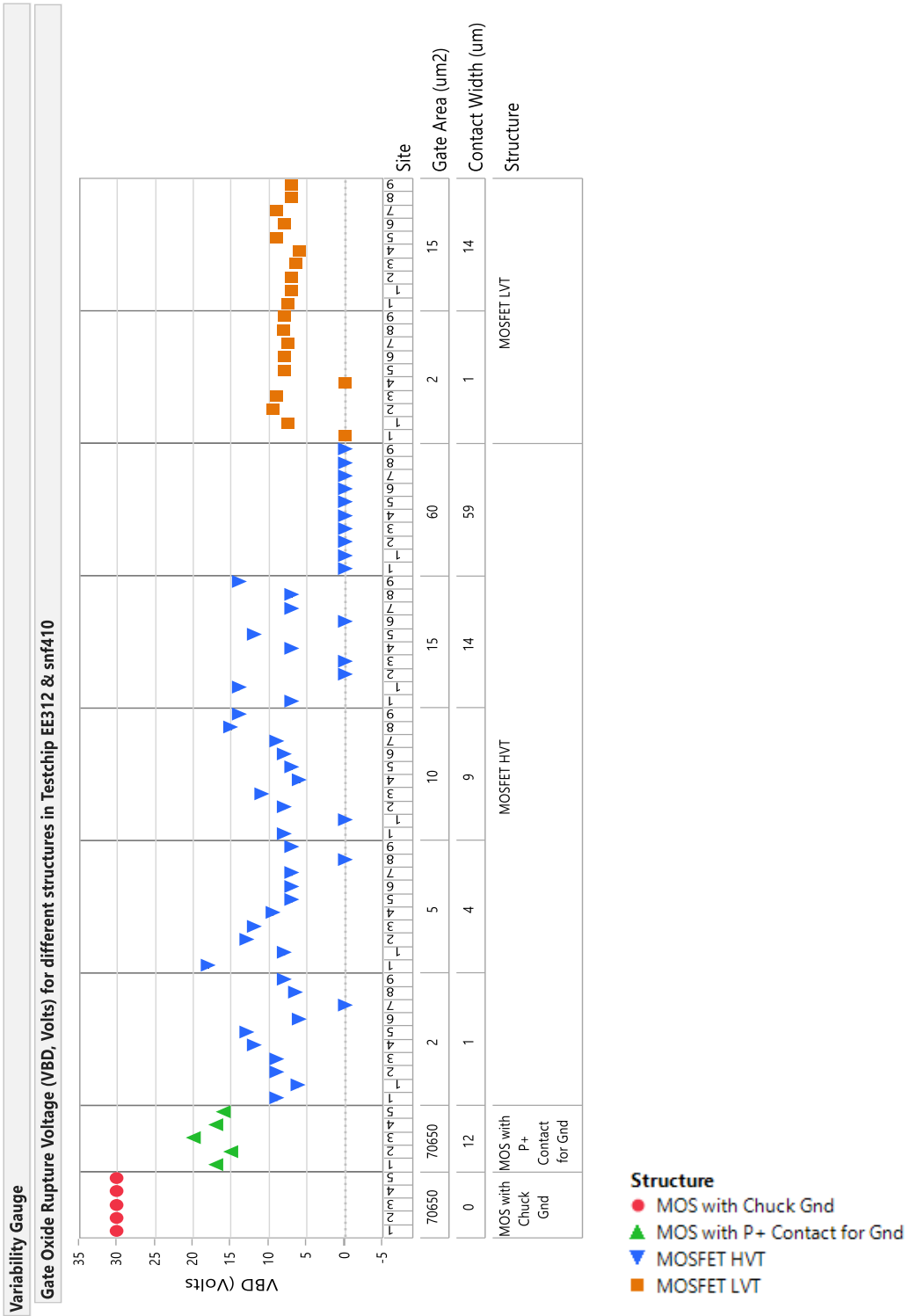
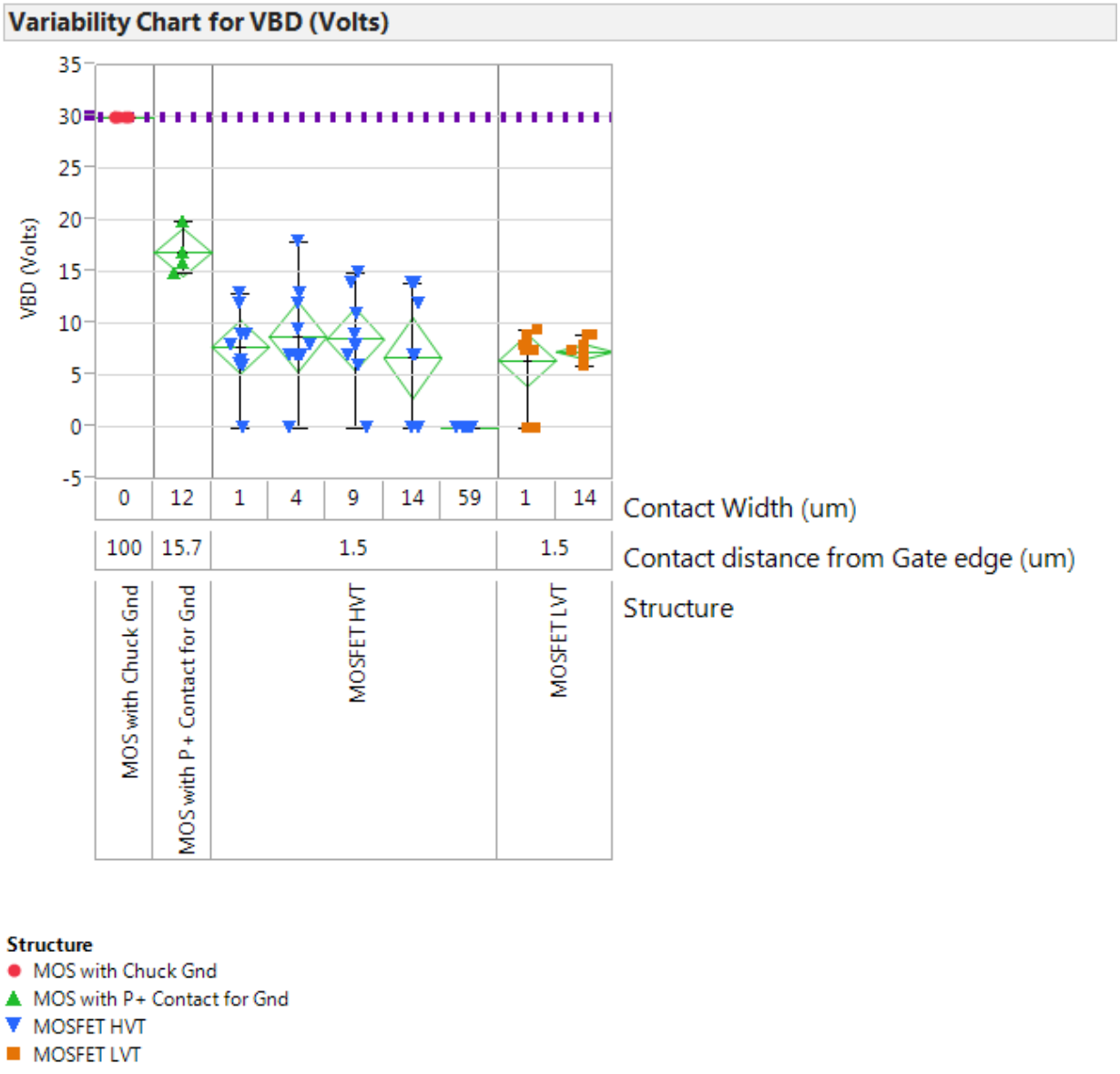


**Fig. 12B**: Variability Gauge analysis of the statistical data presented in Fig. 12A.

This plot shows that the contact distance from the gate edge is the strongest contributor to low rupture voltage and its variation. The MOS with chuck ground structure does not have any contact in its vicinity, we are using a distance of 100 um (arbitrary) to be able to put the data on chart. Contact width is the next contributor in VBD variation. The chart shows, wider the contact, more failure of transistors with 0v VBD. The 60um wide HVT virtually shows no yield within the tested samples. The possible causes of the failure mechanism is discussed in the remaining part of this section.



The advantages of the EE312 depletion nmos flow is that the number of masks and processing steps are greatly reduced compared to a generic CMOS or BiCMOS flow. By using only 3 Implant layers (N+, P+, HVT) and 5 Masks (N+, P+, HVT, CONTACT, METAL), this process is offering functional NMOS, and a mini-standard cell library containing logic gates (INVERTER, NAND, NOR, D-LATCH, X-OR, MULTIPLEXERS) and AMPLIFIER. So, one can build small logic circuits or processors using these building blocks with a reasonable yield. The process flow has been greatly simplified to keep it short and allow the students to have more hands-on experience in different Areas in a clean room (Lithography, Diffusion, Deposition & Etch). The simplified steps are as stated below:

1. The 300 Ang thick "gate oxide" is also supposed to work as "Field Oxide" for device lateral isolation, instead of LOCOS or Shallow Trench Isolation.
2. Gate metal and interconnect metal are the same and hence there is no need for a separate ILD/IMD layer.

However, all the above-mentioned advantages lead to some limitations and trade-offs as described below.

1. In this process flow, no sacrificial oxide is used for implants. Dopants are implanted through gate oxide and resist is spun over gate oxide for implant masking causing potential defects/ damage.
2. Annealing may not be sufficient to remove the implant damage.
3. The production of defect states in the oxide of MOS capacitors during the electron-beam metallization process producing trapped holes & related threshold voltage instability has been reported in literature. The process may experience this defect causing mechanism.
4. It is to be noted that contacts to usual CMOS gates should be sufficiently spaced away from active device area, which is not the case for here.

Therefore, this "gate oxide" for MOS devices in this flow is subjected to contact plasma etch, HF dip (to get rid of contact etch related polymers) within the device active area. Moreover, the Pt Lift-off process requires that there is LOL2000 layer coated on "gate oxide". Based on the visual observations made in the two batches of silicon, it was noted that the LOL adhesion to oxide is not consistent throughout the film. Around large contact openings, the HF dips create rounded corner features, which affects the LOL adhesion to oxide near contact areas. Based on the visual observations, it is seen that very wide transistors show "S-shape" gate, rather than straight gate features (i.e, gate metallization which is parallel to Source/Drain contact area) after photoresist film develops. This is a manifestation of rounded corner contact opening features resulting from HF dip, causing a lack of adhesion of LOL to substrate. It is possible, that during Innotec metal evaporation of contact and metal (at the same step), the evaporated metal produce a "bird's beak" type feature around contacts underneath the gate oxide. It is also possible that gate metallization

is shorting the gate to contact fill areas in Source/Drain by not staying parallel to etched areas in Source/Drain diffusion region. Measured data show that there are many gate oxide shorts at less than 1.0v, with characteristics similar to stringer type resistive short, which may support the comment above. A dual beam progressive FIB cross section may be very useful in this case. Multiple circular contacts connected using a "comb-type" metal connectivity approaching from the outside of the Source/Drain can be used instead of a single slotted wide rectangular contact to minimize collapse/ shorts during LOL processing. Fig 13 captures a group of devices, layout versus in silicon (microscope picture) to show the "S-shape" gates in wide devices and logic gates.

**Fig. 13A:** A MOSFET HV gate width=2um (contact width= 1 um). Microscope picture show the transistor gate is straight, and parallel to source & drain metallizations.

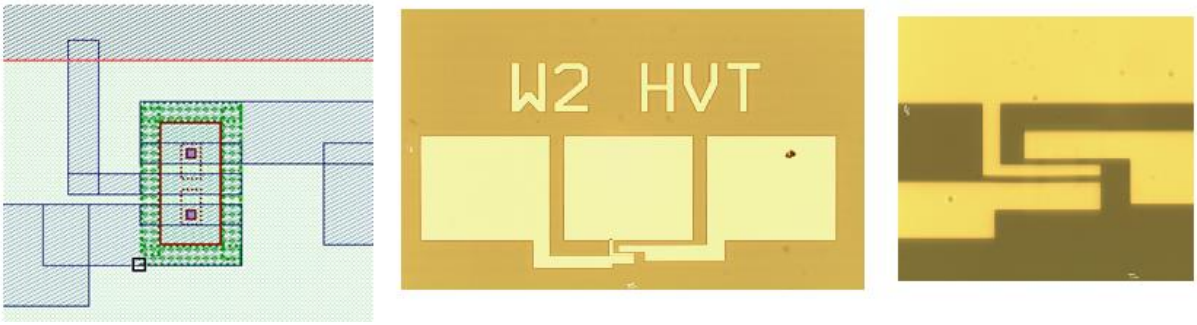



**Fig. 13B:** A MOSFET HV gate width=60um (contact width= 59 um). The layout show straight features on gate & S/D metals; microscope picture show the transistor have "S-shape" gate. This effect becomes progressively worse, starting around Width=15 um.

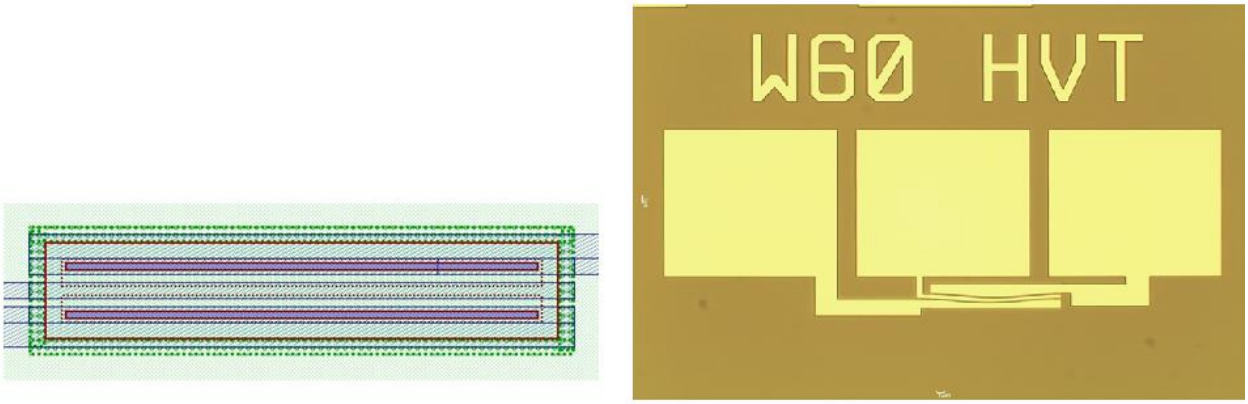


**Fig. 13C:** show a Logic gate (NAND 12:1), the layout versus as it appears on silicon. The contrast in metal gate features on top block versus the bottom block on silicon is very clear.

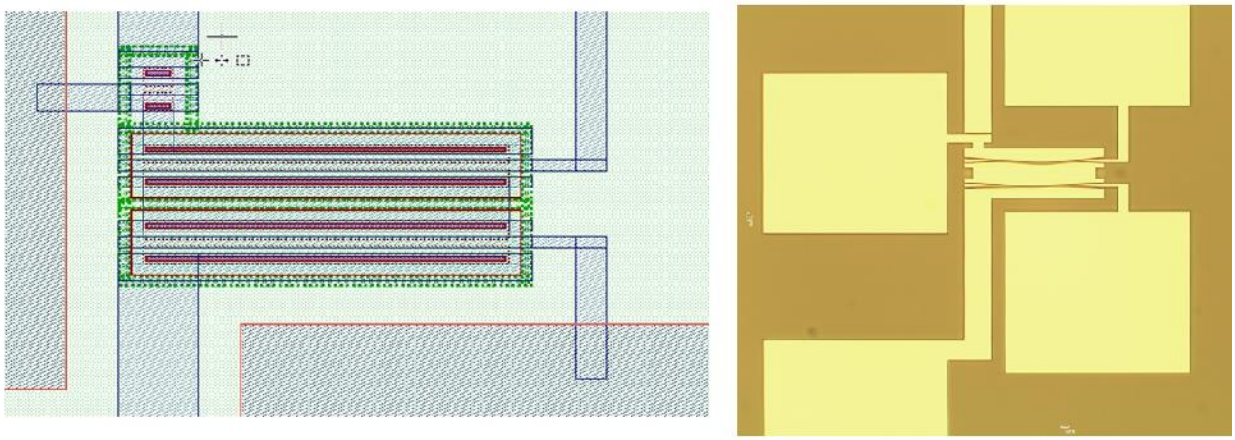
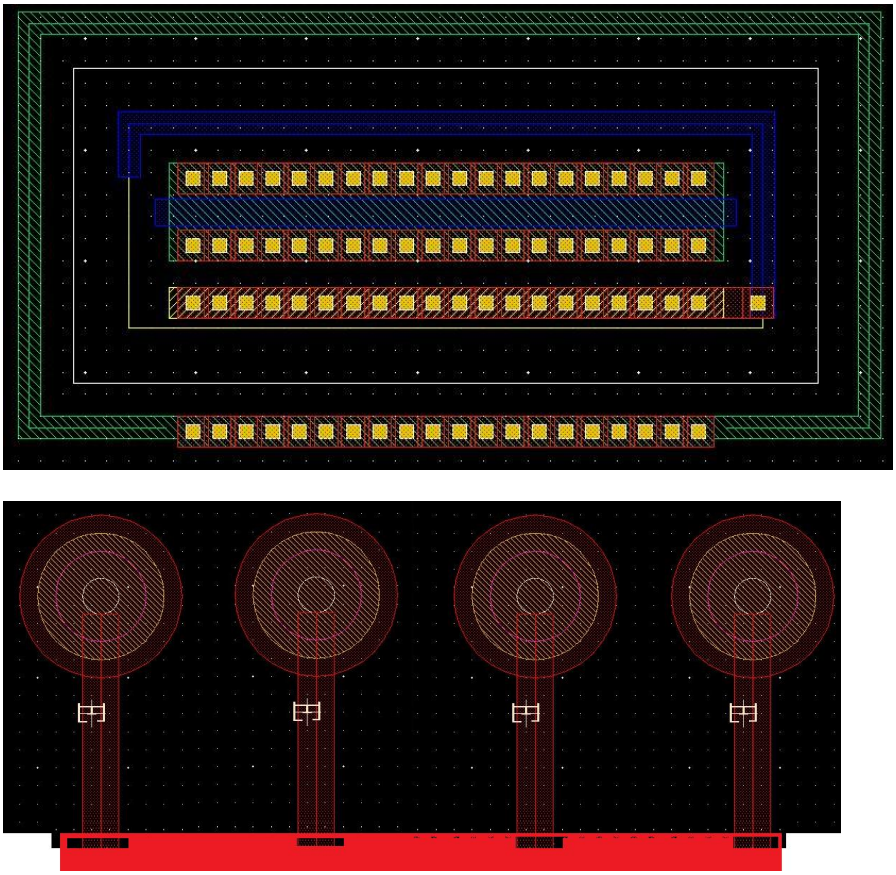


**Fig. 13D:** show a generic MOSFET layout, with an array of contacts to cover the width. Multiple circular contacts connected using a "comb-type" metal connectivity approaching from the outside of the Source/Drain is shown.



A possible improvement in gate oxide quality may be possible by using an Aluminum backend process. This process will evaporate a blanket metal film on gate oxide, then coat this with photo-resist and use Aluminum dry etch using PT-MTL or P5000. So, the process will avoid the uniformity in LOL film adhesion to oxide, and may stop the metal shorts. The mask exist for this process in the reticle, and some snf410 wafers were held in-line to be used for the unit process developments on Aluminum backend.

## Section 3B: NMOS LVT (native) & HVT (w/ threshold implants)

Details of the device physics & processing of the NMOS LVT3T & HVT3T is discussed elsewhere [1], [2], [3]. In this report only the measured data from original NMOS LVT (LVT3T) & HVT (HVT3T) is presented. These transistors have three terminals (3T: Source, Gate, Drain).

The NMOS4T with Body terminal (using Pwell & P+ as substrate pick up) was newly introduced in Snf410 testchip per suggestions from Dr. Roger Howe. There were two layout styles used: one that uses the P-isolation ring as body tap, and another using an external Ground pad. Both type layouts are functional, as have been measured on Snf410 silicon. In this report only the data with P-isolation ring as body tap is presented. With the availability of a body contact, the ground reference for transistor becomes local, rather than using Chuck as ground. Body biasing is often used to change threshold voltage of transistors, a technique widely used by circuit designers.

**Fig. 14** shows the transistor layout with P-isolation ring used as body tap (both in LVT & HVT). These layouts have less overhang of metal in source, drain & gate area compared to original 3-terminal layouts. **Fig 15** shows using a local ground pad in the vicinity to create a ground reference for the transistors. Note, for all these measurements, Chuck was connected to source using a T-connector and forced to ground using GNDU (Ground Unit), which is a passive ground, rather than using a SMU force 0V active ground. Using a passive ground instead of an active ground (SMU Force with feedback circuits) often takes out oscillations from measurements.

**Fig 14**: Transistor layout using P-isolation ring as body tap. Color code for layout reading: Green perimeter= P-isolation implant; Blue represents metal routing; Pink rectangles= S/D implant (n+), blue blocks with red outline= contact drawing.

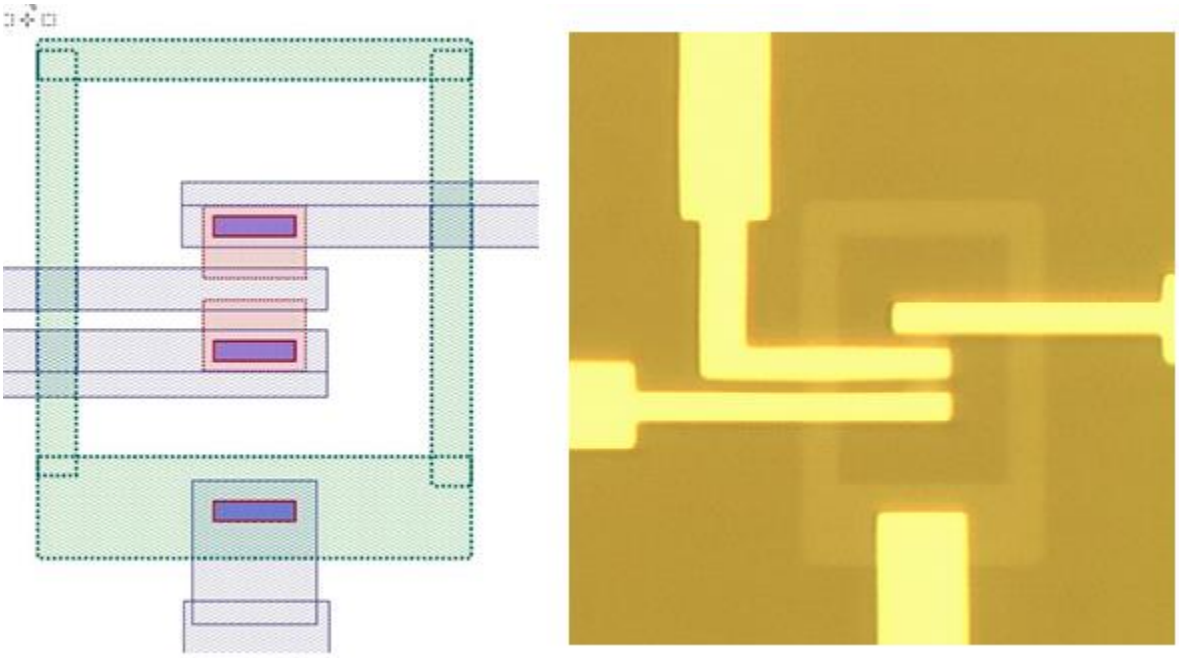


**Fig 15**: Transistor using an external ground pad (Pwell and P+) to create a local ground reference. The external pad can be made with much smaller size array than what's shown here. Similar color codes as top one; large rectangle is array of contacts on pwell, connected by metal.

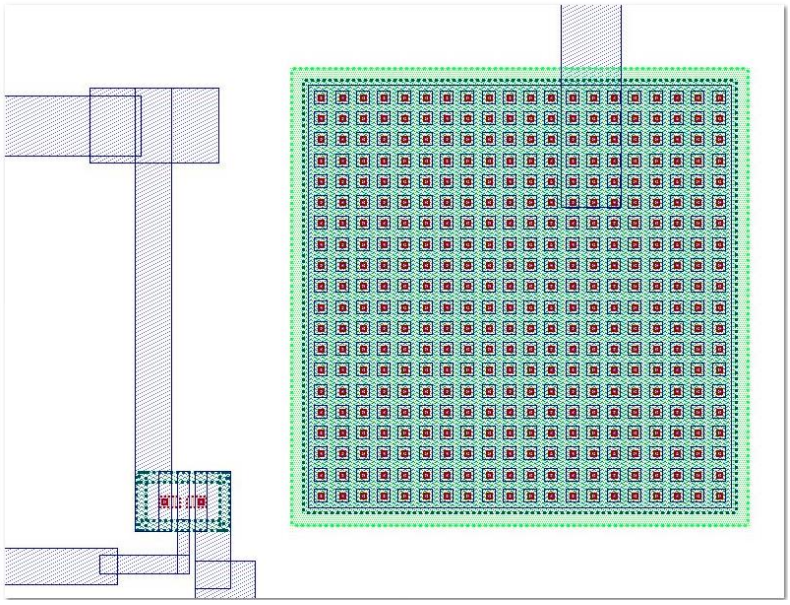
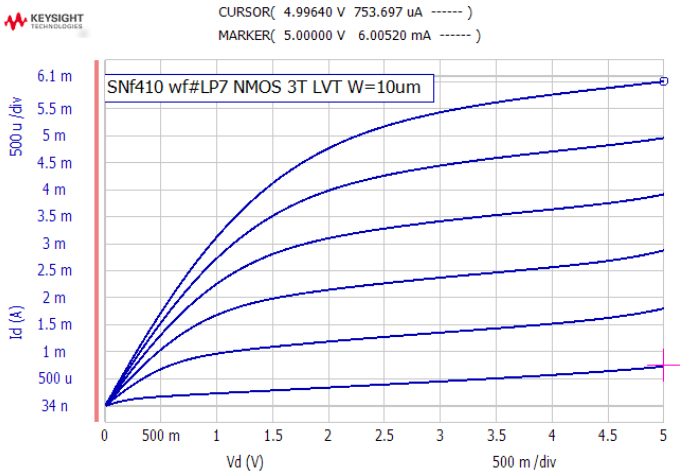
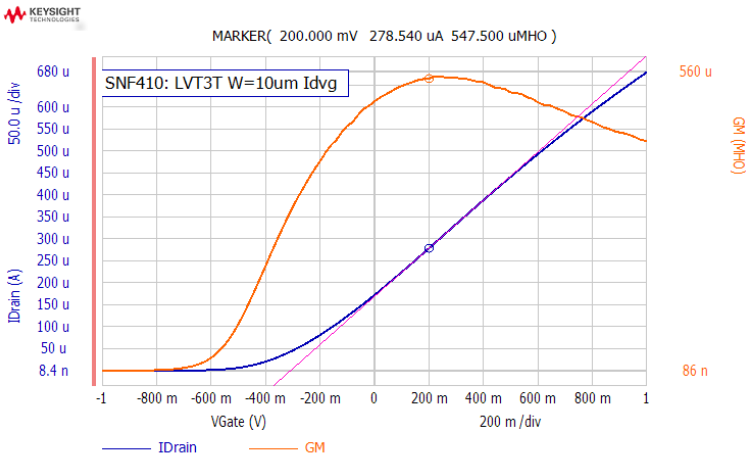


**Fig 16**: Results from **original 3-terminal LVT** (native device) Width=10um:

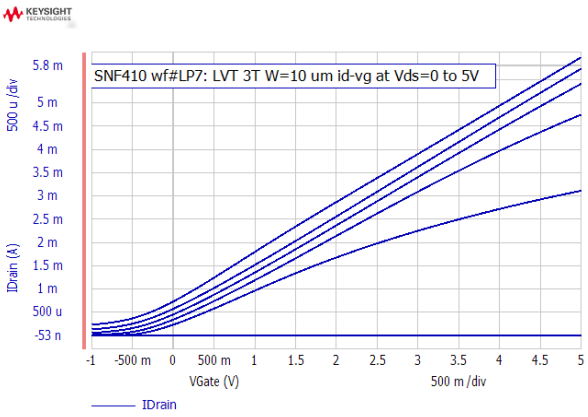
(a) Id-Vd at Vgs from 0 to 5.0v: shows Idsat=6.05 mA, Idss0=753.6 uA. (b) Gmmax= 547.5 uMho, and Vth= -400.0 mV –(500/2) = -650.0 mV, and (c) Id-Vg sweeps at Vds=0 to 5v




Id-Vds at different Vgs steps from 0 to 5v



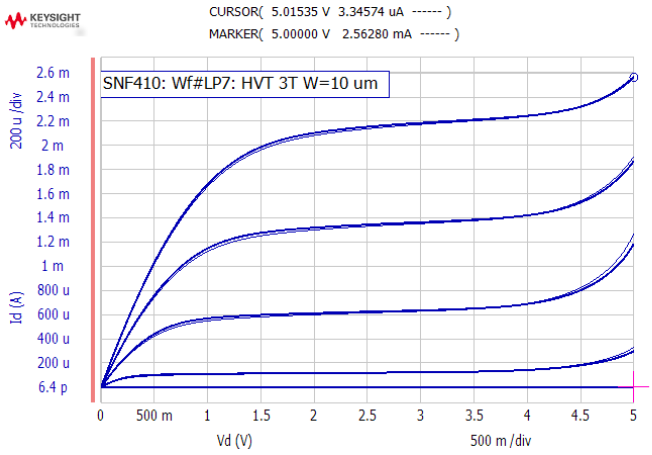

Id-Vgs at Vds=100 mV in Blue; Transconductance trace in Orange color.



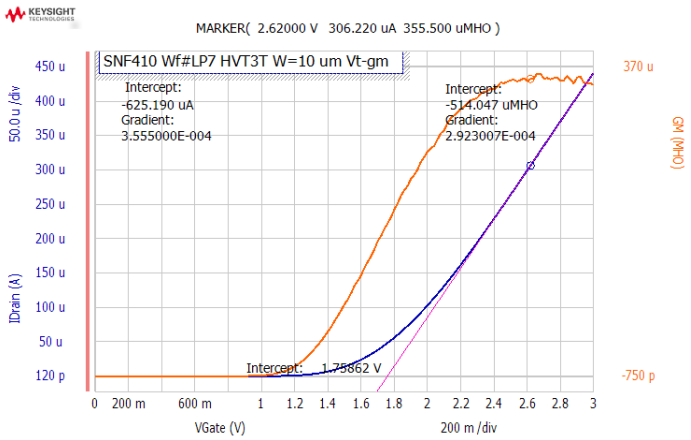

Id-Vgs at different drain voltages from 0 to 5v

**Fig 17**: Results from **original 3-terminal HVT** (Vt-imp device) Width=10um:

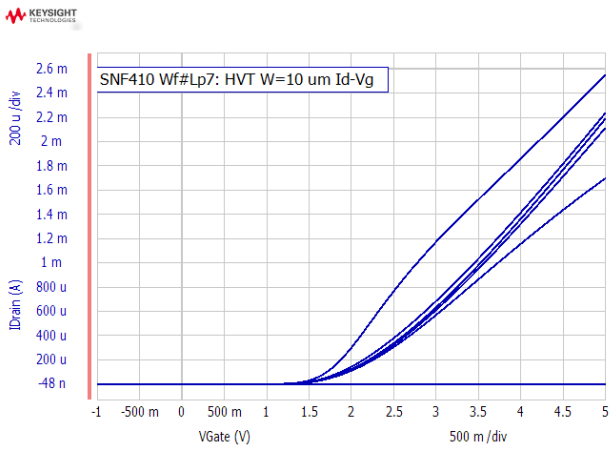
(a) Id-Vd at Vgs=0 to 5v: shows Idsat=2.56 mA, Idss0=3.34 uA. (b) Gmmax= 355.5 uMho, and Vth= 1.758 – (0.5/2) = 1.508 V, and (c) Id-Vg sweeps[Vd=0 to 5V]




Id-Vds at different Vgs steps from 0 to 5v



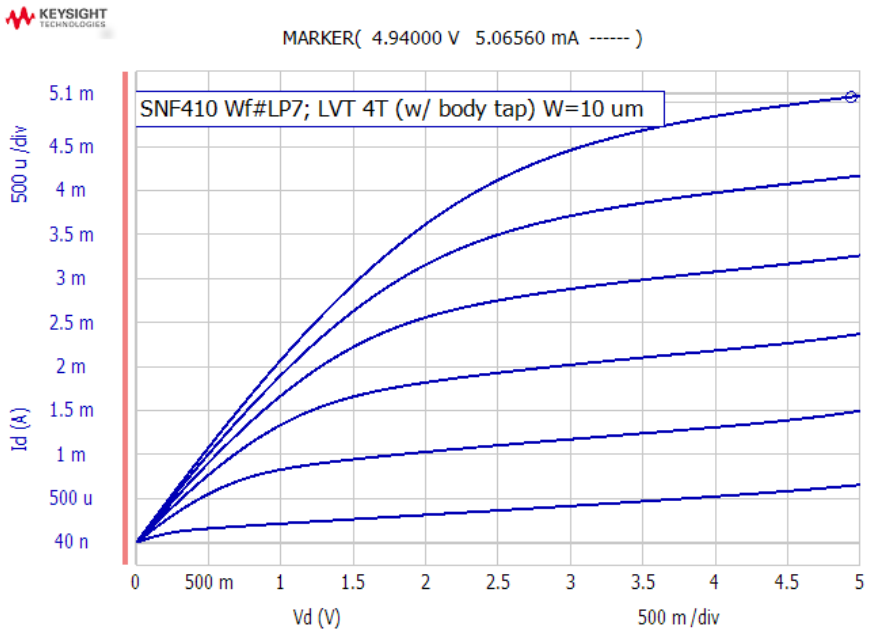

Id-Vgs at Vds=100 mV in Blue; Transconductance trace in Orange color.



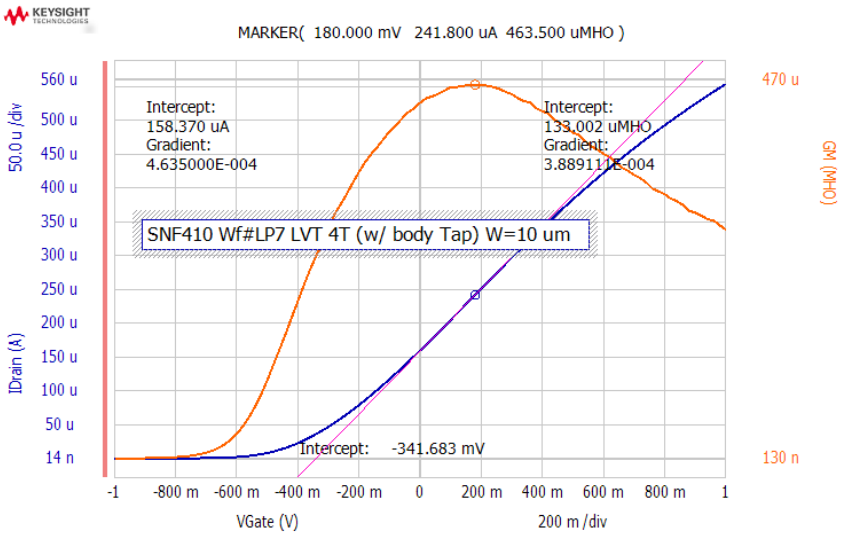

Id-Vgs at different drain voltages from 0 to 5v

**Fig 18**: Results from **new 4-terminal LVT** (native device) Width=10um:

(a) Id-Vd at Vgs=0 to 5v: shows Idsat=5.006 mA, Idss0=14.2 nA. (b) Gmmax= 463.5 uMho, and Vth= -341.6 mV – (500/2) = -590.1 mV.



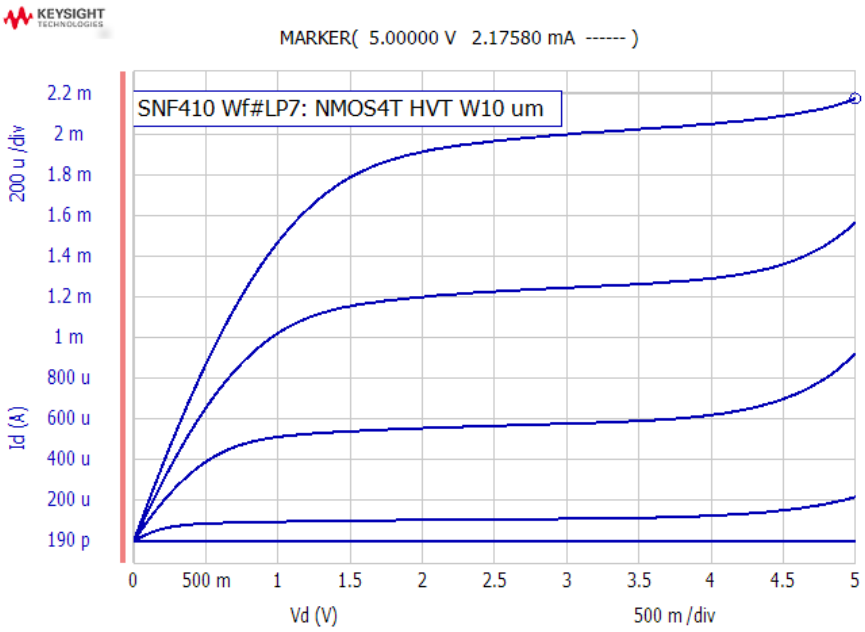

Id-Vds at different Vgs steps from 0 to 5v



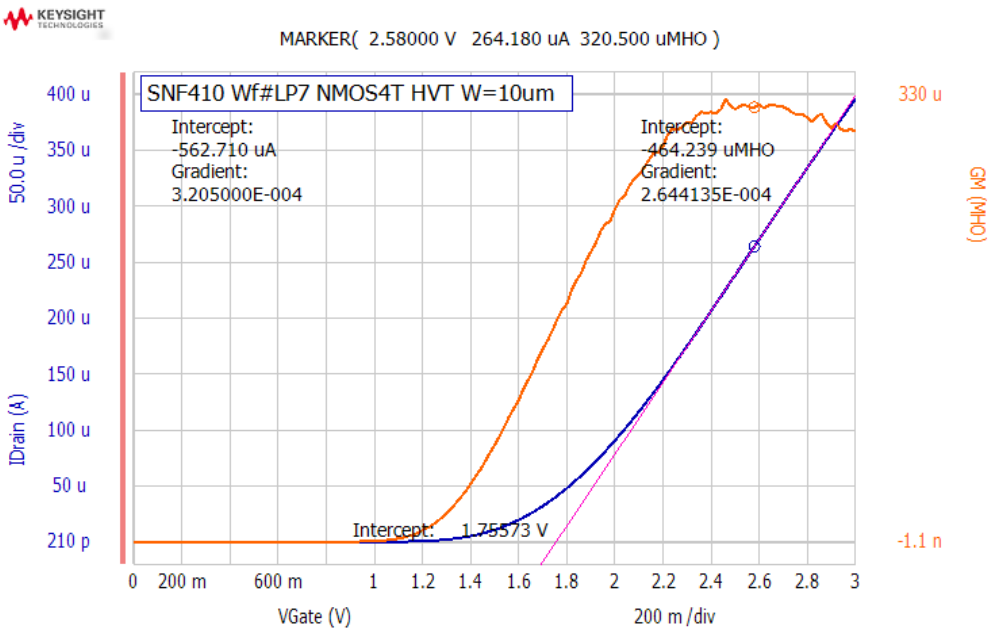

Id-Vgs at Vds=100 mV in Blue; Transconductance trace in Orange color.

**Fig 19**: Results from **new 4-terminal HVT** (implanted device) Width=10um:

(a) Id-Vd at Vgs=0 to 5v: shows Idsat=2.175 mA, Idss0=1.887 nA. (b) Gmmax= 320.5 uMho, and Vth= 1.755 – (0.5/2) = 1.505 V.




Id-Vds at different Vgs steps from 0 to 5v




Id-Vgs at Vds=100 mV in Blue; Transconductance trace in Orange color.

Based on the measurement results, the reason of discrepancy between LVT 3-Terminal to 4-Terminal (and HVT 3-Terminal to 4 Terminal) Idsat could not be determined, whether it comes from site to site variation or leakage from substrate path. A current measurement at every terminal may show how much of source current is ending as drain current versus substrate current. In most cases, a local Tub-ground through body contact is safer than using a backside chuck ground path which adds a large series R-C component in measurement set-up. The shallow junctions in silicon can be subjected to internal junction de-biasing from large series resistance of the chuck ground. Internal junction de-bias could inject extra minority carriers in the substrate, which may further lead to effects like parasitic device turn on or latch up. In large circuit blocks, it is very important to keep all ground references at same potential to avoid a Delta-ground (which may result in a circulating ground current), as opposed to a Y-ground.

## Section 3C: Lateral Bipolar device (LNPN)

With the availability of Pwell, that uses its own drive-in anneal, a lateral NPN (N+ Emitter/ Pwell Base/ N+ Collector) was perceived for this process. However, only some hand calculations of maximum depletion thickness to avoid lateral punch through were used to predict lateral spacing. A LNPN device simulation could have predicted better device layout design parameters & related Pwell junction depth in this case.

As mentioned earlier, this process does not have any LOCOS or shallow trench isolation to stop the lateral leakages between separate diffusion regions. The BJT gain (Beta) will depend on base grading profile & base width, emitter perimeter length & depth; therefore, the gain number is heavily dependent on layout and pwell drive-in depth. The silicon to oxide interface and its healing will play a role in determining leakage current resulting from sub-surface leakages.

**Fig. 20** show the LNPN device layout and as it appears on silicon.

**Fig. 21** show the LNPN Gummel curve with VCB=5V. The gain (Beta) at VBE= 700 mV to 1V region is Beta= Icoll/Ibase = 102.1 uA/5.15 uA = 19.8 (Amp/Amp), which is fairly reasonable for a parasitic bipolar, and can be used as amplifying or gain element by the designers within a limited voltage range operation. Further optimization is possible by increasing Pwell drive in (diluting the base doping) and introducing a LOCOS isolation. **Fig 22** shows the emitter/base diode show forward turn-on at 500 mV and reverse breakdown at 15.0V. **Fig 23** shows the base to collector diode reverse breakdown show onset of several leakage mechanisms at different voltages.

**Fig 20**: LNPN Device: layout and on silicon. Color code for layout reading: Green perimeter= P-isolation implant; Blue represents metal routing; Pink outlines= S/D implant (n), blue blocks with red outline= contact drawing.

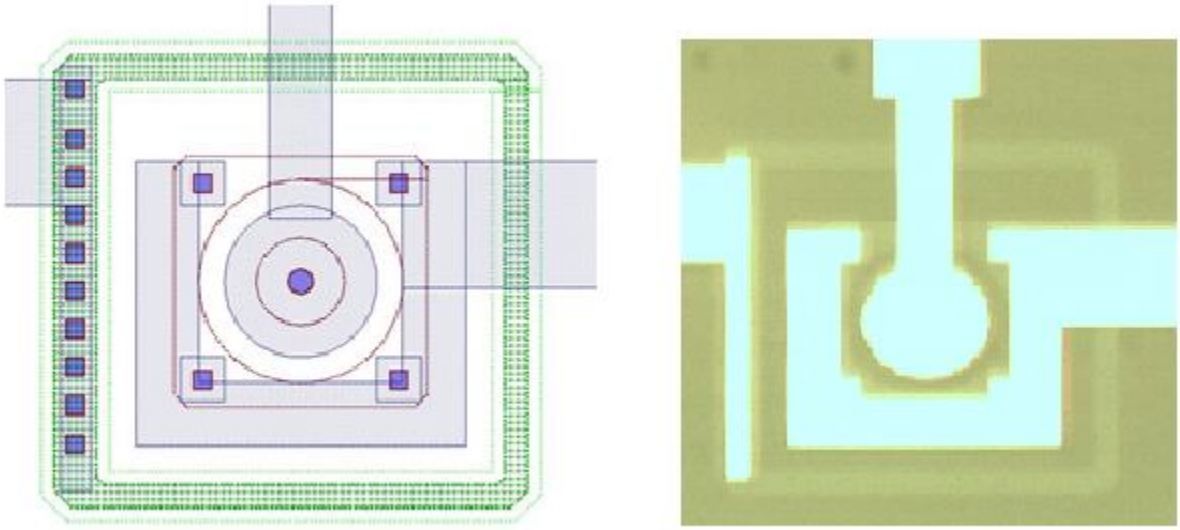


**Fig 21**: Gummel Curve for the LNPN at VCB=5V

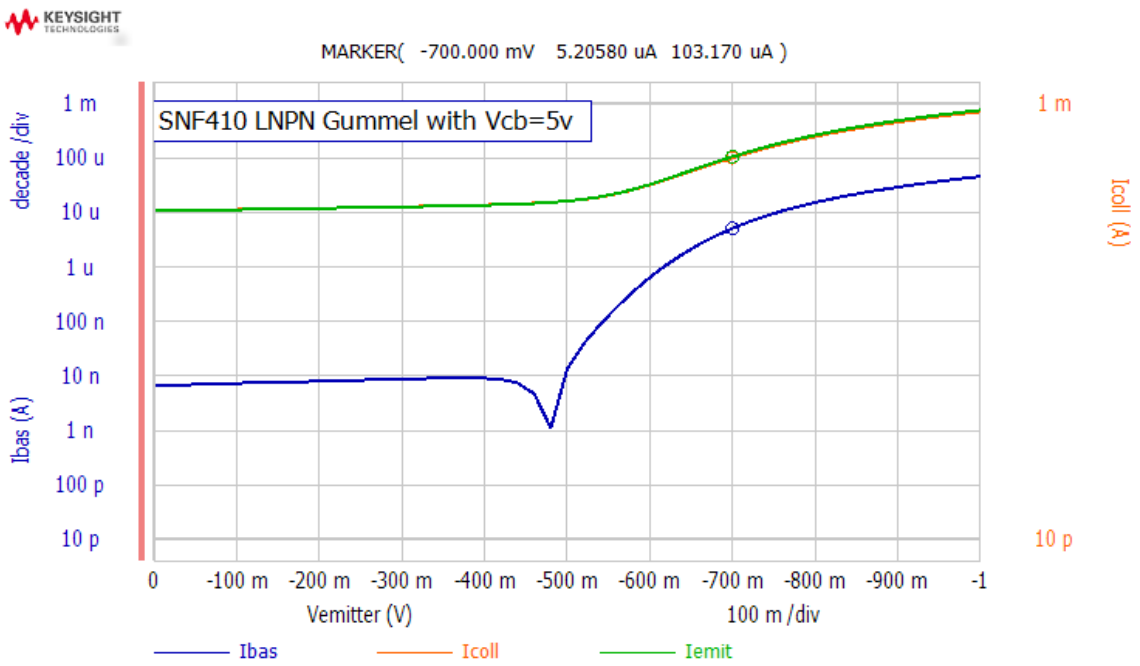


**Fig 22**: Emitter/Base Diode measurement for the LNPN: show forward turn on at 500.0 mV and reverse BV at 15V. This is a log(current) vs. bias voltage curve. At V=-0.6v, diode forward turn on is observed with exponential increase of current. At reverse bias of +10v, leakage starts increasing, and diode breakdown is observed at 15v.

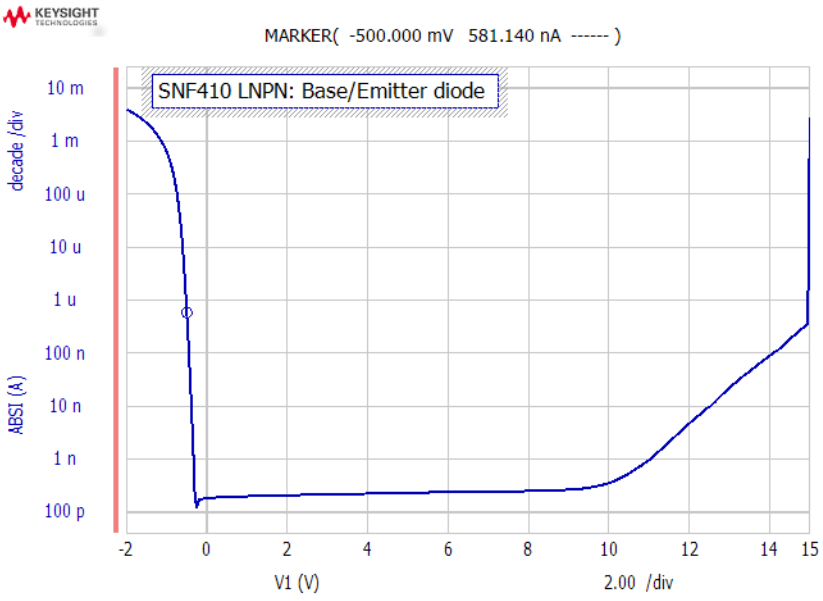
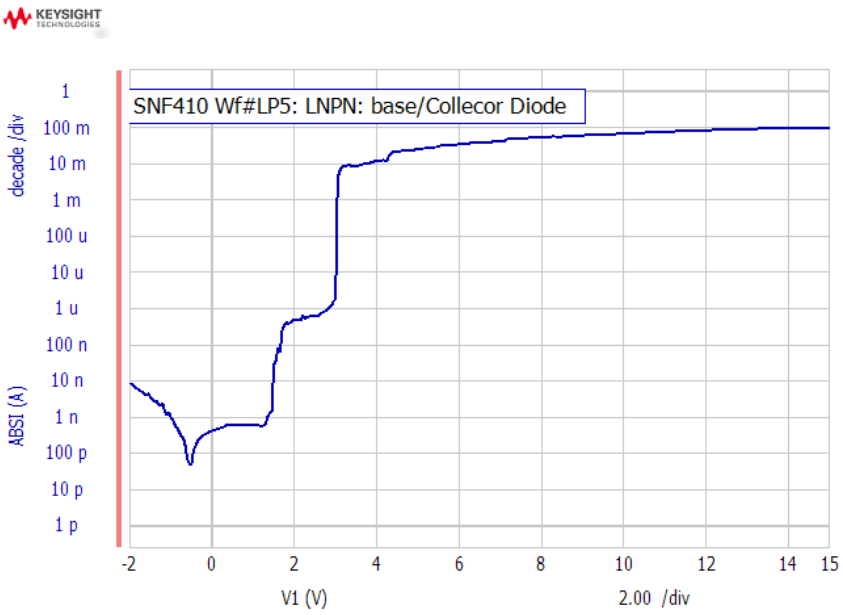



**Fig 23**: Collector/Base Diode measurement for LNPN: show onset of multiple leakage mechanisms. The low breakdown voltage is most probably due to surface or sub-surface punch-through, rather than junction breakdown.



## Section 3D: Vertical Diode (N+/Pwell)

With the availability of Pwell, vertical diode is also perceivable in this process. **Fig. 24** (a) shows the layout of an area diode and Fig 24 (b) shows the layout of a perimeter intensive diode: **Fig 25** (a) & (b) show measurement of forward & reverse bias characteristics.

**Fig. 24(a)**: Diode N+/Pwell. (a) Area diode (100*100um2). Color code for layout reading: Green perimeter= P-well implant; Blue represents metal routing; Pink rectangles= S/D implant (n+), blue blocks with red outline= contact drawing.

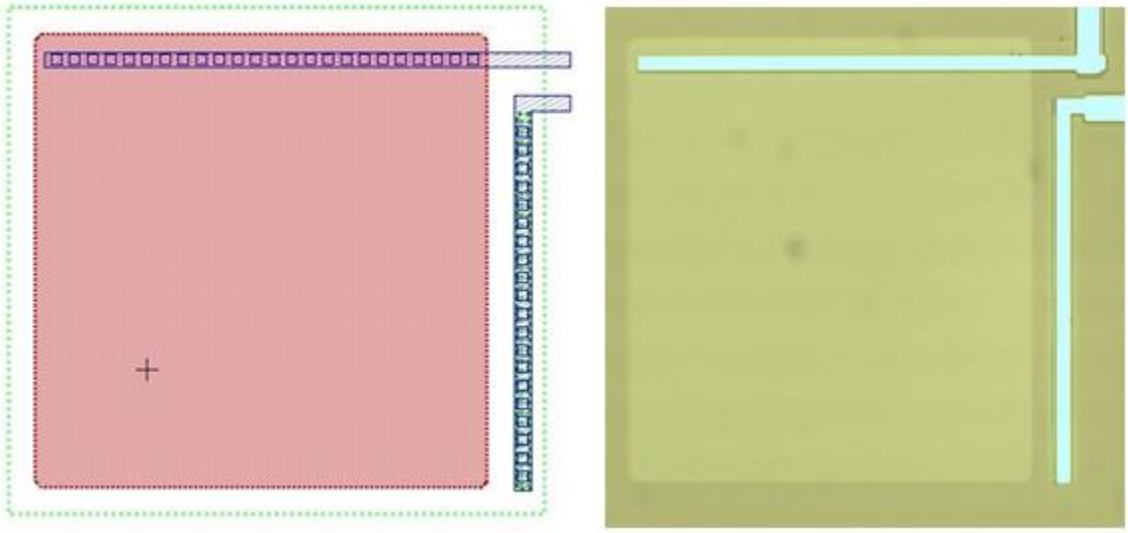


**Fig. 24(b)**: Finger diode [50*(100 um*0.8 um). The n+ region are striped and many, compared to a solid rectangular block in area diode.

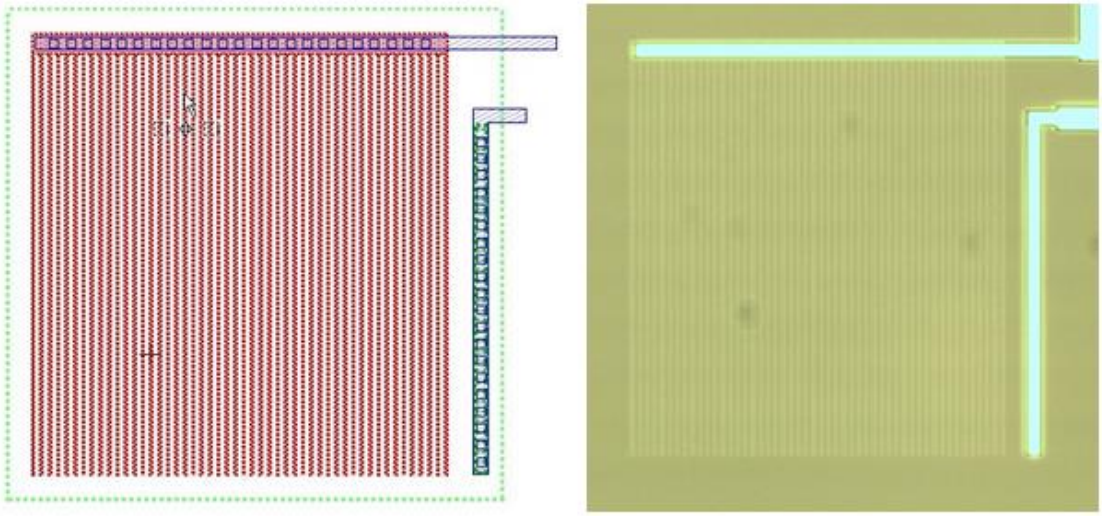
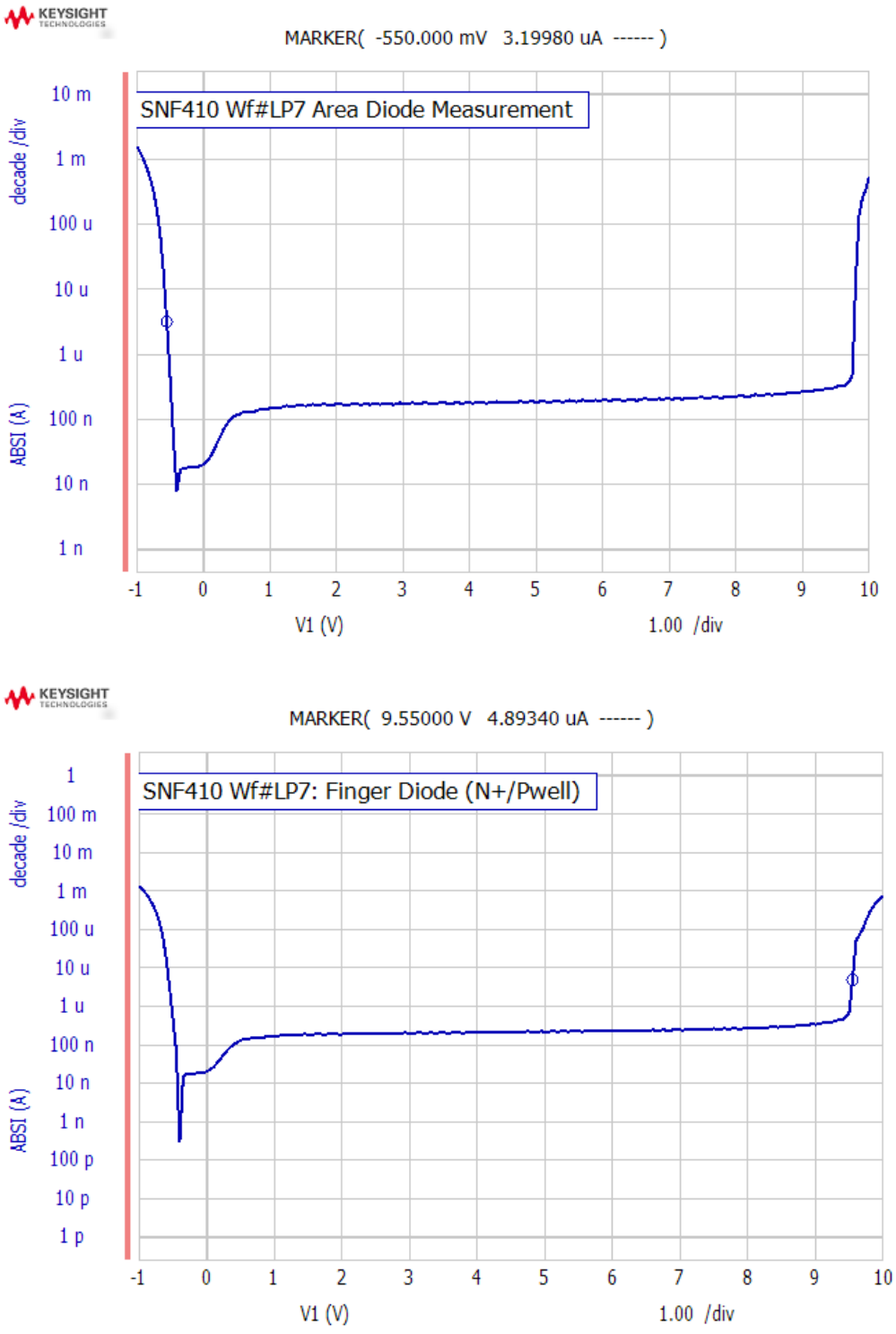


**Fig 25**: Diode measurements. (a) Area diode (b) Perimeter intensive diode



It might be worth mentioning that usually a perimeter intensive diode may show much higher leakage (orders of magnitude) than area diode. The perimeter leakage current is affected by total edge length, edge roughness, etching process and its gradient over the wafer, surface states, annealing condition etc.

Diodes are very important elements for design, failure analysis techniques and process control monitoring. Diode current increases exponentially with temperature, whereas resistive leakage current does not. An important concept needed for identifying the leakage element during failure analysis of chips.

Therefore, the addition of a lateral bipolar as gain element and diode as a rectifying element definitely allow this depletion nmos process with Pwell to demonstrate some simple analog design blocks.

## Section 3E: Contact Chains

There are 3 sets of Contact Chain which are made by individual N+ area having 2 contacts on two sides, connected by Metal 1. There are (20x10=200) individual links, each having 2 contacts. The structure is in a Pwell Tub (for vertical isolation), and individual elements are isolated by lateral spacing (in absence of LOCOS/ STI). The size of contacts are (1.5*1.5), (0.8*0.8) & (0.6*0.6) um2. Measurement unit is: (Ohms/link). As contact sizes get smaller, contact resistance/link will increase. Process parameters like silicon over-etch, contact fill material, N+ area sheet rho, contact fill profile, contact sidewall lateral etch profile will affect this value. This structure can also be used as process control monitor for etching of N+ active in silicon. An overetch in silicon will produce etched away N+ region under contact, and will increase contact resistance by current crowding. This, in turn, would affect other active device characteristics, like bipolar transistor gain or linearity.

**Fig. 26** shows the details of structure layout and Table 1 presents measured data. **Fig. 27** shows a sweep measurement on contact chain. From this plot, resistance/link value is extracted and used to plot Fig 28 for contact resistance versus area. As can be seen from **Fig 28**, contact resistance goes higher as contact area gets smaller. However, the change is very drastic between 0.8 um to 0.6 um. Increase in current crowing around the smaller contacts may contribute to this characteristics. This is an important data in order to determine the optimum contact size for active devices for this process flow.

**Fig 26**: Contact Chain Structure in layout and on silicon. Color code for layout reading: green perimeter= pwell implant; Blue represents metal routing; Pink rectangles= S/D implant (n), blue blocks with red outline= contact drawing.

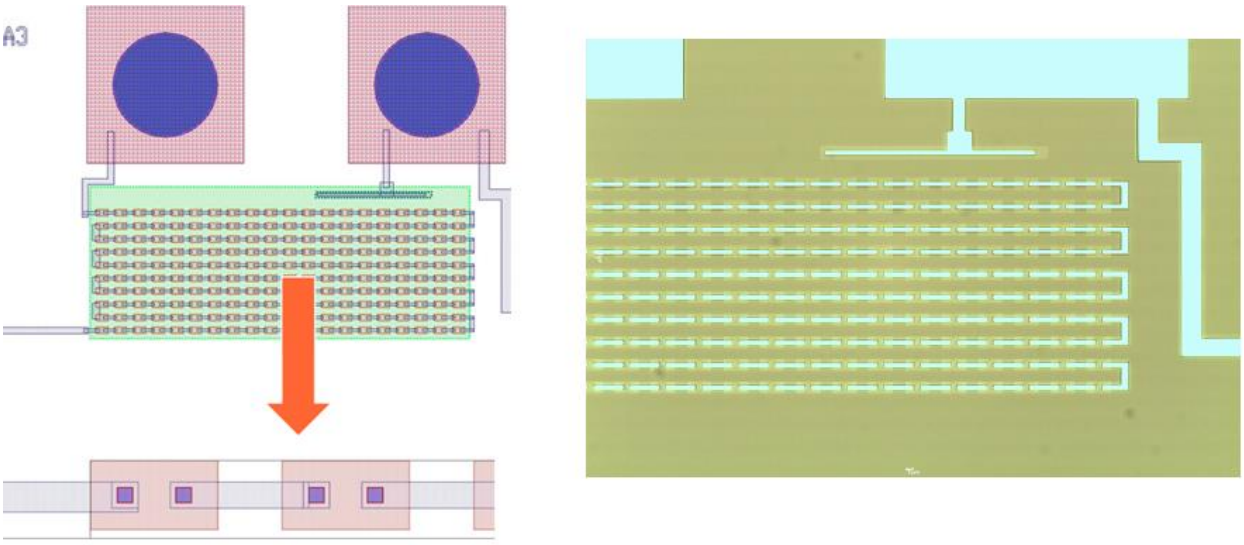



**Fig 27**: Contact Chain Measurement:

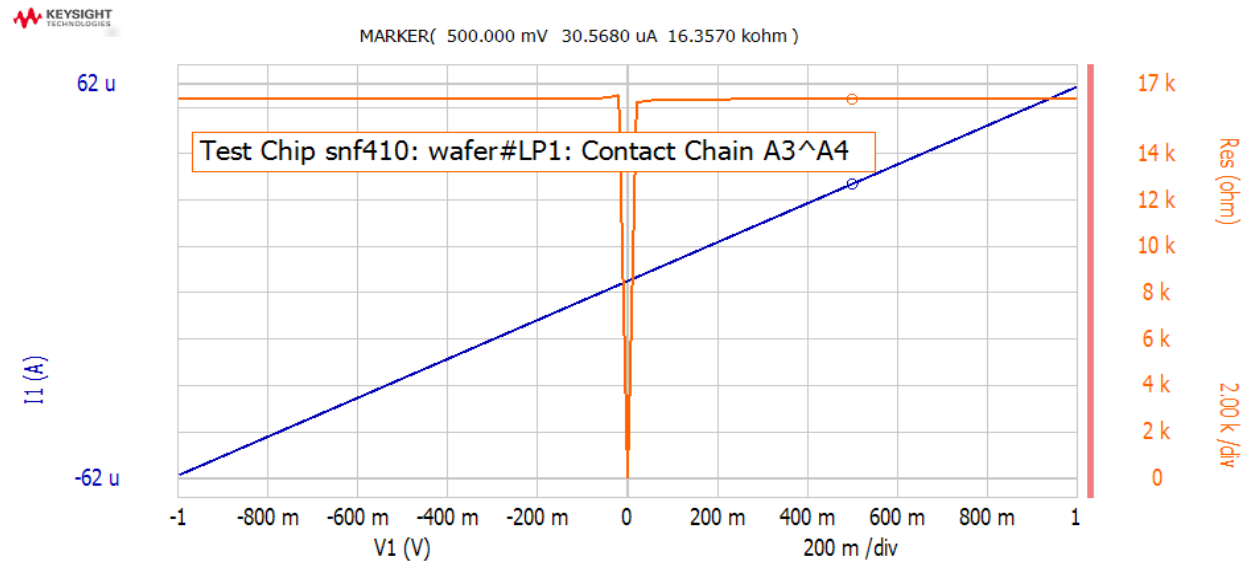
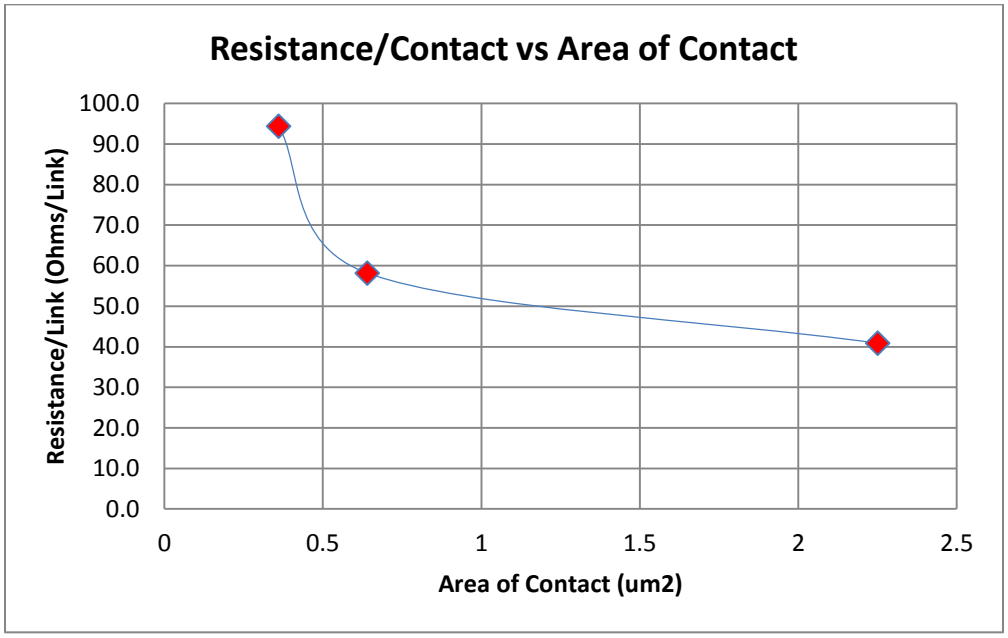


**Table 1**: Measurement results from Contact Chains of 3 sizes (Wf #LP1, 1st batch)

| Contact size | Area of contact | Total Resistance | No of Contacts | Res/Contact | Res/Area |
|---|---|---|---|---|---|
| um*um | um2 | Kohm | # | Ohms/Contact | Ohms/um2 |
| 1.5x1.5 | 2.25 | 16.357 | (20*10)*2 | 40.9 | **7269.8** |
| 0.8x0.8 | 0.64 | 23.275 | (20*10)*2 | 58.2 | **36367.2** |
| 0.6x0.6 | 0.36 | 37.7758 | (20*10)*2 | 94.4 | **104932.8** |

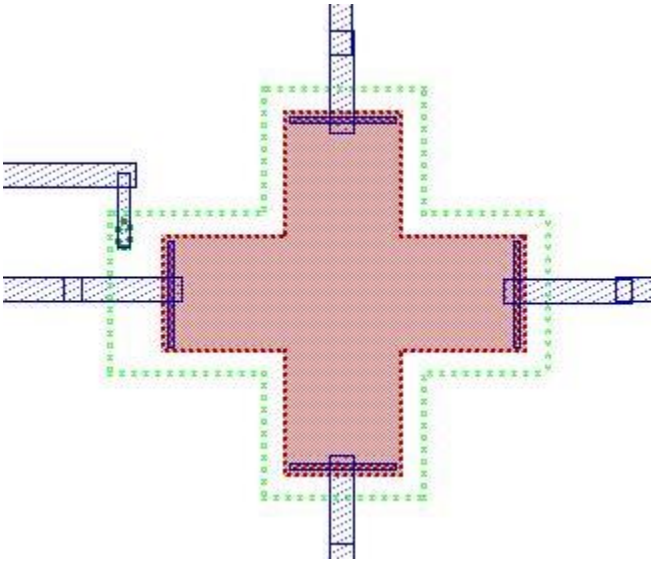
**Fig. 28**: Measured resistance per Contact vs Area of each Contact



## Section 3F: Van der Pauw Sheet Resistance measurement on N+/Pwell:

The Van der Pauw sheet rho structure was drawn to measure sheet rho of N+ region, the Pwell to be connected to Ground along with VLow terminal of the N+ cross. Alternate is to use a biasing_T to hold the chuck at GNDU in parallel to Voltage force low terminal. At the time of writing this report , the measurement result was not available. However, form functionality of contact chains and diodes, it is supposed to be functional.

**Fig: 29**: Van der Pauw sheet resistance measurement structure. Color code for layout reading: green perimeter= P-pwell implant; Blue represents metal routing; Pink rectangles= S/D implant (n), blue blocks with red outline= contact drawing.



## Section 3G: More "ZERO COST" & "LOW-COST" devices that could be supported by the process

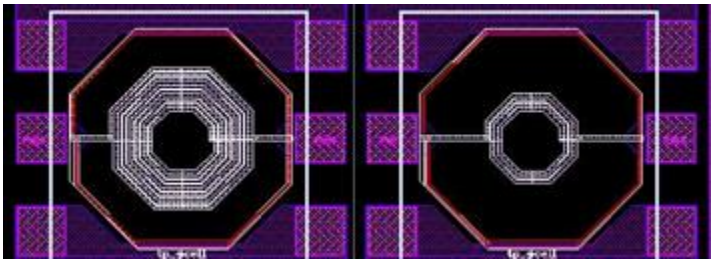
The "ZERO COST" device is referring to devices which can be further supported by the NMOS depletion flow with Pwell option, but without adding any extra implant layers. i.e, these devices could be made with existing implants of Pwell, P+, N+ & HVT. However, these devices will need new layout and reticles, as they are not existing in this reticle. Here is a list:

1. NMOS device with PWELL as Body.
2. OXIDE CAPACITOR on PWELL only.

With an addition of NWELL, which needs its dedicated mask & implant, but may share the screen oxide & drive-in anneal with PWELL, possibilities will be many; including

complementary MOS & Bipolars (P+/Nwell/P+ in Pwell as Emitter/base/collector) The Implant energy and dose of the Nwell can be controlled to give the Nwell profile to have a different depth than Pwell. With a 2-Layer Metal, Logic gates and Inductor coils could be supported. The Logic gates in EE312 reticle already use a Metal 2 layer for interconnection. Fig 30 show an example of Inductor Coil layout. With these complementary bipolar, diode, MOS and passive components like inductor, capacitor & resistor, it will be possible to further push the process capability into analog domain.

**Fig: 30**: Example of Inductor Coil Layout with different number of turns in Ground/Signal/Ground (GSG) configuration and a substrate guard ring around.



## Section 3H: General discussions on test structure/devices

It is pointed out that there are more test structures in the original EE312 reticle, which are copied over along with the new structures in SNF410 reticles. The original EE312 structures have been measured for sanity check and calibration; however, have not been reported here.

The NMOS logic gate functionality depends on logic “zero” and logic “one” state. So as long as there is enough noise margin left between the states, the gate is expected to function properly. LNPN devices show high leakage between lateral diffused area in absence of LOCOS isolation. However, these show a gain about 20 (Amps/Amps) at Vbe= 0.7V to 1.0V. The N+/Pwell diodes show decent characteristics. The passives like diffused resistors and capacitors also show reasonably okay characteristics. Therefore, despite the deviations from ideal device characteristics, and high yield numbers, these active and passive devices can still be used in different logic and analog blocks. There is room for further pushing the process into analog power domain by some additional “zero-cost” and “low-cost” devices, as have been discussed in previous section.

# SECTION 4: UNIT PROCESSES CRITICAL TO THE YIELD OF TESTCHIP:

To obtain good yield numbers with this process flow, there are some unit processes that should be closely monitored and calibrated for each silicon run. These processes are discussed in the following section.

(1) Gate Oxidation Time for 750 Ang WETOX & 300 Ang DRYOX
(2) Contact Etch Time in P5000 Chamber B
(3) HF Dip Time at Standard Resist Strip after Contact Etch
(4) Singe Oven Bake of wafers at 200C for 30 min to 1 hour prior to LOL2000 Coating
(5) Keeping wafer surface soaked under Acetone or IPA during Lift-off process.

(1) Gate Oxidation Time:

It was observed during 750 Ang WETOX recipe development (25 minute @900C) that there is growth rate difference between Thermco1 & Thermco3, as expected for any furnace.. Therefore it is prudent to run test wafers based on Oxidation time & thickness recorded in log book to determine the actual Oxidation Time for that furnace. APPENDIX B & C shows the thickness variability based on statistical data for Thermco1 & Thermco 3 for this silicon run.

(2) Contact Etch Time:

The Recipe in P5000 Chamber B used for Contact Etch is called "surromed"; The chamber needs to be pre-conditioned and then a blanket 1000 Ang Oxide Test wafer is used to determine the etch rate on blanket oxide film. Depending on the etch rate, and necessary overetch, the etch time will vary. e.g, the runcard specifies the etch time of 160 sec, however for the two batches of silicon run of SNF410 wafers, the etch time used was 150 sec.

(3) HF Dip Time at Standard Resist Strip after Contact Etch:

The resist strip process after Contact Etch in P5000 uses resist ash in gasonics followed by Piranha Strip & Dump Rinse. After 6 cycles of Dump Rinse, the wafers are wet transferred to 50:1 HF bath for 20 sec etch. This step mainly eliminates polymer deposits on Contact sidewall from the P5000 plasma etch process. However, the timing of this 20 sec etch is very critical Excessive etch will thin out the thermal oxide and affect the contact sidewall opening profile further affecting LOL adhesion to the oxide. Also, if reworks are done due to poor LOL2000 and photo resist develop quality prior, then only Piranha is to be used. No HF dip is required at rework for LOL & Photoresist develop steps.

(4) Singe Oven Bake of Wafers at 200C for 30 min to 1 hour prior to LOL2000 Coating:

During the first batch of silicon run (wafers clean room out in March, 2017) several reworks were necessary due to the poor adhesion of LOL2000 to substrate. After develop of the photoresist, it was observed that poor adhesion of the film is accompanied by circular shaped area showing multi colored fringes ("bubbles") under microscope light in the product wafer (SNF410 wafers). However, none of the accompanying silicon test wafers that got coated, exposed and developed at the same time exhibited this adhesion- and multi-color "bubble" problem. Per suggestion from Mahnaz M., a bake in Singe oven at 150C was introduced after the SRD cycle, prior to LOL coating. The situation improved to a great extent, but was not cured 100%. So next time a high bake temperature & time was tried (White Oven at 200C for 1 hour), and the problem went away totally. Therefore, it is concluded that the problem was related to moisture retention in the surface of the product wafers.

The test wafers had silicon on surface, after coming out of HF dip, the surface becomes hydrophobic. The product wafers had 300 Ang SiO2 on the surface, coming out of the HF dip and following dump rinse and SRD cycle their surface became hydrophyllic. The moisture retained on the surface below LOL2000 coating. However, after the LOL2000 bake at 195C, they came out underneath the LOL layer like bubble bursts, which affected later steps of photoresist coating and develop. Once the dehydration bake was introduced, this problem was never seen again in the next two runs of silicon.

(5) Keeping wafer surface soaked under Acetone or IPA during Lift-off process:

It is very important to note that during the processing of the Pt Lift off wafers, the wafer surfaces should be kept moist all the time (with acetone, 1165, PG remover or IPA depending on the different steps in Lift-off). Once the surface gets dried up from the wet bench air circulation, the Lift off products get attached to surface creating internal shorts between device terminals. Also overnight soak in acetone followed by sonication of 5 minutes gives better result than using only 5 minutes acetone soak with sonication alone. Under microscope, it can be seen that the edges are pretty straight, compared to some jagged edges with 5 minutes acetone soak with sonication.

# SECTION 5: CONCLUSION

In this report an **optional** Pwell addition to the original NMOS Depletion flow [EE312 Testchip] was discussed. New device functionality was demonstrated with reasonable success.

Two batches of silicon were run in this process flow. Both batches produced Control wafers (without Pwell) to mimic the original EE312 flow and wafers with Pwell. The first batch of 4 wafers (March 2017) produced limited success in demonstration of devices. These wafers got seriously affected in gate oxide related area due to multiple reworks done on wafers related to LOL2000 adhesion problem. In the second batch (July 2017), 3 more wafers came out of clean room with fixes to originally stated problem. These 3 wafers (2 wafers with Pwell: **LP7, LP5** and 1 Control wafer **LC17**) were fully successful is demonstration of the enhancement of the capability of the original process and were used to provide the characterization data presented in this report for most cases.

It was shown that both the 3 terminal depletion- and enhancement-NMOS (NMOS LVT & NMOS HVT) were fully functional in Module 1 of the Testchip. Module 2 contained 4-terminal versions of the same NMOS in two different layout styles. Both showed good functionality. The 4 terminal NMOS were done per advice from Prof. R. Howe. In addition, the Diodes, Lateral BJT, contact chains: all showed reasonable functionality as possible by the process. The new devices were discussed in detail with Prof. K. Saraswat at the initial phase of flow definition and simulation. An extensive gate oxide characterization on several wafers from 1$^{st}$ and 2$^{nd}$ batch silicon gave good insights to how to improve the gate oxide quality further in the process. There are about 10 wafers at HOLD after Pwell implantation (implanted a full batch of 24 wafers with Pwell at ion implantation) in Litho area, should another verification/flow enhancement run is required in future.

Therefore, this Testchip (SNF410) provides success in obtaining functional devices from both the original EE312 testchip and the added Module 2. Thus it can be qualified to use instead of EE312 original reticle if there is a need for the enhanced flow with Pwell. This Testchip can also be used for further future enhancement of the original flow by an Aluminum backend process. Some ground work for determining optimum 0.5 um thick Aluminum dep, necessary PR coating thickness (1.5um), ASML energy & focus for Aluminum, PR develop time had already been completed. The last remaining unit process required is the etch recipe for Aluminum with some silicon overetch (N+ or P+ area in contacts). There are 6 product wafers at HOLD at Contact Etch step for final demonstration of the Al backend process.

Finally, if the question were to be asked “if an optional Pwell flow were to become available, would its deliverables could justify the cost of its development?”; the answer is YES, as was demonstrated by the enhanced results, new devices, and projected new analog capabilities in parallel to its existing digital performance. And the flow will still be short and sweet, like the original process flow.

**ACKNOWLEDGMENTS**:

I would like to express my gratitude and thanks to Usha R., Mahnaz M., Maurice S. and Uli T. for their guidance, technical suggestions, valuable insights, and encouragements in carrying out this project.

Special thanks to Mary T., whose kind considerations enabled me to start as a "volunteer" in SNF. For me, it was a great deal; since it brought back many experiences in the clean room from student days but with a deeper understanding: the clean room equipment experiences that I never had to use again in the next 18 years in industry.

This work is dedicated to the memory of my father,

A. B. M. Azizur Rahman

# APPENDIX A

## Flow simulation for SNF410 w/ PWELL option

# Initialize the simulation
init field=Boron concentration=2.5e15<cm-3> resistivity=5.49 wafer.orient=100

**#pad oxide 750Ang Wet Oxide is grown and pwell implant is added**
**diffuse temperature=800<C> time=10<min> ramprate=10<C/min>**
**diffuse temperature=900<C> time=25<min> H2O**
**diffuse temperature=900<C> time=35<min> ramprate=-2.857<C/min>**

**#Pwell implant**
**implant Boron energy=180<keV> dose=2.5e13<cm-2> tilt=7<degree>**

**#Pwell activation**
**diffuse temperature=1100<C> time=120<min>**

**#Sacrificial Oxide etch**
**strip Oxide**

#Grow 300nm Thermal Dry Oxide
diffuse temperature=800<C> time=10<min> ramprate=10<C/min>
diffuse temperature=900<C> time=150<min> O2
diffuse temperature=900<C> time=35<min> ramprate=-2.857<C/min>

#Isolation P+ Implant
implant Boron energy=60<keV> dose=5.0e15<cm-2> tilt=7<degree>

# Source/Drain N+ implant
implant Arsenic energy=60<keV> dose=2.0e15<cm-2> tilt=7<degree>

# High Vt channel Implant
implant Boron energy=60<keV> dose=1.0e13<cm-2> tilt=7<degree>

#Anneal S/D
diffuse temperature=1000<C> time=20<min>

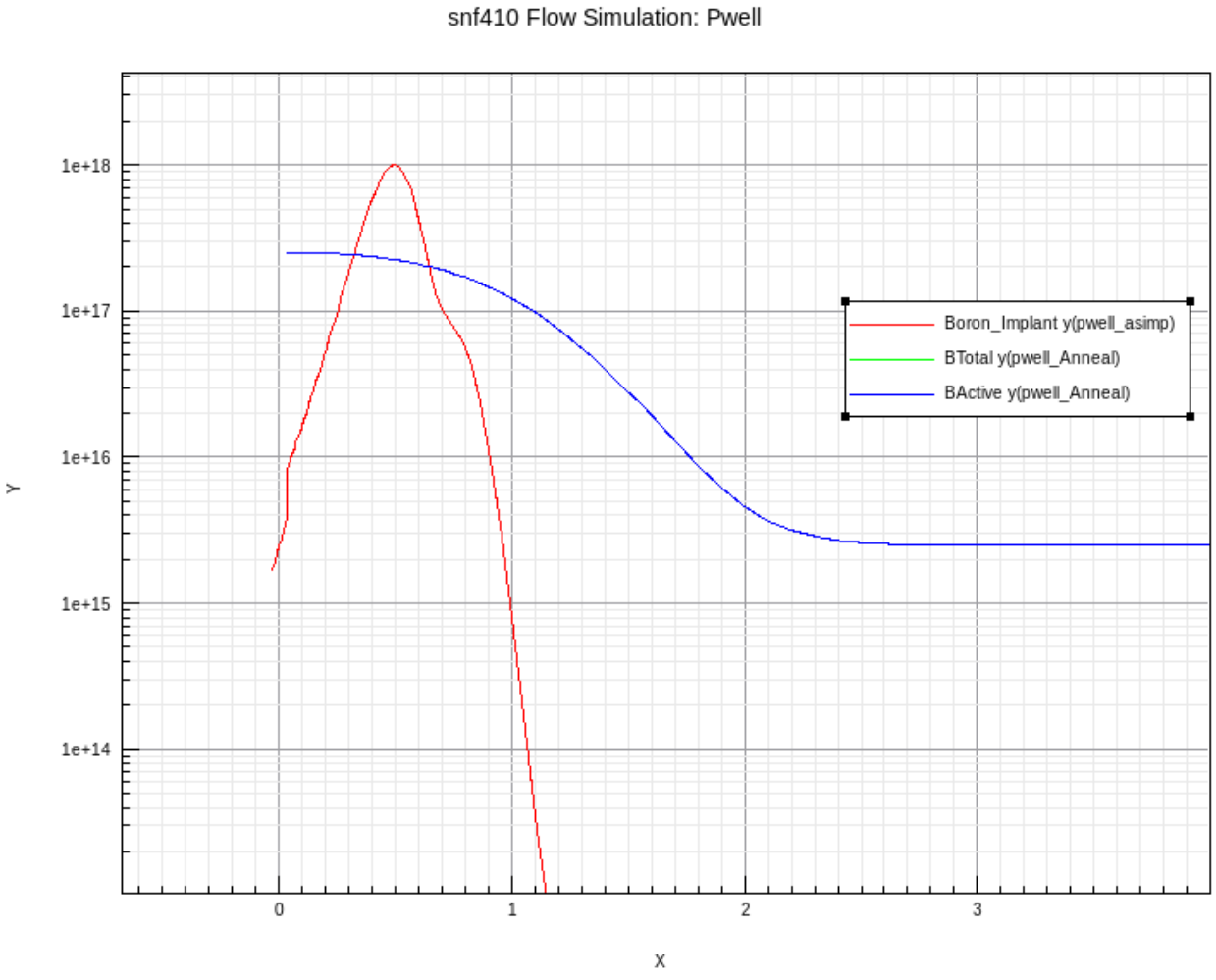
## A2: Notes about the process flow differences:

* Pwell Implant & Drive-in do not affect the thermal budget of the core flow

* The Pad oxide for Pwell is sacrificed prior to growing the 300 Ang oxide. So the Pwell implant does not affect the quality & reliability of the 300 Ang Oxide.

* The Pwell drive in can be independently controlled. It will be a major contributor to the lateral bipolar (N+/ pwell/ N+) gain. May need further optimization based on present performance.

## A3: Simulated P-Well profile as-implanted and after Drive-in:



## A4: Pad Oxide thickness for Pwell implant; this oxide is stripped after drive-in

```
select Z= "1"
-------------------------------------------------------------------------------
------------------------------------------------------------ layers -----
layers
-------------------------------------------------------------------------------
{         Top                Bottom             Integral             Material }
{ -3.738514671019e-02 2.819560981323e-02 6.558075652342e-06 Oxide }
{ 2.819560981323e-02 4.000000000000e+00 3.971804390187e-04 Silicon }
------------------------------------------------------------ implant -----
implant energy= 180.00<keV> dose= 2.50e+13<cm-2> tilt= 7.00<degree> Boron
-------------------------------------------------------------------------------
```

- Oxide thickness simulated = 6.55E-6 cm = 6.55E-6*E8 Ang= 655 Ang (with runcard value of parameters)

-Runcard Value = @Thermco1 avg oxide thickness= 685 Ang (appendix for data)

-Silicon consumed =2.81E-2=28.1E-3 = 28 nm = 280 Ang

-[280 Ang/ 655 Ang = 0.42] Ratio of Silicon consumed to Oxide Thickness

(calculation ref: Sentaurus Manual http://nadin.miem.edu.ru/Sentaurus_Training_2014/sp/sp_b.html, Chapter 2, section 2.7)

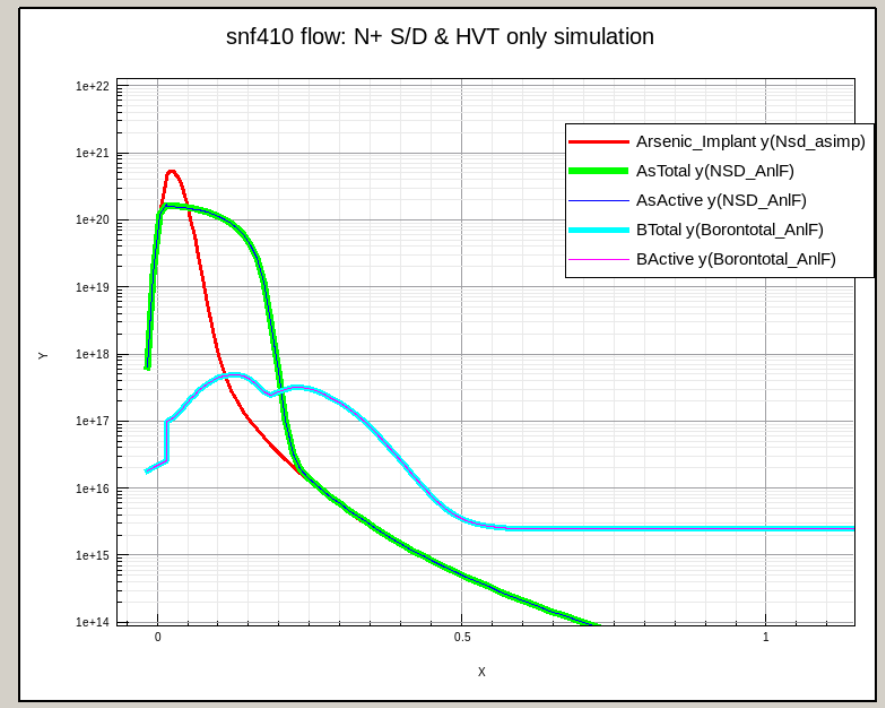
## A5: S/D N+ to HVT P+ junction depth after final anneal (1000C, 20 min)

Section A5 of this Appendix show Source/Drain to HVT P+ junction depth after final Anneal in Thermco at 1000C for 20 minutes in Nitrogen. A5(i) shows simulation result from the author, A5(ii) shows simulation result by Muyu Xue.

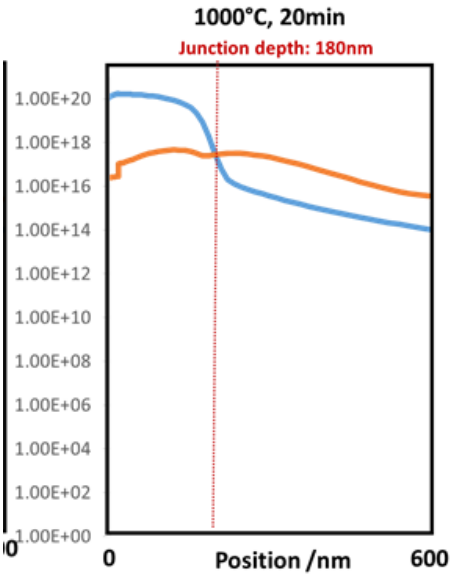
Note that:

- S/D peak concentration after anneal is 1.5E20/cm3; junction depth after anneal is (0.202 um – 135 Ang) = 1885 Ang = 188.5 nm for A5( (i)
- Compare this value to Muyu's simulated value of 180 nm A5 (ii)

## A5 (i): S/D N+ to HVT P+ junction depth after final anneal (1000C, 20 min)

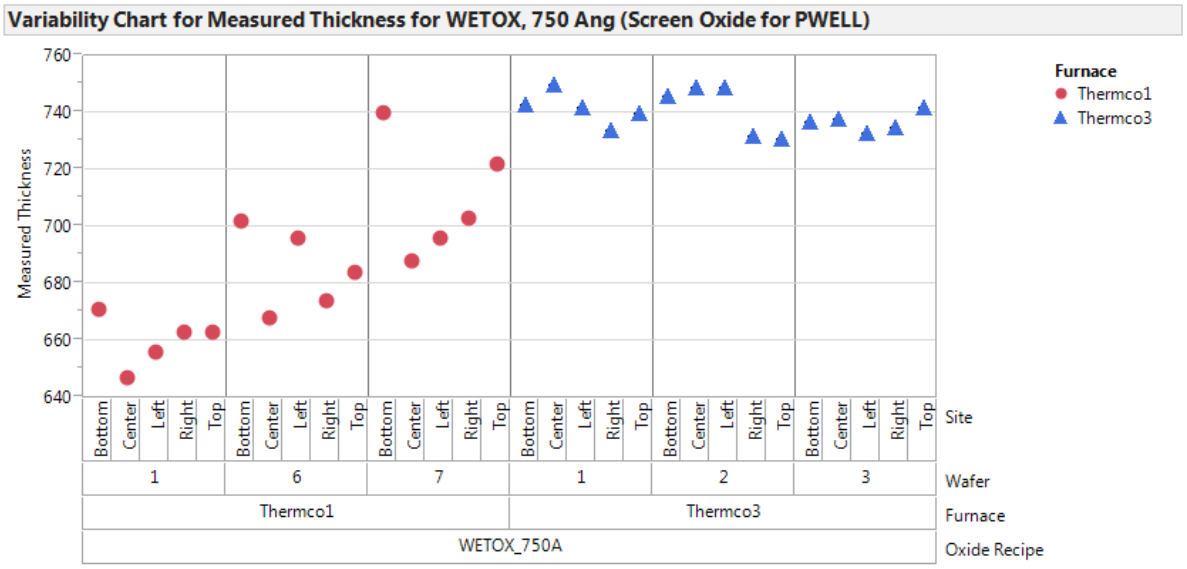


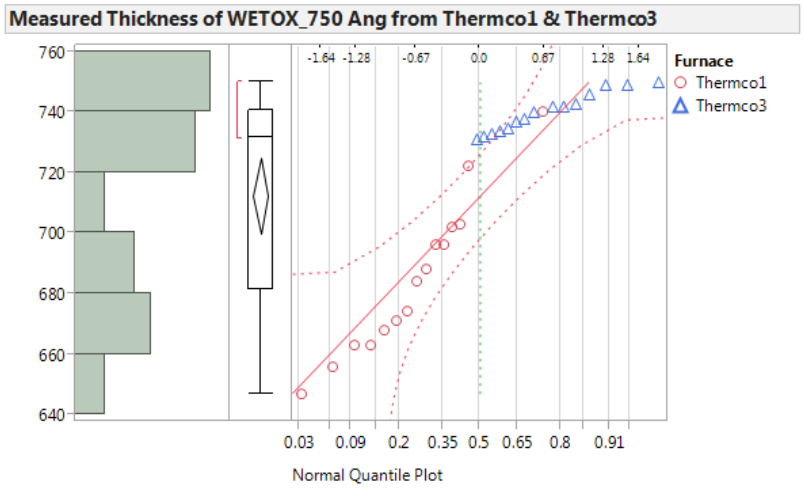

## A5 (ii) : S/D N+ to HVT P+ junction depth after final anneal (by Muyu X.)



# APPENDIX B

## Oxide Thickness and its Variability for Target 750 Ang WETOX (25 min WETOX @900C) in THERMCO1 & THERMCO3.




**Summary Statistics**

| | |
|---|---|
| Mean | 712.46667 |
| Std Dev | 33.504229 |
| Std Err Mean | 6.1170073 |
| Upper 95% Mea | 724.97735 |
| Lower 95% Mean | 699.95598 |
| N | 30 |

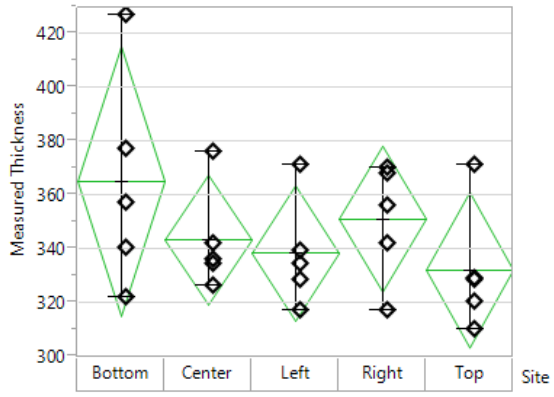
**Oxide Stripping time 4 min in 20:1 BOE (w/ overetch included).**

# APPENDIX C

## Oxide Thickness and its Variability for 300 Ang DRYOX

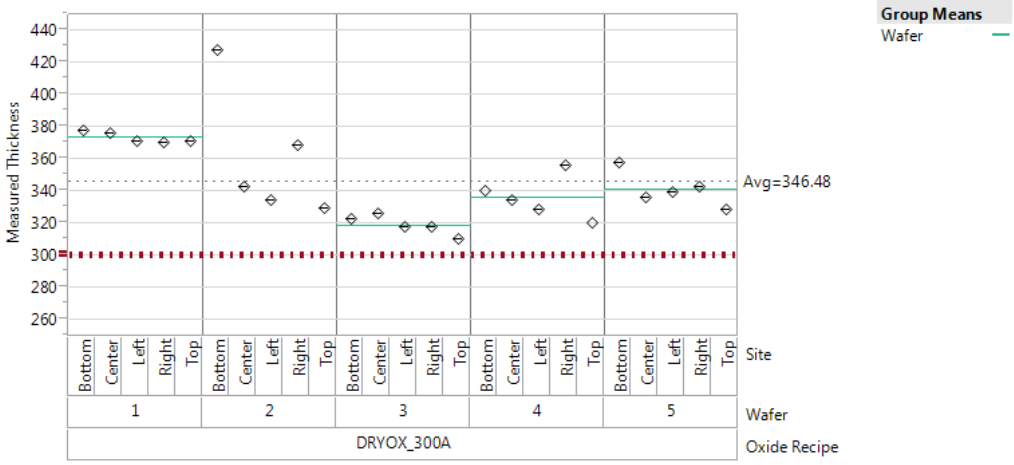
**Variability Gauge**

**Variability Chart for Measured Thickness**




**Variability Gauge**

**Variability Chart for Measured Thickness**




**Analysis of Variance**

| Source | DF | SS | Mean Square | F Ratio | Prob > F |
|---|---|---|---|---|---|
| Oxide Recipe | 0 | 0 | 0 | . | . |
| Wafer | 4 | 9124.64 | 2281.16 | 7.86512 | 0.0011* |
| Site | 4 | 3253.04 | 813.26 | 2.80401 | 0.0613 |
| Within | 16 | 4640.56 | 290.035 | | |
| Total | 24 | 17018.24 | 709.093 | | |

**Variance Components**

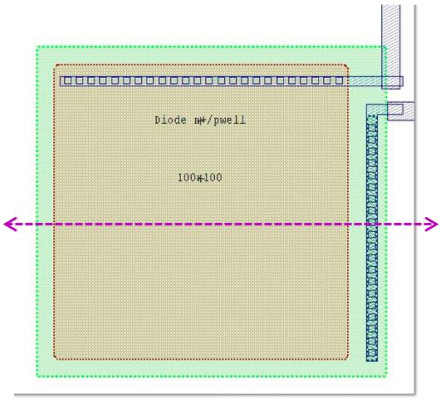
| Component | Var Component | % of Total | 20 40 60 80 | Sqrt(Var Comp) |
|---|---|---|---|---|
| Oxide Recipe | 0.00000 | 0.0 | | 0.000 |
| Wafer | 398.22500 | 50.2 | | 19.956 |
| Site | 104.64500 | 13.2 | | 10.230 |
| Within | 290.03500 | 36.6 | | 17.030 |
| Total | 792.90500 | 100.0 | | 28.159 |

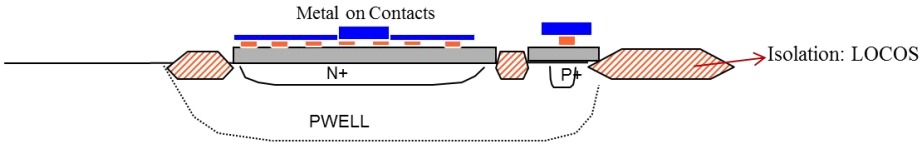
# APPENDIX D

## Device Cross-Sections with LOCOS Isolation

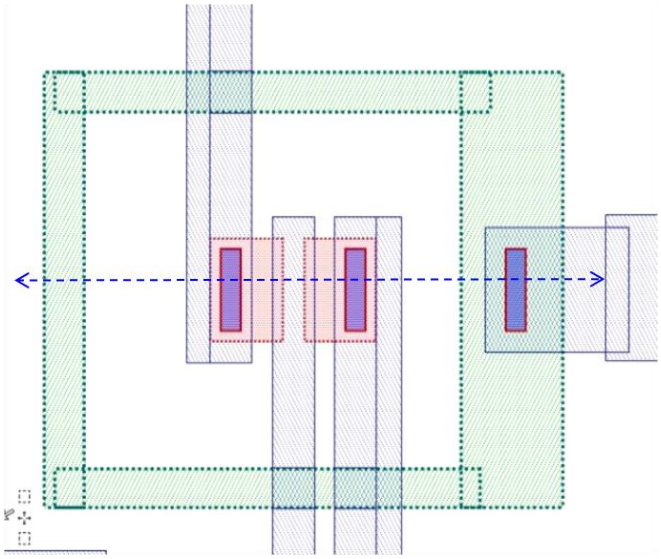
This process **do not have** any LOCOS or STI (shallow trench isolation) type field isolation. However, the device cross-sections provided below show how LOCOS would create lateral isolation between individual N+ or P+ regions.

Diode

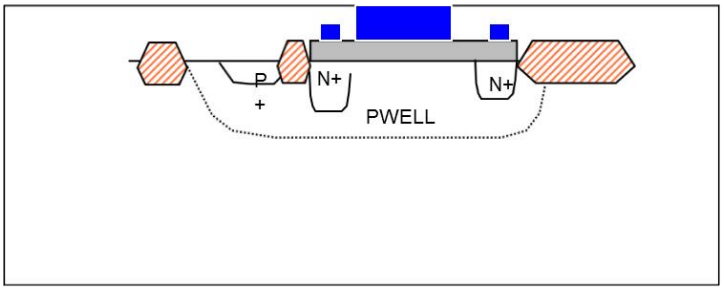



NMOS with Isolation P+ ring



Metal Gate NMOS transistor



# APPENDIX E

Test structure and test details:

| Module | Test Structure | Pads & Terminals | Test Details | Comments |
|---|---|---|---|---|
| Module 2B-1 | MOS Cap on Pwell | A2= Cap Low; Aluminum round pad= Cap High | C-V, I-V | In lack of lateral isolation, the pwell connection has a parallel capacitive path to CapHigh terminal. Structure becomes leaky. Use MOS caps in Module 1 using chuck as Cap Low. |
| | Contact Chain #1 (Size=1.5um) | A3= High; A4=Low; | I-V | Functional; results in Sec 3E |
| | Contact Chain #2 (Size=0.8 um) | A6= High; A7=Low; | I-V | |
| | Contact Chain #3 (Size=0.6 um) | A28= High; A29=Low; | I-V | |
| | | | | |
| | Diode N+/Pwell Area | A8=N+ terminal; A9=Pwell | I-V | Functional; results in Sec 3D |
| | Diode N+/Pwell Perimeter | A10=N+ terminal; A11=Pwell | I-V | Functional; results in Sec 3D |
| | | | | |
| | LNPN: Design 1 | A13=Emitter; Collector=A14; Base=A12 | Gummel; junction lkg and breakdowns | Functional but leaky & low BV; results in Sec 3C |
| | | | | |
| | Van der Pauw Sheet resistance: N+ in Pwell; | Pads: A31, A32, A33, A35 | 4 terminal I-V with Chuck grounded | functional |
| | | | | |
| | Inverter #1 | Pads: A25, A26, A37, A38 | | Not tested; needs pulse generator, oscilloscope, Voltage source. |
| | Inverter #2 | Pads: A22, A23, A40, A41 | | Not tested; needs pulse generator, oscilloscope, Voltage source. |
| Module 2B-2 | Daisy chain for flip chip | the whole pad frame for Module 2 is flip chip bonding compatible | Continuity | Physical bonding has been demonstrated; needs a separate flow than snf410 for Indium bump bond capability; separate report issued on this. |

| Module | Test Structure | Pads & Terminals | Test Details | Comments |
|---|---|---|---|---|
| Module 2B-3 | Low Voltage Transistor (LVT), Width= 2 um | Source=B1; Drain=B35; Body=B2, Gate=B36 | I-V, Vth, transconductance | functional |
| | LVT, Width= 5 um | Source=B5; Drain=B3; Body=B39, Gate=B4 | | functional |
| | LVT, Width = 10 um | Source=B9; Drain=B11; Body=B44, Gate=B10 | | functional |
| | | | | |
| | HVT, Width=2 um | Source=B6; Drain=B8; Body=B40, Gate=B7 | | functional |
| | HVT, Width=5 um | Source=B12; Drain=B15; Body=B48, Gate=B14 | | functional |
| | HVT, Width=10 um | Source=B15; Drain=B17; Body=B49, Gate=B16 | | functional |
| | | | | |
| | | | | |
| **Module 2B-4** | **MOS devices copied from Max's layout, had external ground reference pads nearby** | **external Ground pad** | | |
| | LVT, Width= 2 um | Source=B34; Drain=B32; Body=B37, Gate=B33 | | functional |
| | LVT, Width= 5 um | Source=B31; Drain=B29; Body=B38, Gate=B30 | | functional |
| | LVT, Width = 10 um | Source=B28; Drain=B27; Body=B41, Gate=B26 | | functional |
| | | | | |
| | HVT, Width=2 um | Source=B25; Drain=B23; Body=B43, Gate=B24 | | functional |
| | HVT, Width=5 um | Source=B22; Drain=B21; Body=B19, Gate=B18 | | functional |
| | HVT, Width=10 um | Source=B45; Drain=B47; Body=B18, Gate=B46 | | functional |

# APPENDIX F: Mask Details

**1X calculation WAFER LEVEL, in um**

| | Image Size in 1X ASML, um | | Image Shift in 1X ASML, um | | | MASKS | | Reticle | Fracture window coordinate | Fracture window coordinate | gds layer name in Ledit | Gds layer # | gds data type |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | X | Y | X-shift in ASML | Y shift in ASML | Layer | Digitized Data | Field | | Lower left corner | Upper Right corner | | | |
| PWELL | 8254 | 4190 | -4863 | 6400 | Implant | Clear | Opaque | SNF410A001 | (-8990.0, +4305.0) | (-736.0, +8495.0) | Pwell_implant_55 | 32 | 0 |
| PISO | 8254 | 4190 | 4863 | 6400 | IMplant | Clear | Opaque | " | (736.0, +4305) | (8990.0, +8495.0) | isolation_p | 52 | 0 |
| NSD | 8254 | 4190 | -4863 | 0 | Implant | Clear | Opaque | " | (-8990.0, -2095.0) | (-736.0, 2095.0) | sd_implant_n | 54 | 0 |
| HVT | 8254 | 4190 | 4863 | 0 | IMplant | Clear | Opaque | " | (736.0, -2095.0) | (8990.0, 2095.0) | high_vt_implant | 50 | 0 |
| CONTACT_SD | 8254 | 4190 | -4863 | -6400 | Etch | Clear | Opaque | " | (-8990.0, -8495.0) | (-736.0, -4305.0) | sd_contact_etch | 56 | 0 |
| REVERSE_METAL1 (Platinum Lift Off) | 8254 | 4190 | 4863 | -6400 | Metal Lift off | Clear | Opaque | " | (736.0, -8495.0) | (8990.0, -4305.0) | *metal_liftoff | 58 | *0* |
| | | | | | | | | | | | | | |
| | | | | | | | | | | | | | |
| | | | | | | | | | | | | | |
| | | | | | | | | | | | | | |
| | | | | | | | | | | | | | |
| METAL 1 (Etch) | 8254 | 4190 | -4863 | 6400 | Etch | Opaque | Clear | SNF4108001 | | | metal_liftoff | 58 | 0 |
| VIA410 | 8254 | 4190 | 4863 | 6400 | Etch | Clear | Opaque | " | | | Via1_ee410 | 59 | 0 |
| METAL2 (Al Etch) | 8254 | 4190 | -4863 | 0 | Etch | Clear | Opaque | " | | | metal2_ee410 | 61 | 0 |
| SBUMP_FC (Lift off process) | 8254 | 4190 | 4863 | 0 | Liftoff | Clear | Opaque | " | | | *Sbump_fc* | *20* | *0* |
| PASSIVATION_FC (wafer Coating) | 8254 | 4190 | -4863 | -6400 | Etch | Clear | Opaque | " | | | Passivation_fc | 24 | 0 |
| METAL2_FC (Lift Off) | 8254 | 4190 | 4863 | -6400 | Liftoff | Clear | Opaque | " | | | *Metal2_fc* | *22* | *0* |

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[3] Max Shulaker, "fixed_410_process_W2016_r1".. the runcard for the original process.

[4] L. V. Rozario, L. P. Sadwick, R. J. Hwu, & D. B. King, "SiC BGJFET inverter for high temperature/power applications," *High Temperature Electronics Conference*, 1998 HITEC Fourth International.

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