

Black Magic Pro 4” Graphene Furnace Development and Characterization

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1. ABSTRACT

Various emerging applications (flexible and transparent electronics, chemical sensors, thermal devices, etc.) utilizing graphene are being studied by Stanford researchers spanning multiple departments. With the recent purchase and installation of the Aixtron Black Magic Pro (BM Pro) 4” furnace, SNF users now have local access to a source of high quality graphene. In this project, we vary specific growth parameters in an attempt to improve graphene quality as well as establish reproducibility. We present Raman spectroscopy and electrical data which show that even after > 100 growths, the BM Pro yields consistently high quality, monolayer graphene.

2. INTRODUCTION

Since the first experimental demonstration of Graphene in 2005 [1], academia and industry have spent massive effort searching for an application that fully exploits the unique electrical, mechanical, and thermal properties of graphene. As of 2014, these efforts have already yielded promising results with the introduction of the first high-performance graphene-based RF transistor by IBM [2]; graphene-based transparent electrodes with higher efficiency than ITO [3]; and the first flexible e-ink display fabricated with graphene electrodes [4]. However, many graphene-based studies still utilize graphene exfoliated from bulk-graphite, limiting scalability, or rely on large-area graphene grown by CVD on cost-prohibitive substrates, such as SiC. One attractive, low cost growth solution is CVD growth on copper: a highly reproducible growth method that yields polycrystalline graphene. In this EE412 project, we utilize the new BM Pro 4” furnace in SNF and study the CVD growth of monolayer graphene on Cu. We focus our efforts on establishing highly reproducible growth recipes that yield consistently high-quality graphene at minimal user cost.

2.1 CVD Growth of Graphene

Chemical vapor deposition of graphene first involves the introduction of a carbon source (CH_4 is most common, although C_2H_2 and liquid sources have also be utilized) into an enclosed, heated environment. At sufficiently high temperature, the carbon source decomposes into various radicals, some of which travel to the catalyst surface (Process 1 in Figure 1). Upon reaching the surface, the carbon radicals react with the catalytic substrate to form graphene nucleation (Process 2,3,4,5 in Figure 1), releasing H_2 byproducts (Process 6). As the growth time increase, this reaction continues and the nucleation sites grow to form large grains of graphene. These grains eventually merge to form a continuous layer of graphene, with quality determined by growth conditions (time, temperature, pressure, and gas flow rates) as well as substrate type, cleanliness, and morphology.

If the pressure in the process chamber is sufficiently low (i.e. LP-CVD), surface-reaction kinetics will dominate, limiting growth to a highly uniform, single monolayer (“self-limiting” graphene growth) due to a combination of 1) low solid-solubility of carbon in copper and 2) the elimination of catalytic nucleation sites once a full monolayer is achieved. Note that these conditions are not specific to copper, and in fact, any substrate with sufficiently low carbon solid-solubility can be used. However, copper is readily available and relatively cheap, and is therefore most often used.

For high pressure (i.e. AP-CVD) conditions, “mass-transport” kinetics dominate, yielding graphene of varying layer count and uniformity. Resulting graphene quality is more difficult to control as small differences in substrate geometry as well as temperature will greatly affect the growth conditions. In reality, most furnaces operate in some intermediate regime between LP- and AP- growth conditions due to wildly varying growth chambers and lab conditions, with users carefully tailoring recipes in order to yield preferential mono- or multi-layer graphene growth. For this project, we focus on high-quality, monolayer graphene relevant for high-performance electronics, and therefore attempt to recreate LP-CVD growth conditions.

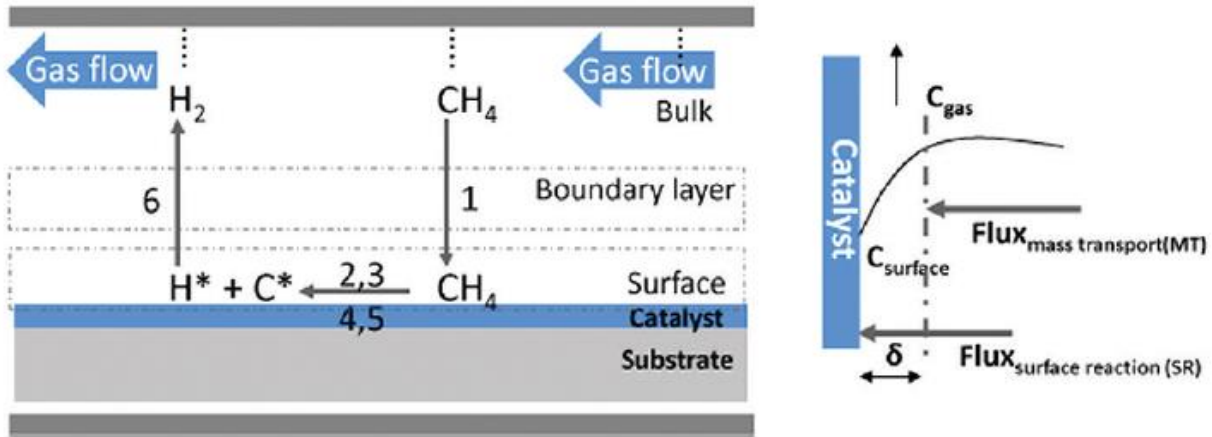


Figure 1. Processes involved in CVD graphene growth. Figure adopted from [5].

2.2 Aixtron Black Magic Pro 4” Graphene Reactor

The Aixtron Black Magic Pro CVD reactor (Figure 2) recently installed in SNF utilizes vertical showerhead gas delivery to ensure high uniformity across the growth substrate. Ar, H₂, and CH₄ gases are available. The SNF Black Magic contains both top and bottom graphite heaters to ensure uniform temperature distribution in the active growth region. Maximum growth temperature is 1100° C, limited by the melting point of the thermo-couples. In addition to the top and bottom thermocouples, the BM Pro also contains a top-mounted IR scope to measure substrate temperature (note the IR scope is calibrated to measure Si temperature and should not be used to accurately determine Cu substrate temperature during growth). Available growth pressures range from 1-25 mBarr, and the furnace is equipped with a butterfly valve to control pressure independent of gas flow. As of 2015, the furnace also contains two spare MFCs to accommodate new process gases.

As a cold-wall furnace, the Black Magic Pro minimizes copper contamination and therefore maintenance. Quartz tubes in traditional hot-wall furnaces must frequently be replaced (i.e. after

only 10 growths) as copper quickly coats the cold end of tube furnaces due to the direct sublimation of copper. Due to the cold-wall design, the BM Pro is able to conduct many high quality runs (>100 in this project) without need for major cleaning. If a clean is required, chamber maintenance is simple as all exposed surfaces are covered by protective quartz, which is easily removed and cleaned in the burn-box located right next to the furnace. Further maintenance details can be found in Appendix A.

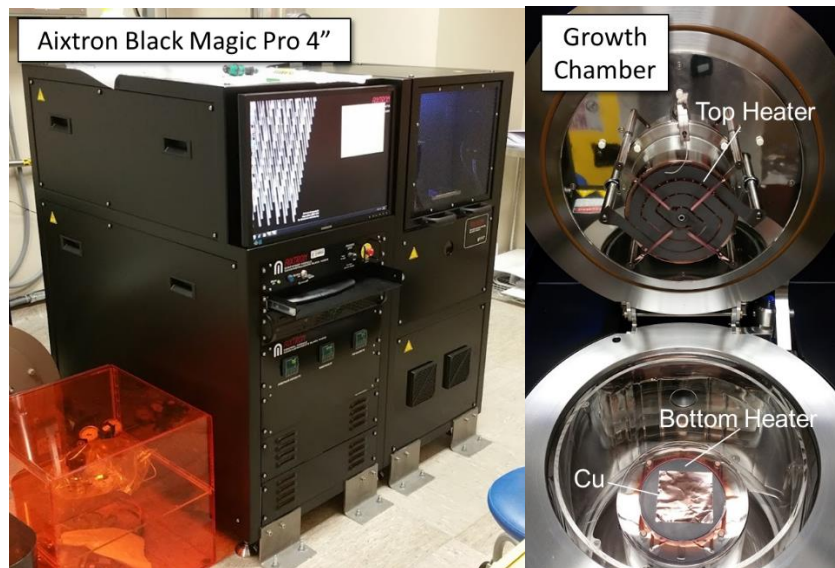


Figure 2. Left: SNF Black Magic Pro 4" Furnace. Right: Inner process chamber.

3. EXPERIMENTAL METHODOLOGY

For this project, we aimed to obtain recipes that consistently yielded large-area, high quality, monolayer graphene in the BM Pro using SNF-sourced materials. Secondary objectives were to minimize cost for SNF users and maintenance for SNF staff. All following choices in experimental methodology reflect these objectives.

3.1 Growth Parameters

To find the optimal growth recipe, a wide number of parameters were adjusted. The first choice that needs to be made is the growth substrate that is used. For the purpose of this work, the main two choices were copper foil and evaporated copper thin film on SiO₂. The details of these substrates are discussed more in Section 3.2.

Once a substrate is chosen, we tune the remainder of growth parameters for maximum quality and coverage.. The anneal and growth temperatures should be optimized in order to allow for the copper grains to coalesce and provide for higher quality growths. However, the operating range for this is limited by the properties of the substrate itself. For example, in the case of the copper thin film, temperatures higher than 1080 °C, the melting point of copper, can evaporate a significant portion of the substrate, causing the growth to be very poor. For this work, the best temperatures for each substrate were determined at the beginning of testing and held constant for the remainder of the runs.

During testing we spent most of our time varying three key parameters: growth time, CH₄ flow rate, and pressure. Given that LPCVD growth of graphene on copper should be a self-limiting process, the growth time only needs to be long enough for the film to fully form. However, we alter growth times when the flow of CH₄ is changed since the speed of nucleation and growth changes. Finally, it is important to manage the pressure such that we reach the LP condition as much as possible as opposed to atmospheric growth. If this condition is not met, growth consistency will be poor as non-idealities (i.e. substrate morphology) can occur and reduce the overall quality of the graphene.

3.2 Growth Substrates

While many growth substrates exist, we focus on Cu-based growths as the growth mechanism is well understood and Cu substrates represent a cost-quality optimum. Our initial runs used a substrate known to yield acceptable graphene quality at extremely low cost: Alfa Aesar 99.8% purity, uncoated, 0.025mm thick Cu (<http://www.alfa.com/en/catalog/46365>, \$125 for 30x1000cm in May 2015). Note that the uncoated version of this copper MUST be purchased, or the resulting growths may appear contaminated (Figure 3) as a result of the default chromium-based coating. If coated copper is purchased (whether from Alfa Aesar or another source), the coating must be removed via a gentle chemical etch in 2:1 DI:HCl or Ni-Etchant (Transene Nickel Etchant Type 1).

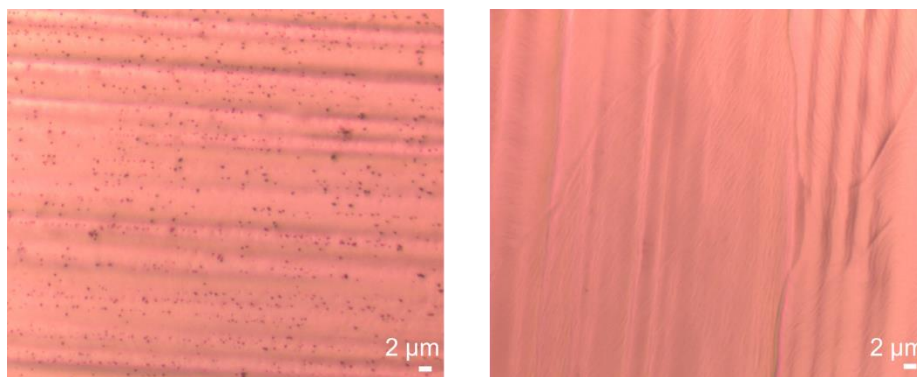


Figure 3. Uncoated vs. Coated Cu Graphene Growths

For higher quality graphene, we utilize 1) high purity (99.999%) Cu foil sourced from JX Mining Company and 2) 500-nm Cu thin-films evaporated in the SNF Innotec on 100-nm dry-oxide (grown in Thermco) on L-Test wafers. Higher-purity foil reduces the number of undesired nucleation sites, resulting in more uniform monolayer growth. In addition, the JX foil appears to have fewer large-area ripples, and we find that the more planar surface yields much better graphene morphology.

Cu-thin film substrates generally yield higher quality graphene due to a more planar surface. In addition, Cu evaporated on SiO₂ preferentially form Cu (111) grains upon high temperature anneal [6]; the Cu(111) surface has been shown to yield the highest quality graphene. Surprisingly, the thin evaporated Cu film does not completely diffuse into the SiO₂ despite exposure to high-temperature conditions (>1050 °C) present during graphene growth. We attribute this to the formation of graphitic regions at the Cu/SiO₂ interface during growth, which studies have shown to be an effective copper diffusion barrier [7].

3.3 Design of Experiment (DOE) for Foil-Based Growth Optimization

Optical images (Figure 4) on the initial copper foil growths displayed “streaks” of bilayer growth. Given that LPCVD growth of graphene on copper should be self-limiting, a number of factors were investigated. First, the copper foil used for previous growths exhibits “rolling lines” due to how it is produced. Two different treatments, one using a sulfuric-based nickel etchant and another using 2:1 H₂O:HCl were devised to attempt to eliminate these features and smooth the copper surface. Another concern was that these lines were often seen in atmospheric growths and, therefore, may be a sign that the process was not achieving sufficiently low pressures. The final point considered was that the carbon source flow was simply not optimized around the correct point so additional, lower flow rates were tried as well. To help analyze the results, the statistical software JMP was used to see if there was a statistically significant relationship between the input parameters and final results.

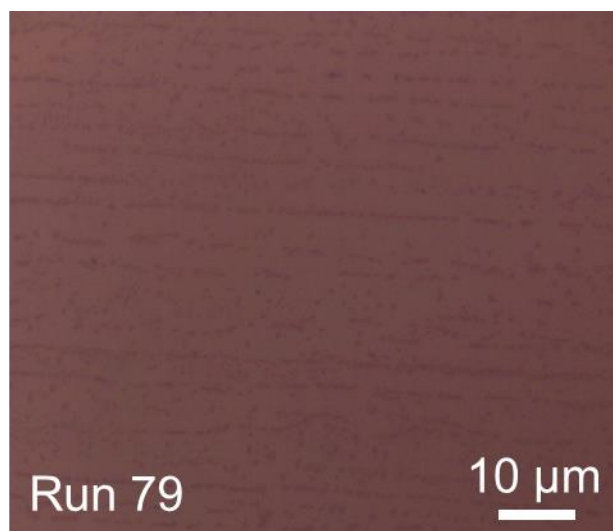


Figure 4. An example of the bilayer “streaks” that form on Cu foil growth samples

3.4 Characterization

We conducted both materials and electrical characterization of graphene in order to obtain a comprehensive assessment of graphene quality. Due to the large scope of the project, we focused on rapid assessment via Raman spectroscopy exclusively for material analysis. The highest quality growths were then used to fabricate backgated field-effect transistors, which we measured to assess electrical quality.

3.4.1 Materials Characterization: Raman Spectroscopy

Raman spectroscopy is a technique commonly used for identifying and qualifying a wide variety of novel materials. This method focuses on identifying materials based on the inelastic scattering of an incident, single-wavelength light source. The scattering event produces or annihilates a phonon of a specific energy and momentum (these are referred to as a “Stokes” or “anti-Stokes” Raman processes, respectively). The resulting photon from this event has an energy that is equal to the energy of the incident phonon reduced/increased by the energy of the

created/destroyed phonon. This energy shift can then be measured allowing for the identification of the material's phonon energies. Such a measurement on graphene results in a plot as shown in Figure 5(a).

For the purpose of qualifying graphene, three key peaks are used: D, G, and G'/2D. The process for each of these peaks varies significantly, as shown in Figure 5 (b). For the G peak, a single scattering event occurs with a zone-center in-plane transverse optical (iTO) or longitudinal optical (LO) phonon (these modes are degenerate at the Γ point). This peak, along with the 2D peak, is seen in all sp^2 bonded carbon materials. The G' peak is due to a double resonance scattering process with two iTO phonons at the K/K' point. In this case, two phonons are required due to the momentum conservation requirements ($k = 0$) of first order processes. However, when there are defects in the lattice, this mode opens up and the D peak becomes visible. This is due to the fact that these defects are localized in space allowing them to have a large range of momenta. Therefore, by scattering with a defect, conservation of momentum can be met at the K point with a single phonon.

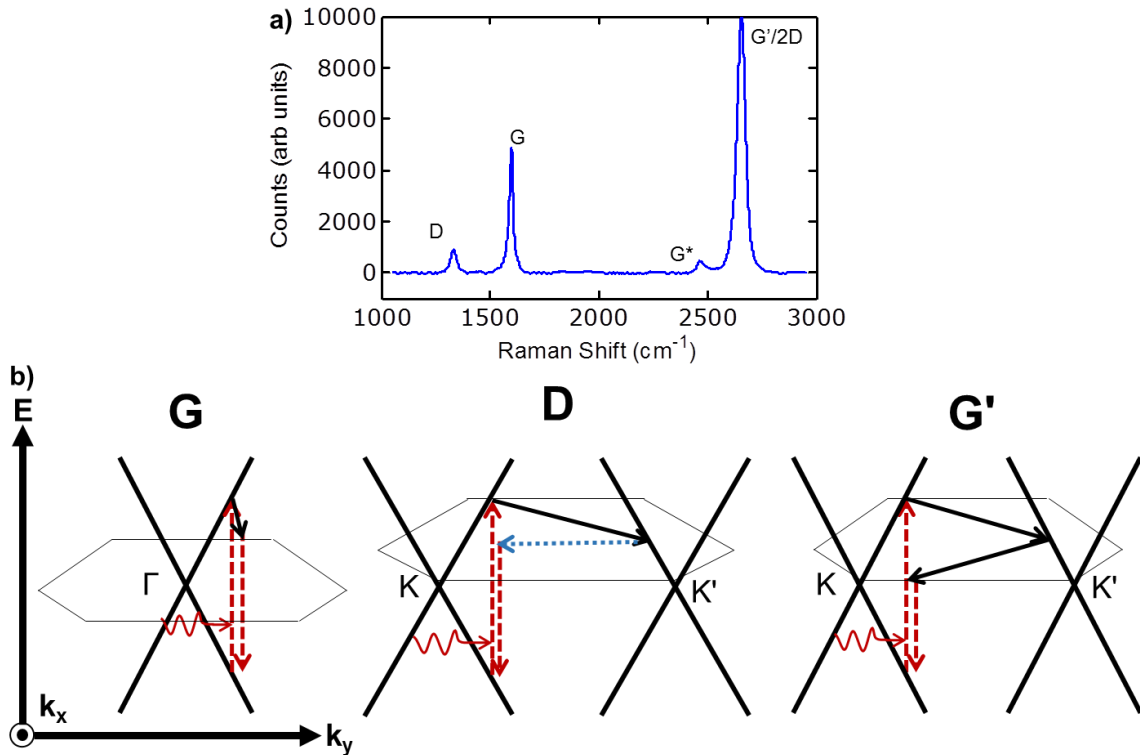


Figure 5. A typical graphene Raman spectra (a) and the mechanisms of each major peak (b). In (b), solid lines are phonons, dashed photons, and dotted defects.

As one might expect, the D peak's dependence on defects allows it to be used as a qualitative measure of defect density of a graphene sample. This is very important for quickly assessing the quality of a large number of samples. The other two previously mentioned peaks, G and G', are also extremely useful for the rapid characterization of graphene. The ratio between these two peaks is often used to identify the number of layers graphene present on a sample. For single-

layer graphene, a ratio 2:1 or greater between the G' and G peaks is expected. Therefore, for this work, “good” graphene is defined as having a minimal or no D peak while maintaining a G'-to-G ratio of >2.

3.4.2 Electrical Characterization

We conducted mass characterization of graphene devices, fabricating and measuring hundreds of 3-terminal graphene field effect transistors. We utilized a simple field-effect model implemented in MATLAB to obtain large-scale estimates of electrical mobility and contact resistance.

3.4.2.1 Graphene Transfer

Graphene must be transferred from the growth substrate for fabrication of field-effect devices. High-quality transfers are crucial for overall device performance as the process can leave behind wrinkles, tears, and/or residues that significantly affect yield as well as electrical performance. We provide here a quick summary of our transfer process, while full details can be found in Appendix B.

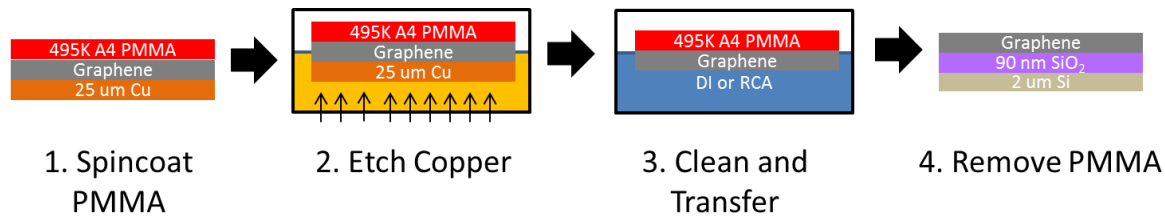


Figure 6. Modified RCA Graphene Transfer

We start by spin coating 495K A4 PMMA as a supporting scaffold (Step 1 in Figure 6). The use of PMMA is necessary to improve transfer yield as CVD Graphene itself is too weak to survive the transfer process. While other supporting films may result in cleaner transfers, PMMA-based transfers have been well characterized and are best for applications requiring high yield at reasonable cleanliness.

The PMMA/graphene/Cu stack is then placed in copper etchant (iron chloride or ammonium persulfate) overnight to remove the copper (Step 2), leaving behind a PMMA/graphene stack. Since the underlying graphene is exposed to the etchant, it must undergo a series of cleans before final transfer onto the desired substrate (Step 3). Our cleaning process is adopted from a “Modified-RCA” procedure developed at NIST [8], which uses diluted-RCA solutions to remove the metal impurities left behind by the etchant. Finally, the graphene is picked up by the final device substrate and the PMMA is removed in acetone after a gentle bake and drying.

For our device substrates, we used RCA-cleaned 90 nm SiO₂ on p++ Si (0.05 Ω-cm) from Silicon Quest International. These substrates are a cost-effective choice and have yielded high quality devices (i.e. $V_{Dirac} \approx 0$ and high electrical mobility) at reasonable cost. 90 nm SiO₂ also yields maximum contrast between graphene and SiO₂, greatly assisting optical alignment. Higher performance can be achieved with atomically thin, clean substrates (i.e. hexagonal Boron Nitride), but high quality versions of these substrates cannot be purchased, and therefore the 90 nm SiO₂ substrates are the best, easily attainable option.

Finally, we note that we also attempted the PMMA transfer for graphene grown on thin-film Cu. Since the PMMA covers the entire wafer surface, this method relies on the slow lateral etch of the Cu thin film. Unfortunately, the yield was poor as the resulting PMMA/graphene film adheres to the underlying SiO₂/Si substrate after the copper etch step. We expect other wet-etch processes will yield similar results, and future users are encouraged to experiment with dry-transfer techniques to remove the high-quality graphene off thin-film substrates.

3.4.2.2 Backgated Field-Effect Transistor (FETs)

After transfer, we fabricated 3-terminal, back-gated field effect transistors in a transfer-length-method (TLM) structure. The fabrication steps outlined in Figure 7 follow SNF standard procedures for optical lithography and are detailed here. First, we spincoat SPR3612 (~5500 RPM, 40 s, 1.2 μm) and conduct a 60-90s pre-bake at 90 °C. We then expose in KarlSuss 1 for 1.2s, postbake for 60-90s at 115 °C, and develop in MF-26A for 30 seconds, leaving behind PR only on the desired channel regions. The excess graphene is etched in Drytek 2 using 250 W O₂ plasma (150 mTorr, 100 SCCM) for 2 minutes and the PR is removed by a quick acetone wash, followed by an IPA rinse to remove any residue.

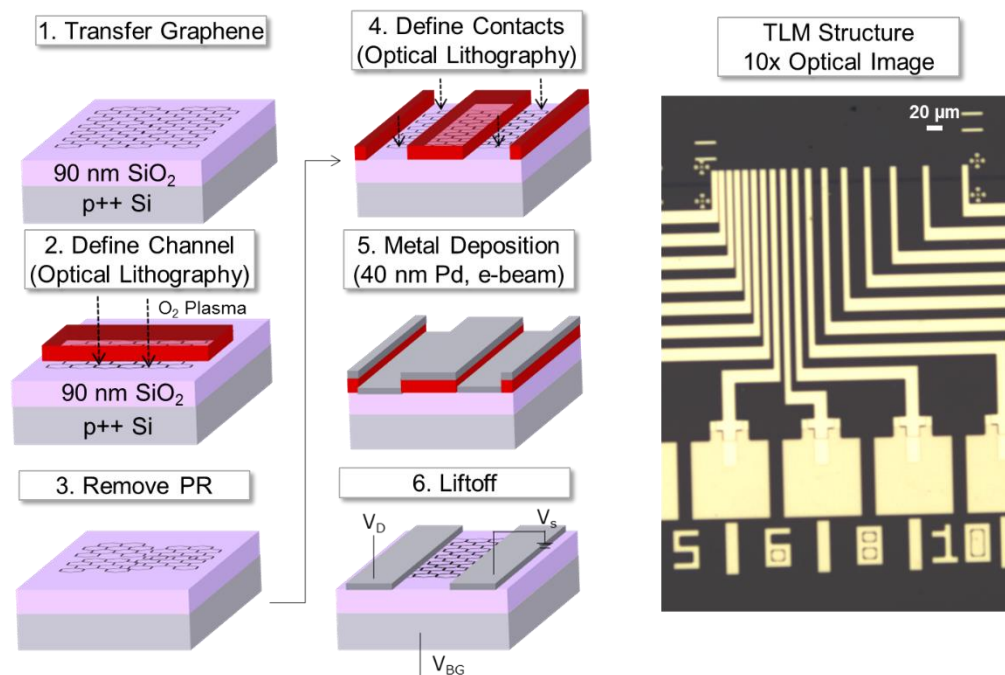


Figure 7. Fabrication Steps for Back-Gated Graphene Field Effect Transistors

We then repeat lithography to define the contacts, this time first spincoating PMGI SF6 (3000 RPM, 40s) as a liftoff layer. Based off anecdotal evidence, use of PMGI leads to lower contact resistance over LOL, presumably as the PMMA-based chemistry of PMGI leaves behind fewer residues. The PMGI is baked at 200 °C for either 35 min in whiteoven or for 10 minutes on a hotplate. The oven method is preferred for better uniformity. The rest of the lithography steps are the same as before (1.2 μm SPR3612, KarlSuss 1.2s, develop 30-40s), although extra attention was paid to development time in order to avoid overdevelopment and removal of 1 μm features. Once the graphene underneath the contact regions is exposed, we deposit 40 nm of palladium

(Pd) via e-beam evaporation (Innotec or KJL in SNC), which we then liftoff in acetone and remover PG overnight at room temperature. Note that liftoff in heated solutions are not recommended as the aggressive liftoff tends to tear and damage the graphene. Final device dimensions for EE412 are widths from 2-10 μm , channel lengths from 1-50 μm , and a contact width held at 10 μm .

Pure Pd contacts are also recommended as they consistently yield low contact resistance due to a combination of high-work function pinning and superior wetting to graphene [9]. Also, we describe here a single-step contact fabrication process where the probe pads and contact metal are the same. Separate probe pad lithography and metallization, with pads consisting of Ti/Pd and contact metal-extensions consisting of pure Pd, are suggested in order to yield pads more robust to repeated probing (Pd only pads scratch incredibly easily) while maintaining low contact resistance.

3.4.2.3 Mass Device Characterization

To rapidly estimate mobility and contact resistance, we use MATLAB to fit the low-field measurements to the following model developed by the Pop research group[10, 11]:

$$(1) R_{d,fit} = \frac{L}{W} R_s + 2R_c + R_{series}$$

where R_s is the bias-dependent sheet resistance of the graphene, R_c is the bias-dependent graphene-to-metal contact resistance, and R_{series} is the lead resistance (in our case as high as 400 Ω due to the extremely long contact extensions). The sheet resistance is given by:

$$(2) R_s = \frac{1}{q\mu_0(n+p)}$$

where q is the elementary charge (1.6×10^{-19} C), μ_0 is the effective mobility, and n and p are the electron and hole carrier concentrations, respectively. Carrier concentration are bias-dependent, with n given by :

$$(3) n = \frac{1}{2} \left[n_{cv} + \sqrt{n_{cv}^2 + 4n_{ip}^2} \right]$$

The equation for p follows a similar form. From the equation, we see that the overall carrier concentration results from electrostatic doping ($n_{cv} = C_{ox}(V_{dirac} - V_{bg})/q$) as well as impurities ($n_{ip} = \sqrt{(n_0/2)^2 + n_i^2}$), which can further be subdivided into contributions from substrate impurities (n_0) as well as thermally activated carriers ($n_i = \pi/6 \times k_B T^2 / \hbar v_F$, [12]). Contact resistance is given by:

$$(4) R_c = \frac{1}{W} \frac{\rho_c}{L_T} \coth \left(\frac{L_c}{L_T} \right)$$

which simplifies to $\sqrt{\rho_c R_s}$ when $L_c \gg L_T = \sqrt{\frac{\rho_c}{R_s}}$.

To extract contact resistance and mobility, we fit low-field I_d - V_{bg} measurements into Eq. 1 and all sub-equations following the flowchart outlined in Figure 8 below:

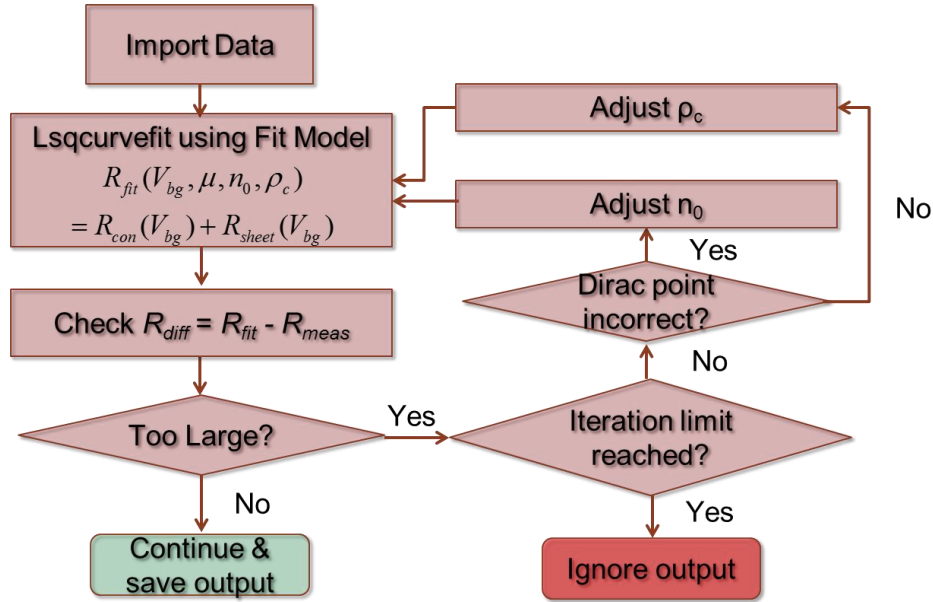


Figure 8. Flow-chart for Electrical Data Extraction

While Eq. 1-4 contain several variables, only carrier mobility (μ_0), substrate impurity concentration (n_0), and specific contact resistivity (ρ_c) are necessary to determine total device resistance at a specific backgate voltage. As such, the algorithm outlined in Fig. 8 starts with initial guesses for these values. The resulting R_{fit} generated using a least-squared approximation is then compared to the original R_{meas} , and the final values are saved only if the resulting error is $< 5\%$. If not, the script runs through a series of checks to see where the discrepancy occurs, and makes the proper adjustment to the next iteration of fit values. If a proper fit is not determined within a certain amount of iterations, a warning is displayed and the output is ignored. All final values, including contact resistance, mobility, Dirac voltage, and impurity concentration, are saved to output Excel files at a specified directory for later batch processing. Since the code is internal to the Pop group, it is not yet adequately documented or particularly user-friendly. Therefore, it will not be released to the general SNF community, although interested users are welcome to ask the authors for the code or implement their own version of the algorithm.

4. Results and Discussion

The results of over 100 growths (both foil and thin-film based) are discussed here, as well as the electrical results of devices fabricated on the two best runs (Run 65 and Run 80).

4.1 Initial Growths

Initial recipes for the Black Magic Pro 4” were provided by Aixtron SE’s technical support and were the starting point for this work. As seen in Fig. 9, these recipes provided a decent baseline for the tool, but have some significant non-idealities. For the foil growths, it is important to note that while there appears to be good, uniform coverage across the sample, Raman spectroscopy shows there is a significant amount of defects. Inversely, the growth on thin films show poor coverage, but no sign of defects. Finally, the initial runs were performed mostly on Aixtron provided substrates meaning additional testing on materials that could be sourced for SNF (see Section 3.3 for more details on the substrates used) was needed.

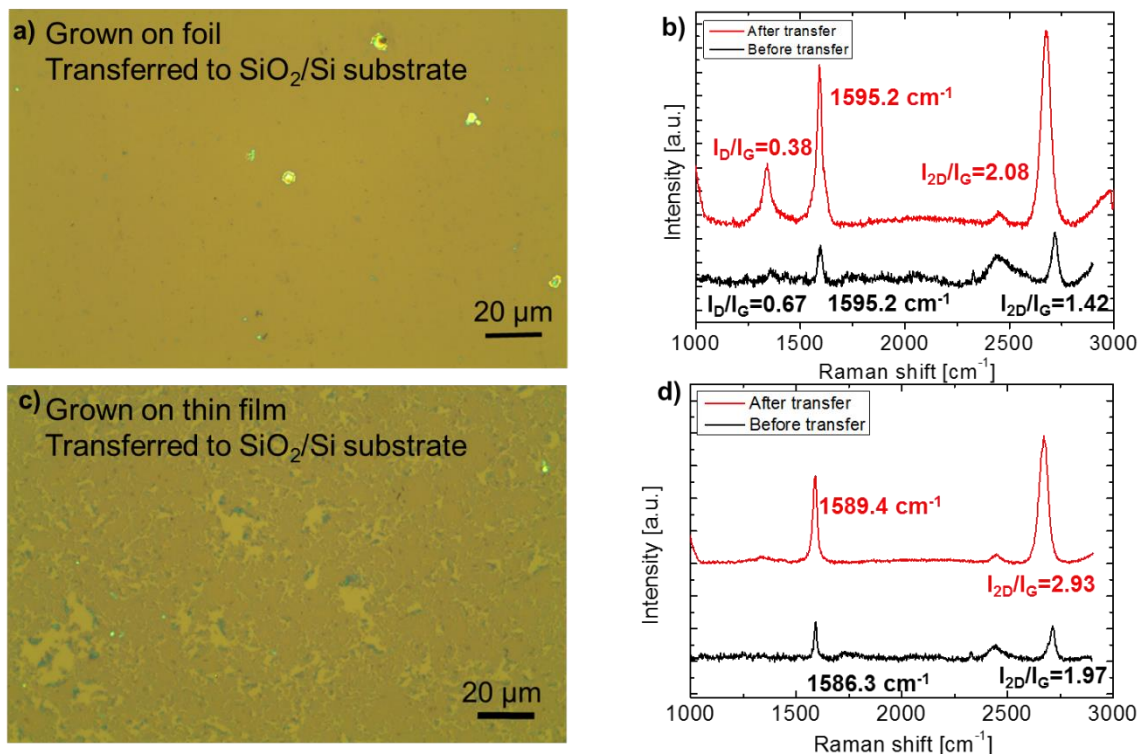


Figure 9. Optical images (a,c) and Raman spectra (b,d) of graphene grown using Aixtron provided recipes

4.1.1 Foil-Results

As stated in the previous section, the main goal for the foil growths was to lower the overall defects density (as shown by the D peak) while maintaining the uniform coverage. Towards this goal, a temperature sweep was done from 1030 C to 1060 C. Optimal growth was found to occur with an operating temperature of 1050 C, therefore, this was used for the remainder of the runs. In addition to this, a number of growths were performed with increasing growth and anneal times. However, as seen from SEM (Figure 10), the growth time needed for complete coverage is rather low (60 seconds for SEMs versus 7.5 minutes in the baseline growths). Therefore, growth time was left at the baseline level. Some improvement was seen with the longer anneal times (30 minutes versus 7.5 minutes baseline), so this has been set as the base recipe for now.

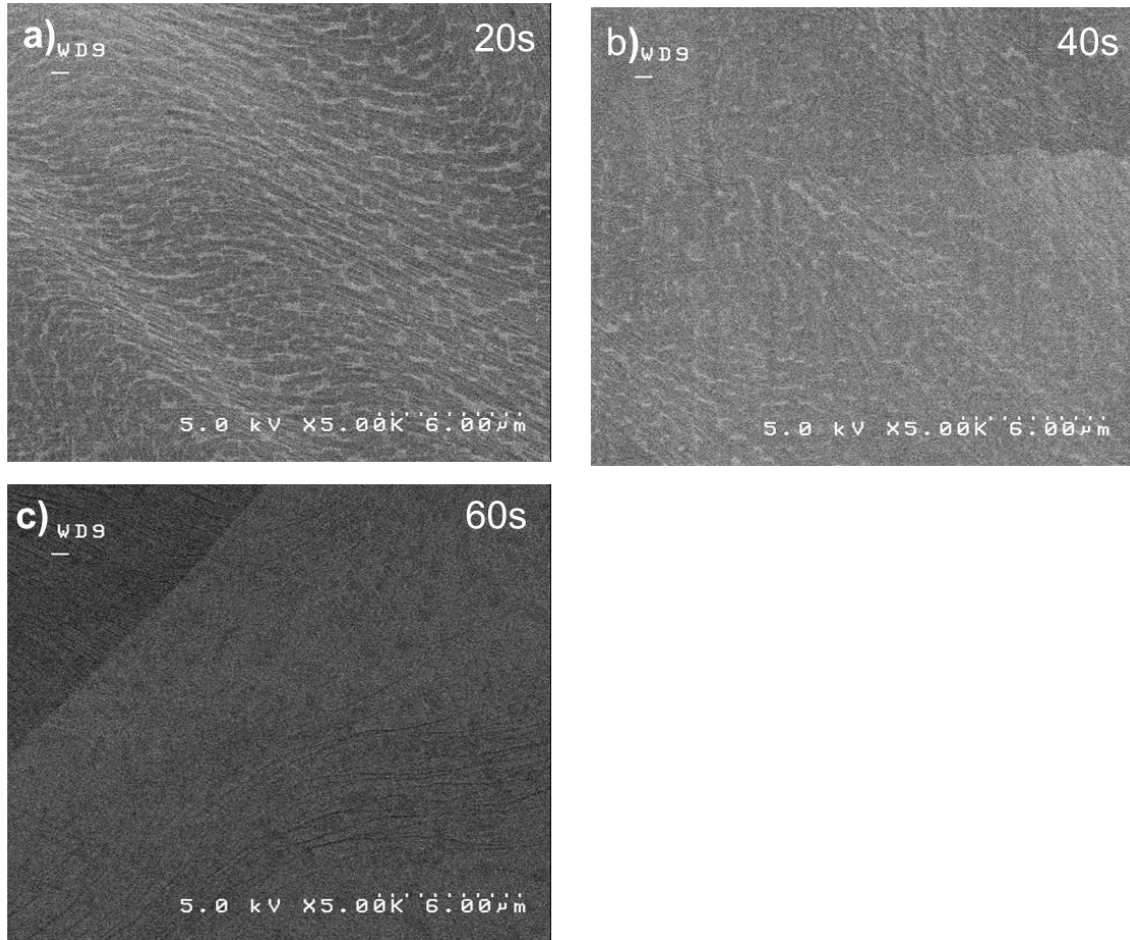


Figure 10. SEM images of graphene with growth times of 20 seconds (a), 40 seconds (b), and 60 s (c). Here we note that by 60 seconds, the grains have coalesced to form a complete layer.

4.1.2 Thin-film

In order to improve the coverage for thin film growths, both the methane flow rate and growth time were increased. As shown in Figure 11(a), a wide range of growth times and flow rates were tried. However, prior to the last growth (60 sccm CH₄ and 40 minute growth time), the top heater broke and had to be replaced. Given that the Raman data (Figure 11(b)) for this last point does not appear to be a significant outlier, it was concluded that this change did not significantly impact the growth. Overall, it appears that the best solution to improving uniformity while maintaining a high quality growth is to simply increase the growth time. This allows for the individual grains to finish growing and coalesce without harming the overall quality of the film.

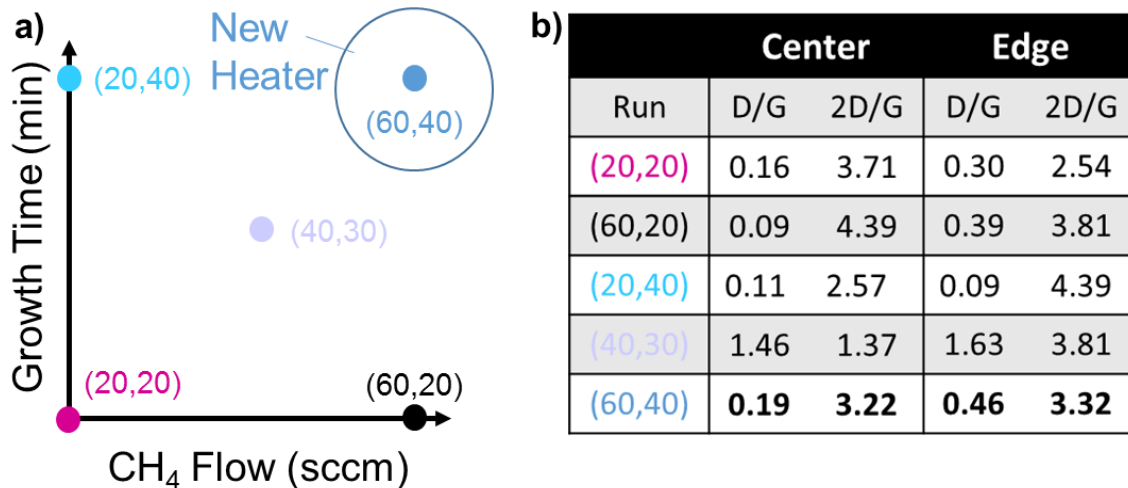


Figure 11. The initial experiment setup (a) and resulting data (b) for the set of thin film runs. Note that edge and center refer to the position on the transferred portion, not the growth substrate

4.1.3 DOE Results

After finishing the growth sessions for the set of runs determined by JMP (see Section 3.2 for details on why these parameters were chosen), the results were tabulated (Fig 12(a)) and processed (Figure 12(b-d)). From these results it can be noted that there is simply not enough data to prove that there is a statistically significant relationship between our input parameters and the density of defects. Because of this, it was decided that additional data points should be taken in order to provide a better understanding of the data. However, due to the Raman spectroscopy tools being down for an extended period of time, these measurements could not be taken. Overall, while it appears that there may be dependence of the defect density on the pressure, more work needs to be done to statistically validate this trend.

From optical microscopy (Figure 13), we see a relationship between the density of the lines and the etchant used. The samples treated by the Ni etchant seemed to be noticeably better than those that underwent the HCl treatment. This is attributed to the fact that the Ni etchant attacks the copper much more vigorously allowing it to better remove the rolling lines in the foil. However, as there were still a significant number of bilayer regions, additional measures needed to be taken to remove them completely.

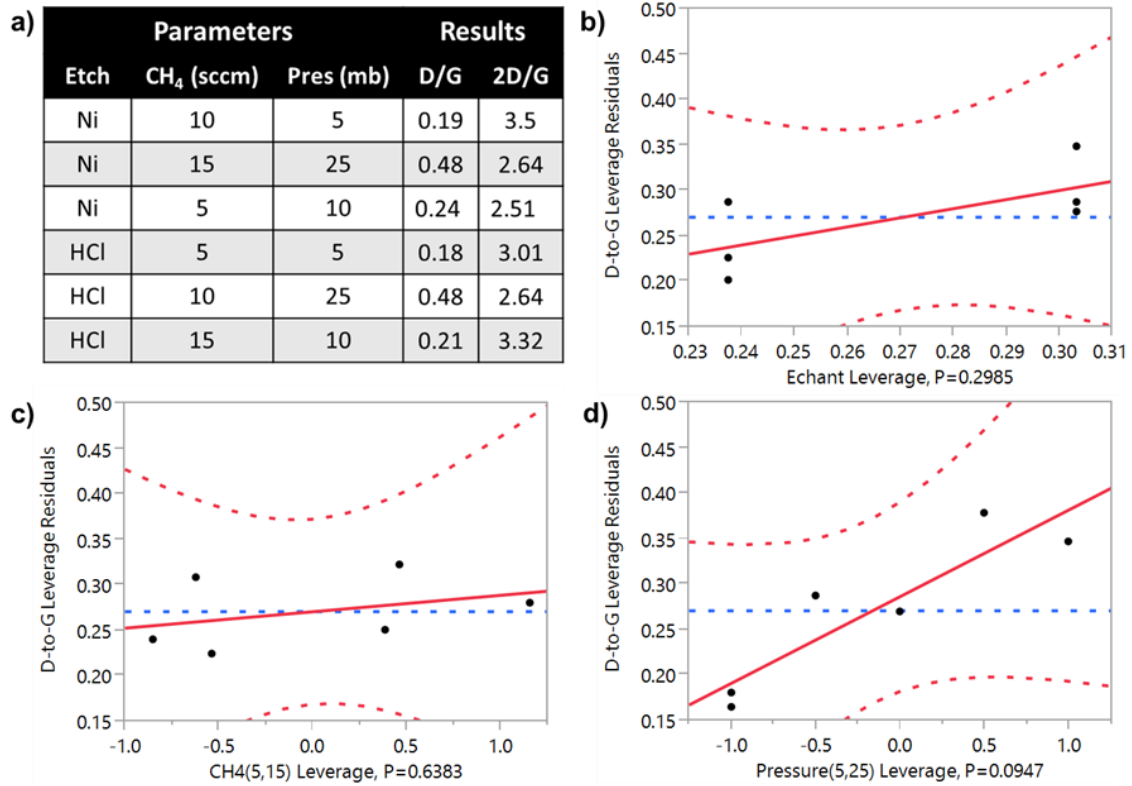


Figure 12. The experimental setup and results (a) are shown along with data fittings (b-d) from JMP. While $P < 0.05$ is generally set as the requirement for rejecting the Null, pressure seems to show a trend.

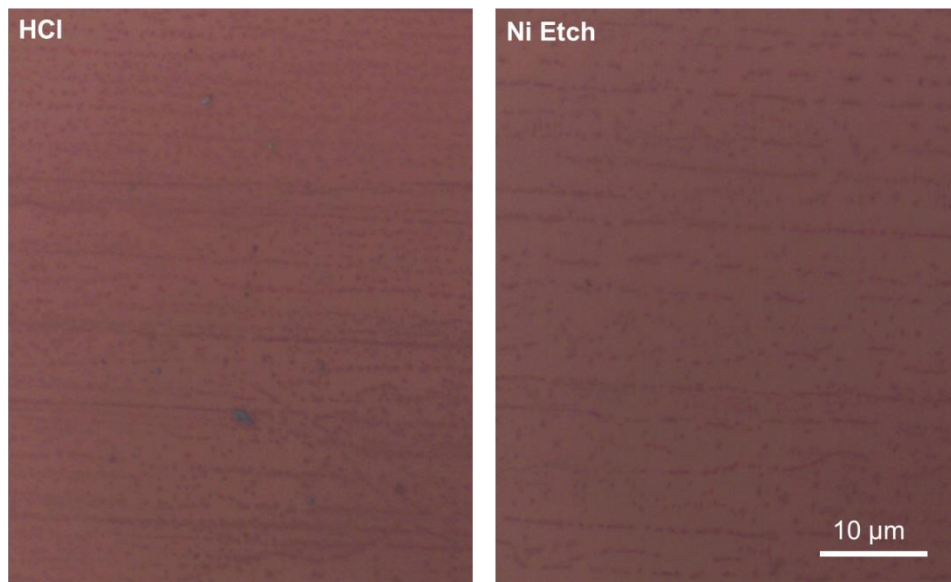


Figure 13. Samples treated with HCl (left) tend to have a higher density of bilayer “streaks” than those that underwent the Ni etch.

4.1.4 High Quality Results (Yong-Cheol's Community Service Growths)

Noting the results of the previous foil runs, a number of changes were made for the “high quality” run attempts. In order to minimize atmospheric-like growth conditions, argon flow was eliminated. This led allowed us to reach the lowest possible pressures while still flowing all the gases necessary for growth. Additionally, high purity, ultra-smooth copper foil was treated in long (>12 hour) acetic acid treatment to remove any possible morphology related effects.

By using these conditions, we were able to obtain a graphene sample that showed no signs of bilayer regions (Figure 14) along with a complete lack of D peak (Figure 15). This demonstrates that the tool is not the limiting factor in these growths; rather, significant investment in both substrate acquisition and preparation is required to achieve high quality results. However, the current source for this substrate is also not commercially available making it difficult to provide SNF with an accessible source for this method.

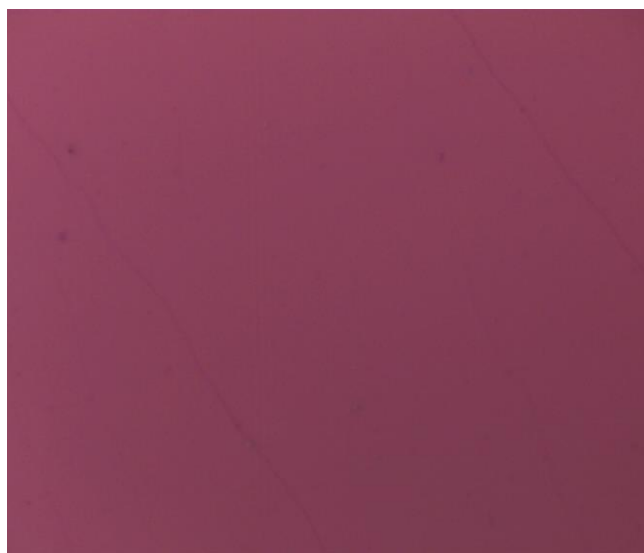


Figure 14. Unlike the previous growths, there are no “streaks” on the high quality samples.

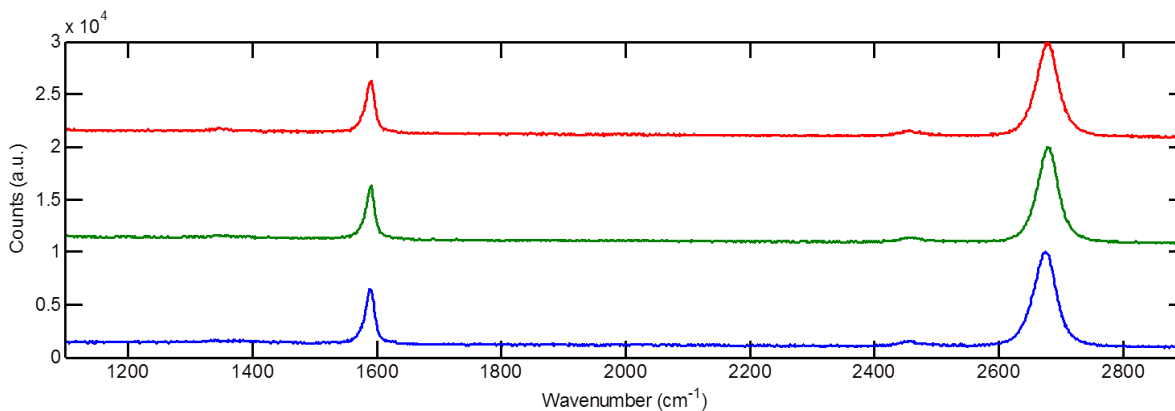


Figure 15. Raman data from multiple spots on Run 65 showed little or no D peak demonstrating the high quality of the film.

4.2 Electrical Results

All electrical measurements were conducted in the Janis vacuum probe station located in Allen 152 (Figure 16) at a base pressure of $\sim 5 \times 10^{-5}$ Torr following a 2 hr vacuum anneal at 400 °C to improve graphene-contact adhesion and reduce contact resistance. Measurements in vacuum are also ideal to minimize oxygen doping, which can severely p-dope graphene.

Initial low-field measurements for two sets of devices are shown in Fig and demonstrate the importance of using clean metal sources for contact metallization. The first device fabricated using Innotec for metallization, where the Pd source appeared visibly contaminated, exhibits unacceptable hole transport when compared to the second device fabricated using a clean Pd source in the Lesker in Allen 111X.

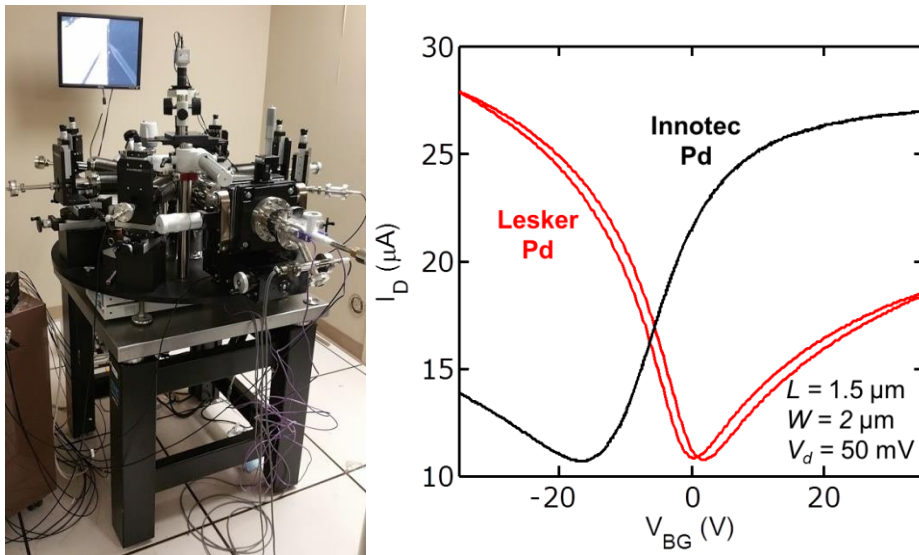


Figure 16. Left: Janis vacuum probe station (located in Allen 152) used for measurements. Right: I_d vs V_{BG} for GFETs fabricated with Lesker and Innotec sourced metallization. Run 80 graphene was used for both devices.

For the second set of devices fabricated using the Lesker, we were also able to compare the results of a typical graphene growth (Run 80 with Alfa Aesar foil) with a high quality growth (Run 65 with JX foil) to demonstrate the impact of extra sample preparation.

The average growth demonstrates good electrical behavior typical of clean, high quality graphene (singular Dirac point with relatively high drive current). However, from a comparison of $L = 1.5 \mu\text{m}$ devices, we already see a drastic improvement in both mobility (as evidenced by a steeper slope) as well as contact resistance (as evidenced by the higher drive current at high gate bias), indicating that graphene quality is not necessarily dictated by the recipe and/or growth conditions, but rather by the amount of user effort toward sample preparation and choice.

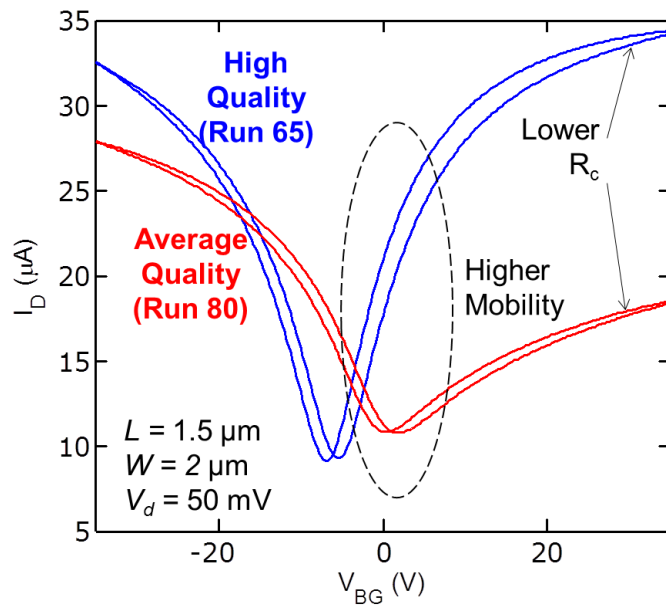


Figure 17. I_d vs V_{BG} for Average vs. High Quality Graphene

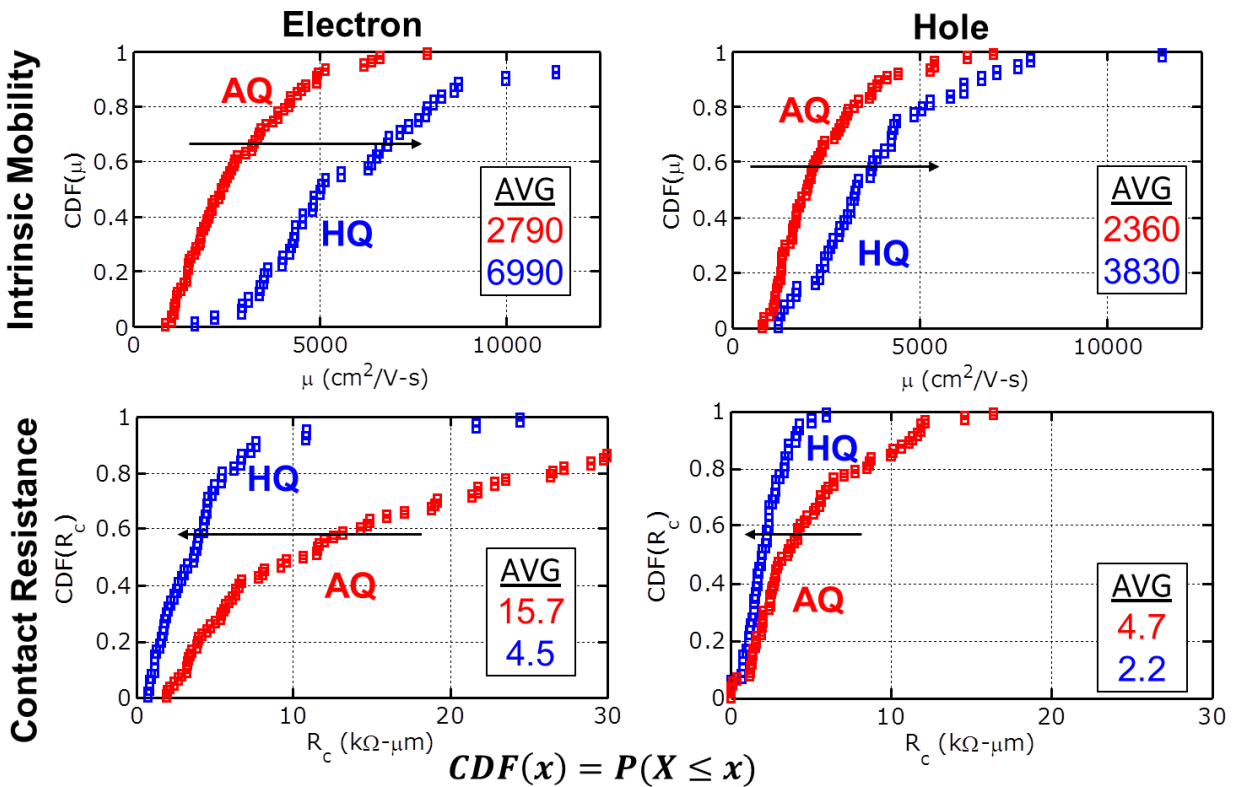


Figure 18. Cumulative Distribution Functions for AQ (Run 80) and HQ (Run 65) Graphene FETs

Using the fit code outlined in section 3.4.2.3, we fit the low-field measurements of hundreds of devices from $L = 1-50 \mu\text{m}$ and $W = 2-10 \mu\text{m}$ to generate large-area statistics of performance (Figure) The statistics affirm the conclusions drawn from the single device analysis, with average

electron mobility improving from 2790 to 6990 $\text{cm}^2/\text{V}\cdot\text{s}$ and hole mobility improving from 2360 to 3830 $\text{cm}^2/\text{V}\cdot\text{s}$. Average hole and contact resistance improve as well, with electron contact resistance dramatically improving from 15.7 to 4.5 $\text{k}\Omega\cdot\mu\text{m}$. Finally, average substrate impurity concentration, a measure of graphene uniformity and cleanliness, improves from 3.2×10^{-11} to 2.1×10^{-11} cm^{-2} , more likely as a result of improved uniformity rather than cleanliness since the transfer processes used were similar. The high-quality graphene however, is curiously doped n-type as exhibited by a Dirac voltage less than 0—we attribute this due to a difference in substrate preparation as the substrate used for Run 65 devices did not undergo standard RCA clean. This treatment appears to leave a cleaner surface as exhibited by the Dirac point closer to zero for devices from Run 80. In general, users are advised to use highly uniform, high purity growth substrates to yield high quality graphene due to the APCVD like growth conditions.

4.2.1 Contact Resistance Limitations

High contact resistance can be extremely detrimental for scaled devices as the contact resistance dominates of channel resistance at high biases. For Run 80, the effect is so severe that on/off ratio sharply degrades for $L < \sim 3$ μm (Figure 19) as the ability to drive further current in the graphene at short channels is increasingly limited by the contact resistance.

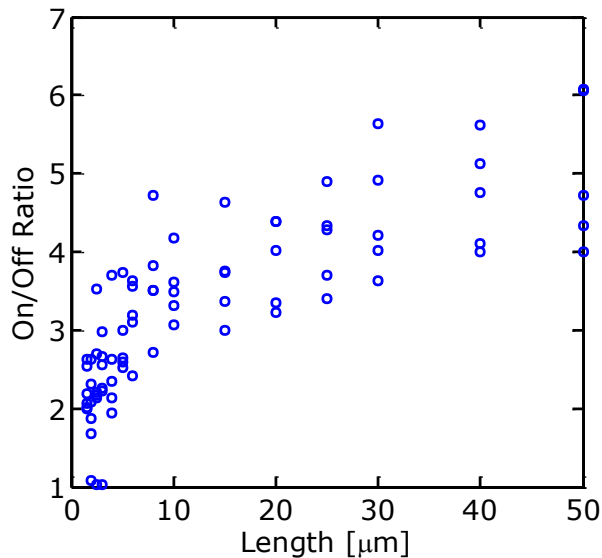


Figure 19. On/Off ratio vs. Channel Length for Run 80 devices. Devices based off other graphene runs exhibit similar trends.

Two factors contribute to contact resistance: 1) the sheet resistance of the material underneath the contact and 2) the contact-semiconductor interface. While the improved electrical transport of our HQ graphene should help 1), the contact resistance is still high at 4.5 $\text{k}\Omega\cdot\mu\text{m}$ for electron transport and 2.2 $\text{k}\Omega\cdot\mu\text{m}$ for hole transport. The lower hole contact resistance is expected as Pd is a high work function metal that theoretically should provide no barrier to hole injection. In fact, both hole and electron contacts are ohmic—the I_d vs. V_d curves shown in Figure 20 show a linear dependence. Thus, the contact-semiconductor interface is *not* the limiting factor since no Schottky behavior is observed. Instead, to lower contact resistance, the sheet resistance underneath the graphene must be improved, whether by doping or some other novel method, or the contact must make greater use of edge-injection, which has been shown to yield lower

specific contact resistance than top-facing contacts [13]. Either method has yet to be explored at Stanford with graphene and SNF users are encouraged to pursue one as a future EE412 project.

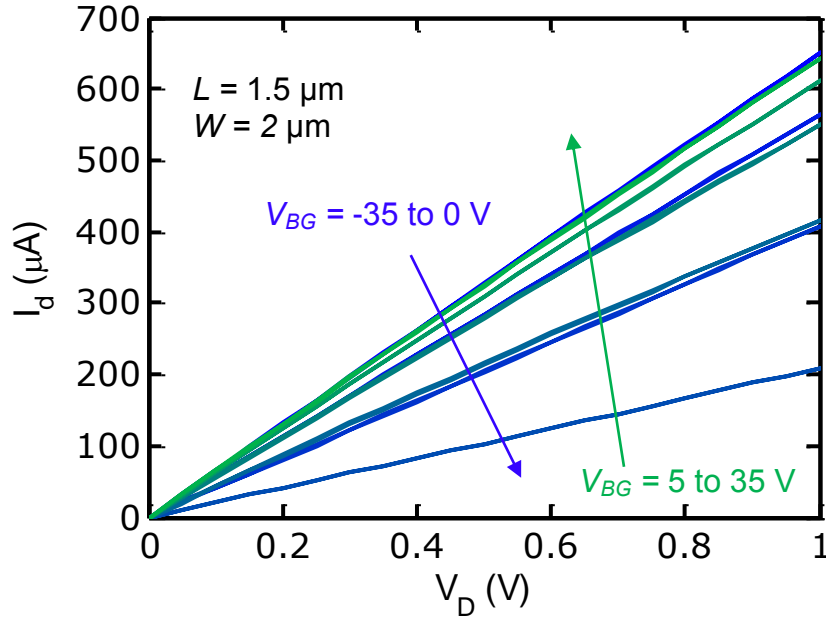


Figure 20. I_d vs V_d for Run 65, HQ Graphene FET.

5. Conclusion

After over 100 growths, we have established a reliable, reproducible recipe for generating large area, high-quality monolayer graphene in the Black Magic Pro Furnace. Initial runs showed dramatic improvement by increasing anneal time to allow formation of larger copper grains and greater impurity removal. However, further improvement was not straightforward—growth conditions were revealed to be APCVD like despite the supposedly low pressures. Subsequent DOEs further confirmed the influence of pressure, and we were able to greatly reduce defects by 1) lowering growth pressure as much as possible and 2) using high purity, smooth substrates and conducting further substrate pre-treatment to ensure highly planar surfaces.

We fabricated hundreds of backgated FETs and conducted extensive electrical characterization that confirm the high electrical quality of the graphene produced in the Black Magic Pro. However, the graphene quality will be determined by the user, and *not* the tool recipes—our results have shown that users can expect either average quality (AQ) or high quality (HQ) graphene depending on sample preparation. The results of our findings are summarized below:

Table 1. Summary of Results

Type	Cu Purity	Grain Size (μm)	μ_e ($\text{cm}^2/\text{V-s}$)	μ_h ($\text{cm}^2/\text{V-s}$)
AQ	99.8%	0.5-1	~ 2800	~ 2300
HQ	99.999%	>10	~ 6900	~ 3800

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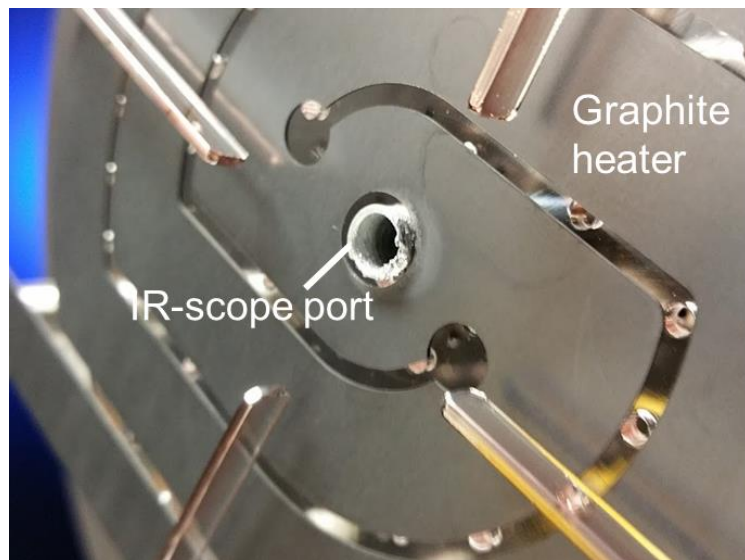
Appendix A: Maintenance Notes

1. Common issues: Throughout the project, we encountered several interlock trips that caused the tool to shutdown unexpectedly. These scenarios and their solution are detailed below:

- a. IR Temperature Interlock

Unfortunately, this interlock stems from two unrelated problems (the first of which should have been fixed permanently, but the fix effectiveness has yet to be determined). With the details provided, it will be up to the superuser to determine which problem is the culprit by checking the log or visually inspecting the chamber.

PROBLEM: Top heater in contact with IR tube, resulting in a path to ground that shorts the top-heater. IR tube then heats due to arc-discharge, resulting in measured temperature >1100 °C. This occurs over-time as the heater warps due to repeated high-temperature processing, eventually coming in contact with the IR tube.



SOLUTION: We tried several fixes, including adjusting the heater position before each run. However, shortening the IR tube to completely prevent contact with heater seems to be the permanent solution. This fix was implemented at the end of May, 2015 and thus the IR tube should no longer be shorting, but the effectiveness of the fix has yet to be determined.

PROBLEM: Recipe contains a step where Ar flow suddenly increases at high temperatures (> 1050 °C). In this case, the sudden influx of Ar cools the chamber, resulting in the top-heater rapidly increasing power to compensate. Measured substrate surface temperature via Ir scope suddenly increase above safe setpoint of 1100 °C.

SOLUTION: Ramp up process gases slowly (i.e. with 200 SCCM increments over 20 seconds). Also implemented FURNACEPOWER mode, which restricts top heater power to a certain percentage of the bottom heater. Superuser is advised to contact Aixtron for more details on this mode as it is not a default function and was added in by Ken Teo (Aixtron VP of Nanomaterials) in early 2015 and requires extra checks at the beginning of each recipe to ensure the top-heater is configured correctly.

b. Extraction Interlock

PROBLEM: Exhaust flow (directly out of chamber, NOT out of pump) is too low, causing the interlock sensor (extraction sensor) to trip.

SOLUTION: Open the exhaust gate (located near the roof) to allow more flow. As of May 2015, the meter is reading 0.5 and works fine.

c. Gas Valves Off

PROBLEM: The BM Pro does not contain internal checks to verify that process gases are flowing. As such, previous recipes would continue with the temperature ramp to growth temperatures in vacuum. This results in massive copper contamination in the chamber in a single growth, and should be avoided.

SOLUTION: Wait commands were inserted at the beginning of recipes to ensure that the recipe does not progress if no gas flow is present by checking to make sure the pressure rises due to the influx of gases during purge steps.

2. **Suggested Maintenance:** Throughout the Spring 2015 quarter, over 100 growths were conducted (see EE412 documentation for more details). Despite the accumulation of copper and carbon contamination in the chamber seen below, the furnace surprisingly generated high quality graphene. As such, we believe the chamber is well seasoned and advise against frequent cleaning, which can alter growth conditions and lower reproducibility.



Figure A1. Chamber conditions after ~70 runs.

However, since high quality growths cannot continue indefinitely, bi-annual cleaning is recommended. This involves removing all quartz liners (bottom heater, top heater, top shield, and chamber liner) and conducting a chemical etch to remove the residue copper on surfaces followed by an oven bake at 1000 C overnight to remove carbon contamination. To minimize user impact, spare quartz ware should be installed while the previous quartz-ware is cleaned (and therefore becomes the new spare). In fact, 3 sets of quartz-ware at all times is ideal: one set which is installed and in use, one spare for swapping in during cleans, and a second spare in case one component breaks during clean. This will ensure that the tool is up and running nearly 24/7 with minor interruption.

3. Non-Standard Growths:

Users are also advised to purchase their own quartzware if they plan to do any nonstandard (i.e. anything other than Cu, Ni) growths. Such growths must be approved by superusers, and will only be allowed if the growths can be proven to not affect regular growth recipes. The use of separate quartzware in this case will help to mitigate any potentialcross contamination.

Appendix B: Suggested Graphene Transfer Technique (Foil-Based Growths)

1. Prepare graphene piece:

- a. Cut desired piece of Cu from the growth substrate.
- b. Spin 495K A4 PMMA @ 2000 RPM. **Note this resist thickness has not been optimized; alternative PMMA weights and/or thickness might yield cleaner interfaces and/or fewer wrinkles.**
- c. Bake @ 80 C for 10 minutes in oven. Alternatively, bake @ 200 C for 2 minutes. First method is likely more gentle and cleaner, but might not fully cure the PMMA.

2. (OPTIONAL) Remove Backside Graphene:

- a. Etch backside graphene w/ oxygen plasma in Drytek 2. Settings: 100 sccm O₂, 150 mTorr, 250 Watts, 120 s

3. Etch Copper:

- a. Place foil in copper etchant (FeCl₃ most common, but can also use Ammonium Persulfate which might be cleaner) for at least 8 hrs.

4. Transfer onto Substrate: Two types of cleans can be conducted prior to transfer of graphene onto final substrate: Modified RCA and DI water rinse. The modified RCA clean is suggested for FeCl₃-based transfers since the RCA clean can remove some of the residual iron from the etchant [1].

a. Modified RCA Transfer:

- 1 After copper is completely removed 'wick' graphene and supporting membrane from solution using a glass slide (Piranha cleaned recommended) or substrate into D.I. rinse. Recommended: leave overnight for thorough clean. Otherwise, let stand for > 10 mins.
- 2 Transfer the graphene from water to SC-2 (20:1:1 H₂O:H₂O₂:HCl) solution. Let stand for > 10 mins.
- 3 Transfer from SC2 to water. Let stand for about 10 min.
- 4 Transfer the graphene from water to SC-1 (20:1:1 H₂O:H₂O₂:NH₄OH) solution. Let stand for > 10 mins.
- 5 Transfer from SC1 to water. Let stand for > 10 mins.
- 6 'Wick' graphene and supporting membrane from D.I. rinse onto substrate.
- 7 Let stand until D.I. water evaporates (> 1 hour usually for 2 x 2 cm sample, recommended overnight). Then place on a hot plate at low temperature (< 60 C) for 30 minutes or more to evaporate water. Alternatively, you can drive off water by placing on hot plate @ room

temperature and ramping to 150° C. Warning: this last alternative method may introduce more tears, however it seems to work so far at Stanford using the solvent plate in 111x.

8 Remove PMMA: Place in acetone for 30 minutes.

b. DI Water Rinse Transfer:

1 After copper is completely removed ‘wick’ graphene and supporting membrane from solution using a **glass slide (recommended, Piranha cleaned)** or substrate into D.I. rinse. **Recommended: leave overnight for thorough clean.** Otherwise, let stand for > 10 mins.

2 Transfer graphene from water to fresh DI water bath using glass slide.

3 Repeat step 2 as desired.

4 ‘Wick’ graphene and supporting membrane from D.I. rinse onto substrate.

5 Let stand until D.I. water evaporates (> 1 hour usually for 2 x 2 cm sample, **recommended overnight**). Then place on a hot plate at low temperature (< 60 C) for 30 minutes or more to evaporate water. Alternatively, you can drive off water by placing on hot plate @ room temperature and ramping to 150° C. **Warning: this last alternative method may introduce more tears, however it seems to work so far at Stanford using the solvent plate in 111x.**

6 Remove PMMA: Place in acetone for 30 minutes.

5. **OPTIONAL:** Anneal graphene in furnace under forming gas (Ar/H₂) ambient @ 400C to remove some residual PMMA. **Note that this will not completely remove the PMMA and may actually slightly damage the graphene if any residual oxygen is present.**