2017 SNF410-Depletion Mode NMOS (Option PWell) Flow Run Sheet: Lot ID:_____

STEP 0.00 - PHOTOMASK #0- ZERO LEVEL MARKS

Starting materials is **P**-type silicon (5-10 ohm-cm). Add four test wafers labeled T1-T6. T1 and T2 are litho test wafers and will travel with the device wafers and get all of the processing steps except implants. T3 will be added at Gate Ox to be used for thickness measurements and for etch rate determination. T4-T6 are for implant test wafers, one each for the implant steps. For Zero Level Marks, all device wafers are processed, plus T1 and T2. Use T1 and T2 to optimize focus and exposure.

STEP 0.05 – CLEAN

Piranha Clean in **wbnometal -** 120°C; 10min; Dump rinse; SRD

Date _____ Time_____ Operator_____

STEP 0.10 - SINGE & PRIME

yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments_____

STEP 0.15 - SPIN COAT RESIST

Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).

System used: ❑***svgcoat2 (Preferred)*** ❑***svgcoat***

Date_____ Time _____ Operator _____

Comments_____

STEP 0.20 – Spin Rinse Dry

All device wafers plus T1 and T2; Inspect backside of wafers for particles/ resist, clean w/ q-tip if needed prior to SRD

LithoSRD
Date_____ **Time** _____ **Operator** _____
Comments_____

STEP 0.25 – NON-ALIGNED EXPOSURE

Expose using ASML stepper:
Job name: /lrozario/SNF410_2
Layer ID: ZERO
Layer Number: ZERO
Image ID: 45023981A009
Reticle ID: Combi Reticle (ASML)

Exposure used:_____**70** mJ_____

Date _____ Time _____ Operator _____

Comments_____

STEP 0.35 – POST EXPOSE BAKE

Bake using SVG Dev track, bake program 1 (bake only)

System used: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments_____

Comments: _____

STEP 0.30 - RESIST DEVELOP& Scribe

Develop using SVG Dev track, develop program 3 (develop) and bake program 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Scribe:
Hand-scribe wafers on the front side near one edge of the flat away from the zero marks.

Comments_____

STEP 0.35 – VISUAL INSPECTION

Visual microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

Comments_____

REWORK DONE? ❑***yes*** ❑***no***

Wafers reworked: _____
If yes, attach REWORK sheet here.

STEP 0.40 – ALIGNMENT MARK SILICON ETCH

All device wafers plus T1 and T2.

P5000, Chamber C, Program: "Poly Etch", Etch time= 40 sec
Pre-season: 10:00min;

Date_____ Time _____ Operator _____

Comments_____

STEP 0.45 - RESIST ASH

All device wafers plus T1 and T2

gasonics, recipe sequence 014

Date_____ Time _____ Operator _____

Comments_____

STEP 0.50 – STANDARD RESIST STRIP

All device wafers plus T1 and T2

wbnonmetal, Piranha @ 120°C, 20', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

Measure step height on two alignment marks on T1 or T2 (Spec 1200+/-200A)_____ _____

STEP 0.55 - STANDARD PRE-DIFFUSION CLEAN

All device wafers plus T1 ,T2 & T3 . The wafers should be loaded straight into oxidation furnace after performing these cleans.

Wbclean-1 or -2,
5:1:1 H2O:H2O2:NH4OH @ 50°C, 10'; dump rinse;
50:1 DI:HF @ Room Temp, 30 sec; dump rinse, spin dry
5:1:1 DI:H2O2:HCl @ 50°C, 10'; dump rinse;
~~50:1 DI:HF @ Room Temp, 30 sec; dump rinse, spin dry~~

Date _____ Time _____ Operator _____

2017 SNF410-Depletion Mode NMOS (Option PWell) Flow Run Sheet: Lot ID:_____

***** STEP 0.561 – Pad Oxide for PWell Mask -Thermal Oxidation – Target – 750 Ang**
Only Pwell Option wafers + 2 Test Wafers
Temperature = **900C**
Time = **0:25:00** hrs:mins:sec
Thermco1: **Recipe: "3WETOX" @ Thermco3**

Date _____ Time _____ Operator _____

Oxide Growth Time: _____

Comments: _____

*****STEP 0.562 –THICKNESS MEASUREMENT**
Use Woollam, WVASE program ------ to measure the oxide thickness and uniformity on T3.

Oxide: T_____ C_____ B_____ R_____ L_____

Thk % Uniformity:_____

Comments_____

*****STEP 0.563 - PHOTOMASK #1- for PWELL Implant**

All PWELL option wafers plus T1 and T2. Use T1 and T2 to optimize focus and exposure.

*****STEP 0.564 - SINGE & PRIME**
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments_____

*****STEP 0.565 - SPIN COAT RESIST**
Apply 1 micron of 3612 positive resist w/o VP 2mm EBR only, using SVG Coat track programs 7 (coat and softbake).

System used: ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date_____ Time _____ Operator_____

Comments_____

*****STEP 0.566 – Spin Rinse Dry**
All device wafers plus T1 and T2
Inspect backside of wafers for particles and resist residue & clean prior to SRD

LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

*****STEP 0.567 - ALIGNED EXPOSURE**
Expose using ASML stepper:
Job name: /lrozario/SNF410_2
Layer ID: PWELL_IMP Layer Number: 1
Image ID: PWELL_IMP
Reticle ID: SNF410A001

Focus Used: __0_____ Exposure used:__ 70 mJ_____

Date _____ Time _____ Operator _____

Comments_____

*****STEP 0.568 – POST EXPOSE BAKE**
Bake using SVG Dev track, bake program 1 (bake only)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments _____

*****STEP 0.569 - RESIST DEVELOP**
Develop using SVG Dev track, develop program 3 (develop) and bake program 1 (bake).

System used: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator_____

Comments_____

*****STEP 0.570 - RESIST HARDENING (for implantation)**

Hard bake 30 mins @ 110C.

Date _____ Time _____ Operator _____

Comments_____

*****STEP 0.572 – VISUAL INSPECTION**
Visual and microscope inspection. Check for defects, alignment and exposure quality.
Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

REWORK DONE? ❑***yes*** ❑***no***

Wafers reworked: _____
If yes, attach REWORK sheet here.

*****STEP 0.573 –PWELL Implant**
All PWELL option wafers plus Test wafers

Species: B_{11}^{+}; Dose: 2.5E13; Energy = 180 keV; 7 deg tilt

Date _____ Time _____ Operator _____

Comments _____

*****STEP 0.574 - RESIST ASH**
All device wafers plus T1 and T2

gasonics, recipe sequence " 014"

Date_____ Time _____ Operator _____

Comments_____

2017 SNF410-Depletion Mode NMOS (Option PWell) Flow Run Sheet: Lot ID:_____

*****STEP 0.575 – STANDARD RESIST STRIP**
All device wafers plus T1 and T2

wbnonmetal, Piranha @ 120°C, 20', dump rinse, spin dry
Date_____ Time _____ Operator _____

Comments_____

*****STEP 0.576 - STANDARD PRE-DIFFUSION CLEAN**
All optional Pwell wafers plus Test wafers . The wafers should be loaded straight **into diffusion furnace** after performing these cleans.

Wbclean-1 or -2,
5:1:1 H2O:H2O2:NH4OH @ 50°C, 10'; dump rinse;
50:1 DI:HF @ Room Temp, 30 sec; dump rinse, spin dry
5:1:1 DI:H2O2:HCl @ 50°C, 10'; dump rinse;
~~50:1 DI:HF @ Room Temp, 30 sec; dump rinse, spin dry~~

Date _____ Time _____ Operator _____

Comments_____

*****STEP 0.577 – PWELL DRIVE-IN**
All optional PWELL wafers plus Test wafers
Temperature = 1100°C Nitrogen
Time = 02:00:00 (2 hours)
Furnace: Thermco1: recipe: "1ANNEAL"

Date _____ Time _____ Operator _____

Oxide Growth Time: _____

Comments: _____

*****STEP 0.578 – OXIDE THICKNESS MEASUREMENT POST DRIVE-IN**
Use Woollam, WVASE program ------ to measure the oxide thickness and uniformity on Test Wafer.

Oxide: T_____ C_____ B_____ R_____ L_____

Thk % Uniformity:_____

Comments_____

*****STEP 0.579 – PAD OXIDE STRIP**

All PWELL option wafers plus Test Wafers.

Oxide WET Strip; **20:1 BOE Etch**; Time: 4:00 minute

STEP 0.59 - STANDARD PRE-DIFFUSION CLEAN
All device wafers plus T1 ,T2 & T3 . The wafers should be loaded straight into oxidation furnace after performing these cleans.

Wbclean-1 or -2,
5:1:1 H2O:H2O2:NH4OH @ 50°C, 10'; dump rinse;
50:1 DI:HF @ Room Temp, 30 sec; dump rinse, spin dry
5:1:1 DI:H2O2:HCl @ 50°C, 10'; dump rinse;
~~50:1 DI:HF @ Room Temp, 30 sec; dump rinse, spin dry~~
Date_____ Time _____ Operator _____

Comments _____

**** AFTER THIS STEP OPTIONAL PWELL FLOW WILL MERGE WITH CORE DEPLETION NMOS FLOW. ALL STEPS ARE IDENTICAL TO EE410 FLOW AFTER THIS****

Comments_____

STEP 0.60 – Thermal Oxidation – Target - 30nm
All device wafers plus T1, T2 & T3.
Temperature = 900°C
Time = 2 hr 34 min @ Thermco1
Thermco1: 1DRYOX

Date _____ Time _____ Operator _____

Oxide Growth Time: _____

Comments: _____

STEP 0.7 –THICKNESS MEASUREMENT
Use Woollam, WVASE program ------ to measure the oxide thickness and uniformity on T3.

Oxide: T_____ C_____ B_____ R_____ L_____

Thk % Uniformity:_____

Comments_____

STEP 1.00 - PHOTOMASK #1- Isolation P+ Implant

All device wafers plus T1 and T2. Use T1 and T2 to optimize focus and exposure.

STEP 1.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments_____

STEP 1.20 - SPIN COAT RESIST
Apply 1 micron of 3612 positive resist w/o VP 2mm EBR only, using SVG Coat track programs 7 (coat and softbake).

System used: ❑***svgcoat2 (preferred)*** ❑***svgcoat***

Date_____ Time _____ Operator_____

Comments_____

STEP 1.25 – Spin Rinse Dry
All device wafers plus T1 and T2
Inspect backside of wafers for particles and resist residue & clean prior to SRD

LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

2017 SNF410-Depletion Mode NMOS (Option PWell) Flow Run Sheet: Lot ID:_____

STEP 1.3 - ALIGNED EXPOSURE
Expose using ASML stepper:
Job name: /lrozario/SNF410_2
Layer ID: LAYER2 Layer Number: 2
Image ID: PISO_IMP

Focus Used: __0_____ Exposure used:__**70mJ**_____

Date _____ Time _____ Operator _____

Comments_____

STEP 1.35 – POST EXPOSE BAKE
Bake using SVG Dev track, bake program 1 (bake only)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments _____

STEP 1.4 - RESIST DEVELOP
Develop using SVG Dev track, develop program 3 (develop) and bake program 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator_____

Comments_____

STEP 1,45 - RESIST HARDENING (for implantation)
Hard bake 30 mins @ 110C.

Date _____ Time _____ Operator _____

Comments_____

STEP 1.6 – VISUAL INSPECTION
Visual and microscope inspection. Check for defects, alignment and exposure quality.
Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

REWORK DONE? ❑***yes*** ❑***no***

Wafers reworked: _____
If yes, attach REWORK sheet here.

STEP 1.70 – P+ Isolation Implant
All device wafers plus T3 & T5

Species: B_{11}^{+}; Dose: 5E15; Energy = 60keV; 7 deg tilt

Date _____ Time _____ Operator _____

Comments _____

STEP 1.8 - RESIST ASH
All device wafers plus T1 and T2

gasonics, recipe sequence 017

Date_____ Time _____ Operator _____

Comments_____

STEP 1.9 - STANDARD RESIST STRIP
All device wafers plus T1 and T2

wbnonmetal, Piranha @ 120°C, 20', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 2.00 - PHOTOMASK #2- Arsenic Source/Drain N+ Implant

All device wafers plus T1 and T2. Use T1 and T2 to optimize focus and exposure.

STEP 2.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments_____

STEP 2.20 - SPIN COAT RESIST
Apply 1 micron of 3612 positive resist w/o VP and back-side EBR only, using SVG Coat track programs 7 (coat and softbake).

System used: ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date_____ Time _____ Operator_____

Comments_____

STEP 2.25 – Spin Rinse Dry -All device wafers plus T1 and T2
Inspect & clean backside of all wafers for particles/ resist residue

LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

STEP 2.30 - ALIGNED EXPOSURE
Expose using ASML stepper:
Job name: lrozario/SNF410_2
Layer ID: LAYER3 Layer Number: 3
Image ID: NSD_IMP
Reticle ID: SNF410A001

Focus Used: __0_____ Exposure used:__**70**mJ_____

Date _____ Time _____ Operator _____

Comments_____

STEP 2.35 – POST EXPOSE BAKE
Bake using SVG Dev track, bake program 1 (bake only)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments_____

2017 SNF410-Depletion Mode NMOS (Option PWell) Flow Run Sheet: Lot ID:_____

STEP 2.40 - RESIST DEVELOP
Develop using SVG Dev track, develop program 3 (develop) and bake program 1 (bake)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments_____

STEP 2.45 – HARD BAKE
Oven Bake: 110C, 30 min

Date _____ Time _____ Operator _____

Comments: _____

STEP 2.60 – VISUAL INSPECTION
Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

Comments_____

STEP 2.7 – Souce/Drain N+ Implant -
All device wafers plus T3 & T4.

Implant Services: 7 deg. tilt, 60 keV, As75, $2x10^{15}$ cm^{-2}

Date_____ Time _____ Operator _____

Comments _____

STEP 2.8 - RESIST ASH
All device wafers plus T1 and T2

gasonics, recipe sequence 018

Date_____ Time _____ Operator _____

Comments_____

STEP 2.9 - STANDARD RESIST STRIP
All device wafers plus T1 and T2

wbnonmetal, Piranha @ 120°C, 20', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 2.95 - RESIST ASH
All device wafers plus T1 and T2

gasonics, recipe sequence 017

Date_____ Time _____ Operator _____

Comments_____

STEP 3.00 - PHOTOMASK #3 – High VT Implant
All device wafers plus T1 and T2. Use T1 and T2 to optimize focus and exposure.

STEP 3.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments_____

STEP 3.20 - SPIN COAT RESIST
Apply 1 micron of 3612 positive resist w/o VP, back-side EBR only, using SVG Coat track programs 7 (coat and softbake).

System used: : ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date _____ Time _____ Operator _____

Comments _____

STEP 3.25 – Spin Rinse Dry -All device wafers plus T1 and T2
Inspect and clean backside for particles and resist residues

LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

STEP 3.3 - ALIGNED EXPOSE
Expose using asml stepper:
Job name: lrozario/SNF410_2
Layer ID: LAYER4 Layer Number: 4
Image ID: HVT_IMP
Reticle ID: SNF410A001

Date _____ Time _____ Operator _____

Exposure used:_____**70**mJ_____

Comments_____

STEP 3.35 – POST EXPOSE BAKE
Bake using SVG Dev track, bake program 1 (bake only)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments_____

STEP 3.4 - RESIST DEVELOP
Develop using SVG Dev track, programs 3 (develop) and 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____ Time _____ Operator _____

Comments_____

STEP 3,45 - RESIST HARDENING (for implantation)
Hard bake 30 mins @ 110C.

Date _____ Time _____ Operator _____

Comments_____

2017 SNF410-Depletion Mode NMOS (Option PWell) Flow Run Sheet: Lot ID:_____

STEP 3.55 – VISUAL INSPECTION
Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

Comments _____

REWORK DONE? ❑***yes*** ❑***no***

Wafers reworked: _____
If yes, attach REWORK sheet here.

STEP 3.6 – High Vt IMPLANT (P)
All device wafers plus T3 & T6.

Species: B_{11}^{+} ; Dose: 1E13; Energy = 60keV; 7 deg tilt

Date _____ Time _____ Operator _____

Comments _____

STEP 3.8 - STANDARD RESIST STRIP
All device wafers plus T1 and T2

wbnonmetal, Piranha @ 120°C, 20', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 3.85 - RESIST ASH
All device wafers plus T1 and T2

gasonics, recipe sequence 013

Date_____ Time _____ Operator _____

Comments_____

STEP 3.86 - STANDARD PRE-DIFFUSION CLEAN
All device wafers plus T1 ,T2 & T3 . The wafers should be loaded straight into oxidation furnace after performing these cleans.

Wbclean-1 or -2,
5:1:1 H2O:H2O2:NH4OH @ 50°C, 10'; dump rinse;
50:1 DI:HF @ Room Temp, 30 sec; dump rinse, spin dry
5:1:1 DI:H2O2:HCl @ 50°C, 10'; dump rinse;

Date _____ Time _____Operator _____

STEP 3.90 – Anneal
Temperature = 1000°C
Time = 00:20:00 (20 minutes)
Furnace: Thermco1: recipe: "1ANNEAL" Nitrogen

Date _____ Time _____ Operator _____

Comments: _____

STEP 4.00 - PHOTOMASK #4 – CONTACT
All device wafers plus T1,T2. Use T1 and T2 to optimize focus and exposure.

STEP 4.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments_____

STEP 4.20 - SPIN COAT RESIST
Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).

System used: : ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date _____ Time _____ Operator _____

Comments _____

STEP 4.25 – Spin Rinse Dry- All device wafers plus T1 and T2
Inspect and clean backside for particles and resist residues

LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

STEP 4.30- ALIGNED EXPOSE
Expose using asml stepper:
Job name: lrozario/SNF410_2
Layer ID: LAYER 5
Layer Number: 5
Image ID: CONTACT_SD
Reticle ID: SNF410_A001

Date _____ Time _____ Operator _____

Exposure used:_____**70mJ**_____

Comments_____

STEP 4.35 – POST EXPOSE BAKE
Bake using SVG Dev track, bake program 1 (bake only)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments_____

STEP 4.40 - RESIST DEVELOP
Bake using SVG Dev track, programs 3 (develop) and 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____ Time _____ Operator _____

Comments_____

STEP 4.45 – DESCUM

Drytek 2, Program 1
Season Drytek 2 for 5 min with conditions described below before loading wafers. Process wafers for 20 sec
150mT, 100 sccm O2, 150W power.

Only use the clean shelves.

Date _____ Time _____ Operator _____

2017 SNF410-Depletion Mode NMOS (Option PWell) Flow Run Sheet: Lot ID:_____

STEP 4.50 - VISUAL INSPECTION
Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

Comments _____

REWORK DONE? ❑***yes*** ❑***no***

Wafers reworked: _____
If yes, attach REWORK sheet here.

STEP 4.60- PLASMA OXIDE ETCH
All device wafers.

P5000, Chamber B; Recipe: surromed; Time: 160s;
Run preconditioning with the same recipe for 300sec.
Verify etch rate on blanket SiO2 wafer before processing. Etch time will vary.

Date _____ Time _____ Operator _____

Comments_____

STEP 4.65 - RESIST ASH

gasonics, recipe sequence 014

Date_____ Time _____ Operator _____

Comments_____

STEP 4.7 STANDARD RESIST STRIP
All device wafers plus T1 and T2. Add T3 at this point for SiO2 thickness measurement.
wbnonmetal, Piranha @ 120°C, 20', Dump rinse; wet transfer to 50:1 HF bath for 20 sec. etch.

Date_____ Time _____ Operator _____

50:1 HF dip, Room temp, 20sec, Dump rinse, SRD

Date_____ Time _____ Operator _____

Comments_____

SiO2 Thickness on T3 after HF Dip:
T_____ C_____ F _____ L_____ R _____

In case, the wafers need rework:
wbnonmetal, Piranha @ 120°C, 20', Dump rinse; SRD;
Note: NO 50:1 HF Dip step in rework.

Date _____ Time _____ Operator _____

STEP 5.00 - PHOTOMASK #5: Gate/ M1 Patterning
All device wafers plus T1,T2. Use T1 and T2 to optimize focus and exposure.

STEP 5.05 – SINGE
Singe wafer in White Oven @200C for 1 hour.
COOL DOWN WAFER.

STEP 5.10 – LOL2000
Headway: 3000 rpm; 60 sec
Bake in white Oven: Load at 125C, close door, set temp to 200C; Bake for 25 min (incl ramp time)

Inspect the back of the wafer after coating and clean any LOL with acetone on the backside of the wafer prior to baking.

Date_____ Time _____ Operator _____

Comments_____

STEP 5.2 -1.0 micron SPIN COAT RESIST
Spin 1um of 3612 positive resist w/o VP with 2mm EBR, using SVG Coat track program 7 (coat and softbake).

System used: : ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date _____ Time _____ Operator _____

Comments _____

STEP 5.25 – Spin Rinse Dry- All device wafers plus T1 and T2
Inspect and clean backside for particles and resist residues
LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

STEP 5.3 - ALIGNED EXPOSE
Expose using asml stepper:
Job name: lrozario/SNF410_2
Layer ID: LAYER 6
Layer Number: 6
Image ID: METAL1
Reticle ID: **SNF410_B001**

Date _____ Time _____ Operator _____

Exposure used:_____**52 mJ**_____

Comments_____

STEP 5.35 – POST EXPOSE BAKE
Bake using SVG Dev track, bake program 1 (bake only)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments_____

STEP 5.4 - RESIST DEVELOP
Bake using SVG Dev track, programs 5 (develop) and 1 (bake)
Change Program 5 Steps **4 & 7** to **21 sec (original = 22sec)**

System used: ❑***svgdev*** ❑***svgdev2***

Date_____ Time _____ Operator _____

Comments_____

2017 SNF410-Depletion Mode NMOS (Option PWell) Flow Run Sheet: Lot ID:_____

STEP 5.45 – VISUAL INSPECTION
Inspect and clean backside for particles and resist residues
Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

Comments _____

STEP 5.5 – Drytek 2 Descum – Device wafers + T1, T2 & T3
Drytek 2, Program 1
Season Drytek 2 for 10 min with conditions described below beore lading wafers. Process wafers for 40 sec
150mT, 100 sccm O2, 250W power

Date _____ Time _____ Operator _____

Comments _____

STEP 5.6 - STANDARD PRE-METAL CLEAN
All device wafers plus T1, T2 and T3
There is queue time between this clean and metal dep. Load wafers into metal dep right after this step without any delay

50:1 DI:HF @ Room Temp, **30 sec**, dump rinse; spin dry

Date_____ Time _____ Operator _____

Remove T3 and measure Tox
T _____ C_____ F _____ L _____ R _____

Comments_____

STEP 5.70 - METAL DEPOSITION
All device wafers and T1 & T2

Innotek Evaporation:
Ti = 5 nm
Pt = 75 nm

Date_____ Time _____ Operator _____

Comments_____

STEP 5.80 – Metal Lift Off

Use T1 & T2 to practice if needed

wbsolvent bench
**** Acetone Soak – Overnight soak + 5 mins in sonication***
**** Megaposit Remover 1165: 3 hours***
**** IPA 5 minutes***
Wafers need to remain "wet" or "soaked" in between chemical changes

Blow dry with N2 gun

Date_____ Time _____ Operator _____

Comments_____

STEP 5.90 - ANNEAL AND ALLOY
8 sccm forming gas (4% H_2 in N_2) @ 350°C; 10 min

RTA-R: progam T350FGLR.RC

Date_____ Time _____ Operator _____

Comments_____

Wafer Resistivity:
All wafers are P t-type; Boron doped
Wafers 1-12 – K-Prime – 5-10ohm-cm
Wafers 13-24 – L-Prime – 11-20ohm-cm

Thermal Oxidation Conditions:
Ramp 30 min N2 800 900c
Dry variable time 900c O2 7slm
Ramp 30 min N2 900 800c

****

Revision Control of this Runsheet:

Rev 0: Runsheet originated from Document "fixed_410_process_W2016_r1" by Max Shulaker for Prof. Roger Howe to define Depletion_NMOS flow (Winter, 2016)

Rev 1: Added Steps for Pwell Implant through 750 Ang Pad Oxide, Pwell Drive in and Oxide strip step before growing 300 Ang Oxide for core flow. These steps are incorporated in **STEP 0.561 TO STEP 0.59**. After these

steps this Optional flow merges to core Depletion_NMOS flow at STEP 0.60. All steps will be identical to Depletion_NMOS_Flow from Step 0.60 to Step 5.90. (Lisa V. Rozario; 1/15/2017).

Rev 1.1: All Pre-Diffusion Clean steps have been changed to take out the last HF clean.

Wbclean-1 or -2,
5:1:1 H2O:H2O2:NH4OH @ 50°C, 10'; dump rinse;
50:1 DI:HF @ Room Temp, 30 sec; dump rinse, spin dry
5:1:1 DI:H2O2:HCl @ 50°C, 10'; dump rinse;
~~50:1 DI:HF @ Room Temp, 30 sec; dump rinse, spin dry~~

Rev 2.2:

1. Exposure energy used for ASML Stepper jobs changed from 50mJ to 70mJ (Usha R. & Ludwig G: 1/18/2017)
2. Remove Descum step prior to All Implants. Keep Descum steps prior to Metal processing. (Usha R.)
3. Alignment Mark Silicon Etch (Step 0.40) in AMTetcher 6:00 minutes gives 1280 Ang in test silicon. Can use P5000 Cham"C" Recipe: Poly Etch for 25 seconds alternatively.
4. Changed 300Ang Oxidation Time to 2 hr 34 minutes (02:34:00) at Thermco1 based on interpolated data.
5. Pwell Anneal time: 2 hour (02:00:00) at Thermco1.
6. Pad Oxide strip time @Step 0.579 is 4 min using 20:1 BOE strip.
7. Fixed ASML job name & Layer numbers for SNF410A001 mask set.
8. Pad Oxide for Pwell Mask: @ Thermco1 "1WETOX" time: 00:25:00 (25 minutes) give 680~740 Ang in 2 runs.

Rev 2.3:

1. Added Pre-diffusion clean prior to regular S/D anneal at 1000C for 20 minutes

Rev 2.4:

Added Step 5.05: Singe @ 200C in White Oven prior to LOL200 coating for driving moisture out and better adhesion of LOL to substrate.

Metal Lift Off conditions also changed for better result and avoid stringers on wafers.