EE410 LAYOUT DESIGN

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2008 Post-Mortem

In general, the P and As profiles are quite close to simulation, but the B profiles are significantly different. In particular, the NMOS Drain is actually p+ doped due to a very high concentration of B (I'm not sure if it remains p+ all the way to the surface since there isn't enough resolution right at the surface).

The dosage on the SIMS data indicates 9.5e15at/cm^2 and 1.1e16at/cm^2 for B at the NMOS and PMOS drains, respectively. However, the highest B doping (the BF2 P-Blanket implant) should have a dosage of 1e15at/ cm^2.

Is it probable that the p-blanket implant was mistakenly done at too high a dose (1e16 instead of 1e15). Otherwise, I am not sure what can cause such a high concentration of B.

Thanks, Jason

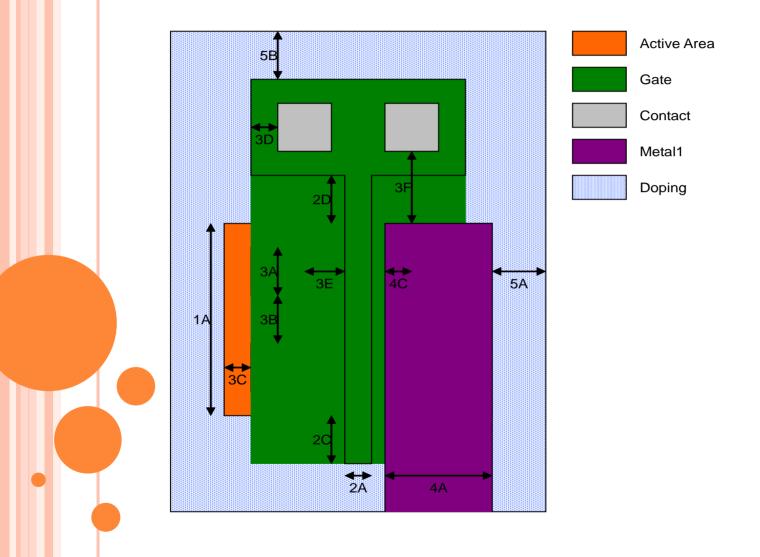
1.E+22 **Boron Profiles** 1.E+21 1.E+20 Concentration (1/cm^3) 1.E+19)P (SIMS -----)As (SIMS)B (SIMS 1.E+18 ------)P (SUPREM ----)As (SUPREM)B (SUPREM 1.E+17 1.E+16 1.E+15 1.E+14 -0.2 0.4 1.2 0 0.6 0.8 1 1.4 Depth (um)

NMOS Drain SIMS vs SUPREM Dopant Profiles

ASML EE410 Design Rules

Rule	Description		Limit (µm)	Standard (µm)		
1. A <mark>c</mark> tiv	ve Ar <mark>e</mark> a			•		
1A	Active Area Width ¹	≥	2.00	4.00		
1B	Active Area Spacing ¹	≥	2.00	4.00		
	¹ LOCOS or STI isolation					
2. Gate						
2A	Gate Length ²	≥	0.10	0.45		
2B	Gate Spacing	2	1.00	1.00		
2C	Gate Extension of Active Area	2	0.50	1.00		
2D	Gate to Active Area Spacing	2	1.00	2.00		
	² Th <mark>e</mark> minimum gate length with trimming process					
3. Con	tact					
3 A	Contact Size	=	1.00	2.00		
3B	Contact Spacing	≥	2.00	2.00		
3C	Active Area Overlap with Contact	≥	0.50	1.00		
3D	Gate Overlap with Contact	≥	0.50	1.00		
3E	Contact to Gate Spacing	≥	0.50	1.00		
3F	Contact to Active Area Spacing	≥	1.50	3.00		
4. Meta	al1					
4A	Metal1 Width	≥	2.00	4.00		
4B	Metal1 Spacing	≥	1.00	2.00		
4C	Metal1 Overlap with Contact	≥	0.50	1.00		
5. Dop	ing (Ion Implantation)					
5A	Doping Overlap with Active Area	≥	1.00	2.00		
5B	Doping Overlap with Gate	2	1.00	2.00		

ASML EE410 Design Rules



What is a Parameterized Cell?

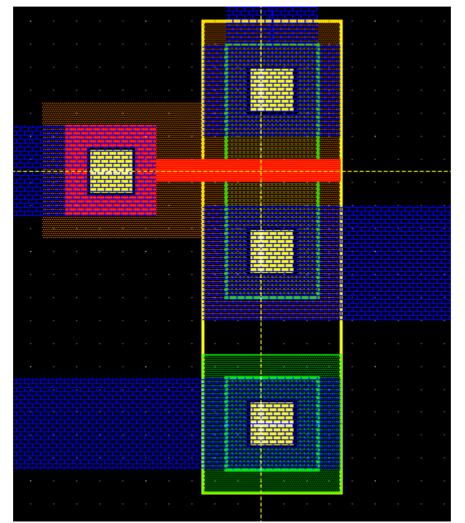
> A parameterized cell, or pcell, is a graphic, programmable cell that lets you create a customized instance each time you place it.

> The pcell you create is called a master. A master is the combination of the graphic layout you draw to make a cell and the parameters you assign to it.

> The edits you make to the master appear in the cell instances when you compile the master. You must make all changes to the master. You cannot edit an instance of a pcell.

P-CELL DESIGN

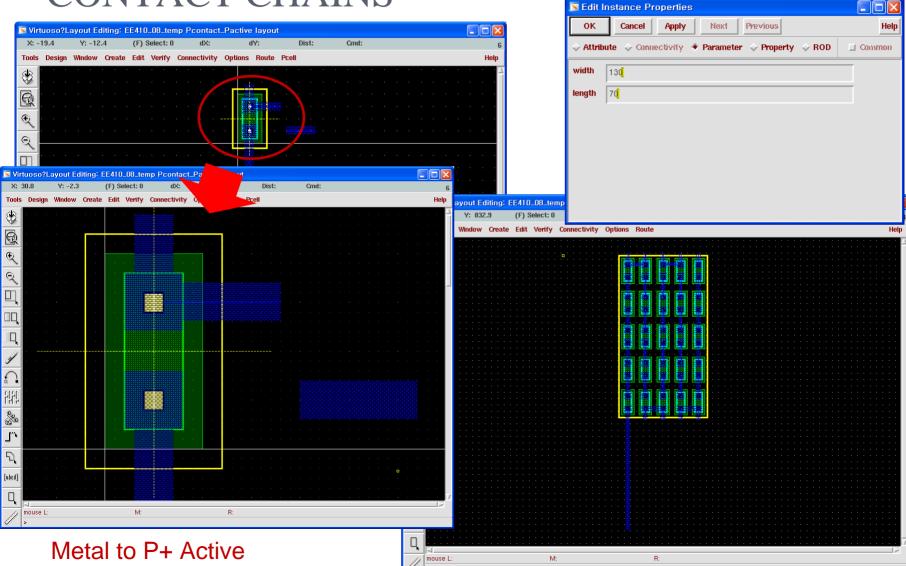
N-CHANNEL MOSFET



P-CHANNEL MOSFET

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CONTACT CHAINS

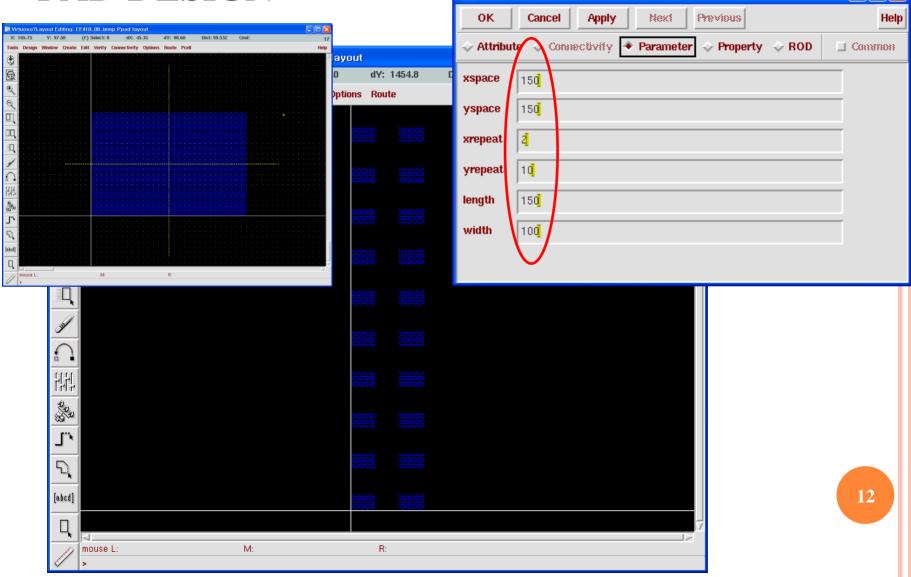


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GROUPING + PAD

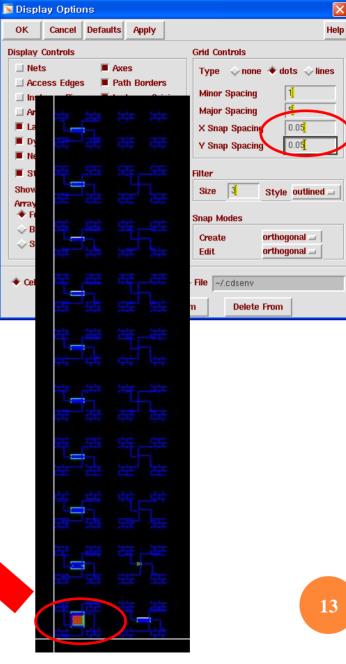
PAD DESIGN



🔀 Edit Instance Properties

P-CHANNEL MOSFET

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CAN THIS FIT IN TO 8.3 MM X 8.3 MM ?

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Top Layout Screen Shot (without circuits and fabrication test structures)