Superconducting Parallel Plate Capacitors with High Kinetic Inductance

E241 Winter-Quarter Report

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Introduction

Project Motivation

Parallel plate capacitors can potentially achieve high capacitance values, while shouldn't introduce unwanted parasitic self-resonances. In addition, introducing kinetic inductance allows nonlinear processes to occur. Combining these three virtues, on-chip parallel plate capacitors open a way to fabricate high-efficiency nonlinear devices for frequency conversion and signal amplification in microwave and millimeter-wave regime. Two applications are especially tempting - microwave to mm-wave transduction for establishing quantum networks and Josephson parametric amplification of microwave signals.

Building of Quantum Networks can be a milestone in the development of quantum computers as it would allow to distribute entanglement between quantum machines and run computing tasks on scattered devices. We proposed[1] a kinetic-inductance-based converter of qubit microwave signals to mm-waves, which could be transmitted between two dilution refrigerators with almost no loss. Moreover, this transducer could facilitate conversion to even higher, optical frequencies when integrated with non-centro symmetric crystal platforms like lithium niobate[2]. We already achieved coupling of mm-waves to a superconducting device[3] and for the next stage of the project, we need to introduce a 5 GHz resonance that requires a large capacitance, that can be achieved with parallel-plate capacitors.

Josephson parametric amplifiers (JPAs) have become a crucial component of superconducting qubit measurement circuitry, enabling recent studies of quantum jumps, generation, and detection of the squeezed microwave field, quantum feedback, real-time tracking of qubit state evolution and quantum error detection[4]. We plan to make an on-chip JPA and for our circuit parameters, it requires non-planar superconducting capacitors to avoid parasitic resonances in the circuit.

Benefits to the SNF Community

We propose the fabrication of a parallel-plate capacitor analogous to the process in the study of K. Cicak et al.[4] for aluminum structures. In our case we want to fabricate devices of niobium on Sapphire, Nb has a higher transition temperature and kinetic inductance than Al. Sapphire substrate potentially allows to integrate superconducting circuits with optical platforms, like lithium niobate and work in the infrared regime with low loss. First, we plan to develop a process to fabricate a capacitor with a dielectric layer (SiO2), then we would like to work out a way to remove the dielectric (or another sacrificial layer) and fabricate vacuum-gap capacitors to achieve lower loss resonators.

Deliverables:

Done in the Fall Quarter:

- ✓ Characterization of selective Nb etching in CF_4 plasma – 3 parameters DOE
- ✓ Characterization of selective SiO_2 etching in CF_4:CHF_3 plasma – 3 parameters DOE

- ✓ Characterization of lesker-sputterer in the context of Nb Deposition
- ✓ Evaporation of good-quality Niobium films

Done in the Winter Quarter:

- Process flow for wet HF etching of SiO_2 and releasing Nb structures:
  - Air Bridges for Spiral Inductors
  - Parallel Plate Capacitors
- Process for creating vias to galvanically connect two planes

All of the process components that we develop during the class will allow other SNF users to fabricate complex niobium/oxide structures like, for instance, non-planar resonators[4], electro-optic modulators[2], microwave to millimeter-wave frequency transducers[1] or MEMS devices.

Superconductivity

Superconductivity is an attribute of materials where the resistance vanishes and magnetic fields are repelled. Any material that shows these electrical properties is called a superconductor. Conventional superconductivity can be understood by Bardeen-Cooper-Schrieffer theory or BCS theory[6]. The theory describes superconductivity as a microscopic phenomenon caused by the formation of an electron-electron bound state called a Cooper-pair.

To see how the formation of Cooper-pairs is related to superconductivity, we will follow a classically-motivated approach[7,8]. For normal conductors, the resistance to electrical currents can be seen microscopically as the scattering of the electrons off of the conductor's crystal-lattice. In other words, the lattice-vibrations have a direct influence on the resistance. As we cool down the conductor, we find that the low-thermal-energy-environment causes the lattice vibrations become dampened and decreases the probability of electrons to scatter off of the lattice. Hence, the resistance decreases.

For superconducting materials when the temperatures are low enough, the electrons that are moving will attract positive charges within the lattice. This deformation of the lattice causes another electron, with opposite spin, to move into the region of higher positive charge density. The two electrons now become correlated i.e. form a Cooper-pair with total spin either 0 or 1. Since there are many such pairs in superconductors and have bosonic spin properties, they can collect and form a condensate. In this condensed state, the energy required to break a single Cooper-pair bond is related to the energy to break the bonds of all the Cooper-pairs. Thus, when the condensate is travelling through the superconductor it remains undisturbed by the lattice because the vibrations do not have enough energy to impact the state of a single Cooper-pair and so all of the electrons flow without any resistance.

Superconducting Parallel Plate Capacitors

Superconducting devices are electronic devices that utilize the zero-resistance properties of superconductors. In general, these devices are used for highly sensitive, low-loss electrical systems. We are interested in on-chip low-loss microwave electronics wherein quantum

systems are developed. In addition to low-loss components, we also care about microwave components that can be treated as lumped-elements.

Often, coplanar waveguides (CPWs) are used as transmission lines or resonators when paired with interdigitated capacitors (IDCs)[9]. However, for our purposes fabricating resonators with CPWs and IDCs require footprints spanning millimeters. With large footprints these components suffer from non ideal, distributed characteristics such as parasitic inductances and capacitances resulting in unwanted resonant modes[10]. With parallel-plate capacitors, we are provided access to large capacitances while suppressing the nonidealities we observe with IDCs.

In addition to fabricating lumped-element resonators, we are concerned with intrinsic loss-mechanisms within the materials. The main loss mechanisms for quantum systems that we are interested in are due to unsaturated two-level system (TLS) defects found in amorphous dielectric materials[10,11]. For LC resonators with dielectric-filled parallel-plate capacitors, it has been shown that energy is lost to a TLS-bath[10]. Therefore, we would like to develop vacuum-gap capacitors (see Figure 1 below), releasing the dielectric from between the capacitors on a Niobium-Sapphire platform, instead of a Aluminum-Sapphire platform shown in previous work[5].

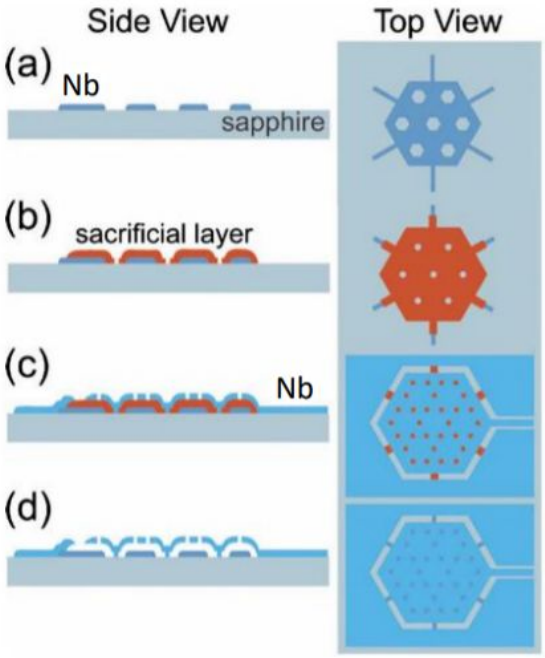

Figure 1. Proposed parallel plate capacitor processing flow. Modified from Cicak et al.[5]

Kinetic Inductance

Our decision to use Niobium as our metal-film for this project comes from the fact that it has a high kinetic inductance. Kinetic inductance is naturally described by the Drude model of electrical conduction[13]. The Drude model is an application of kinetic theory and assumes that the microscopic behaviour of electrons in a solid may be treated classically (as we did when

discussing superconductivity). The model considers DC conductivity and the time-to-collision, τ, of mobile charge carriers:

$$\sigma(\omega) = \frac{ne^2\tau}{m^*(1+\omega^2\tau^2)} - i\,\frac{ne^2\omega\tau^2}{m^*(1+\omega^2\tau^2)} = \sigma_1 - i\,\sigma_2$$

Here m^* is the effective mass of the charge carrier. In our case, the charge carriers are electrons. The imaginary component of the complex conductance, $-\sigma_2$ represents the kinetic inductance. For superconductors, the time-to-collision $\tau \to \infty$ and we find that in the limit the term that represents kinetic inductance remains. This model also shows that even though dc resistance vanishes for superconductors, there is still a non-zero ac-impedance observed[14].

Intuitively, kinetic inductance comes from the inertial mass of the electrons in alternating electric fields. Since electrons (or other charge carriers) have finite mass, they tend to travel at a constant velocity, once accelerated. Therefore, it takes a finite amount of time for the electrons to gain speed, when acted upon by the changing electric field. Thus, resulting in a phase lag with respect to the varying electric fields (voltage). This is identical to the phase lag experienced by geometrical inductors when they are exposed to a change in voltage which is opposed by a change in magnetic flux. In one case the energy is stored in the kinetic energy of the electrons (where the name comes from) and in the other case the energy is stored in the magnetic field. Since they have the same phase lag characteristics, both of these energy storage mechanisms are seen as inductances $L = L_0 + L_K$.

Fabrication Process Development

Last quarter we answered three main questions that were critical for this fabrication process:

1. How to deposit acceptable niobium films? (Bottom electrode)
2. Can we selectively etch oxide against niobium? (Niobium posts/vias)
3. Can we selectively etch niobium against oxide? (Top electrode)

Detailed answers to the above questions can be found in our Fall Quarter Report. We determined that sputtering good quality Niobium films in Kurt J. Lesker 1 tool in the ExFab at SNF is not a viable option. Daily chamber venting and allowing many different materials in the chamber makes it difficult to meet the specification of the tool. Contamination and high chamber pressure reduce the quality of the sputtered films. In the end, we used our lab's e-beam evaporation tool (Plassys) and found that it gave acceptable films with T_c ~ 7 K (see Planar Resonators section for details).

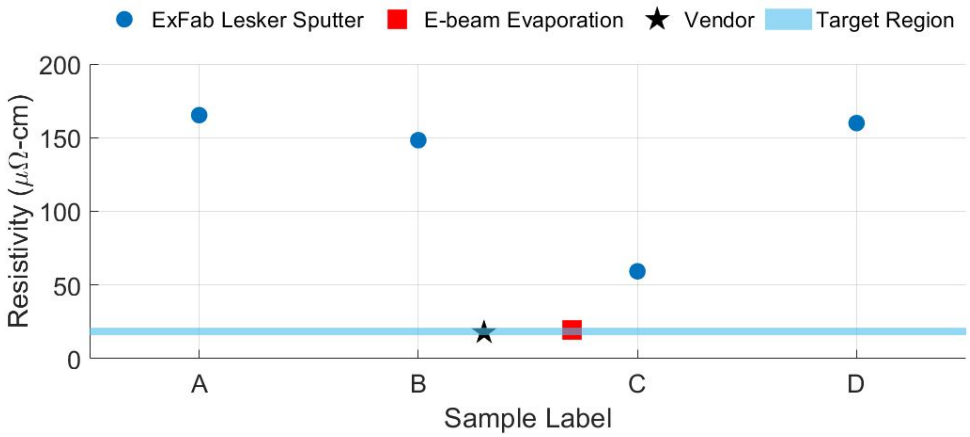

Figure 2. Resistivity results from last quarter. Resistivity is correlated with the superconducting temperature. We see that the best ExFab deposition is ~ 4x the value of the resistivity required in the target region. Samples A, B, C, D were processed with different fabrication conditions.

After we deposited Niobium with resistivity that is in the target region (see Figure 2), we patterned some superconducting quarter-wave resonators and conducted measurements. In Figure 3 (A), we see through the microscope of the Westbond Wirebonder tool which is part of SNSF. We need to wirebond our resonator device to have a connection from the PCB ground plane to our device's ground plane (this is a coplanar waveguide geometry).

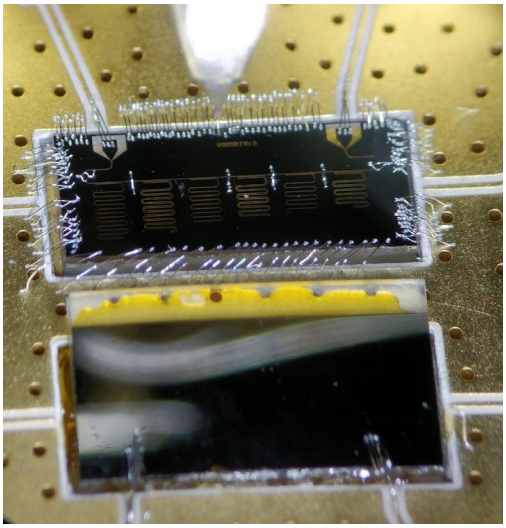

Figure 3. (Top) Niobium coplanar waveguide resonators coupled to a feedline on Sapphire substrate. The device is wire-bonded to a custom PCB to make good contact to the ground planes. The holes in the PCB are vias that connect the top PCB ground plane to the bottom PCB ground plane. The chip is 4 mm x 9 mm. (Bottom) Unpatterned Niobium on Sapphire chip and serves as a control.

We also developed selective etch processes using PT-Met and PT-Ox, in addition to Silicon Dioxide deposition using ccp-dep in SNF. The Niobium etch has a selectivity of 9:1 against oxide, with an etch rate of 283 nm/min using PT-Met: 70 sccm CF_4, 2 sccm O_2, 50 mT pressure, and 50 W RF Bias power. Figure 4 shows the bottom plate of the capacitor, post-etch. PT-Met leaves some organo-metallic post-etch residue on the substrate, for which the cleaning procedure was developed this quarter (see Post Metal Etch Cleaning Procedure).

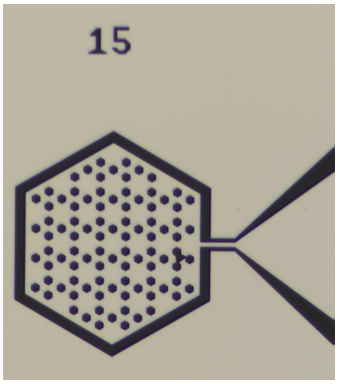

Figure 4. Bottom electrode of the capacitor, post etch. We can see a defect which comes from Heidelberg2 or chip contamination.

The Oxide etch has a selectivity ~ 10:1 against Niobium, with an etch rate of 171 nm/min using PT-Ox: 10 sccm CF_4, 40 sccm CHF_4, 20 mT pressure, and 150 W RF Bias power. Figure 5 shows the pattern post oxide etch. At this stage, our main fabrication questions have been answered.

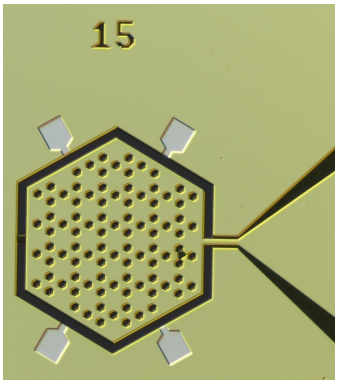

Figure 5. Mask two of the fabrication process, post oxide etch. Heidelberg2 aligns to within 0.5 microns.

For this quarter, our main fabrication questions were:

1) How do we deposit Niobium so that it fills the vias for the top electrode?
2) How can we clean the post-etch residue that is left by PT-Met?
3) How can we release the capacitors *i.e.* selectively etch oxide?

The answers to these questions are provided in the following sections of this report. We will also discuss some design procedures we used for the superconducting devices.

Niobium Evaporation

We use a Plassys Electron Beam Evaporator MEB550S, courtesy of the Safavi-Naeini lab. This is a state of the art physical vapor deposition tool that uses an intense electron beam source material under high vacuum (~2e-8 Torr), offering a wide range of well-controlled deposition rates via crystal monitor. This system is also equipped with an Ion gun for sample cleaning and milling. Figure 6 shows an example of how we mount our sample onto the platten of the Plassys. We have two different evaporation procedures, one for the bottom electrode (Mask 1) and one for the top electrode (Mask 3).

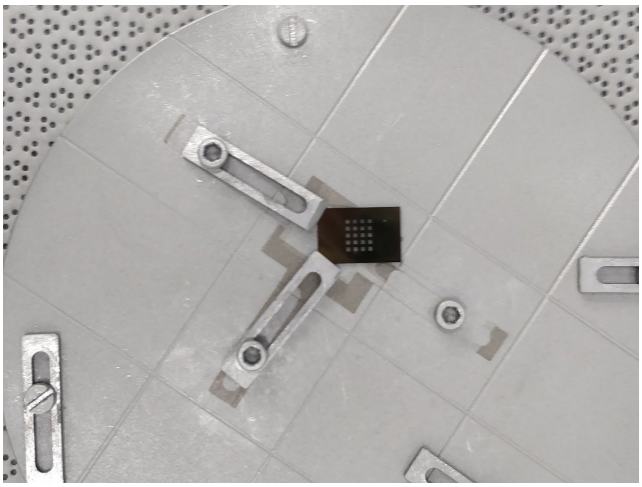

Figure 6. A 10 mm x 15 mm piece mounted onto the Plassys platten. We leave several millimeters of space between the clamps and the patterns to avoid shadowing effects from the clamp faces.

Normally Incident Evaporation

For the bottom layer of Niobium we have a simpler evaporation procedure compared to the top layer of Niobium. We begin with a fresh substrate sample:

1. Rinse sample with Acetone for 30 seconds
2. Wet transfer into Acetone dish > ultrasonic bath for 5 minutes
3. Rinse the sample with 2-Propanol (IPA) for 30 seconds
4. Wet transfer into IPA dish > ultrasonic bath for 5 minutes
5. Final rinse with IPA for 30 seconds, blow dry with N_2
6. Bake sample for 20 minutes at 180 C
7. Mount sample on the platten (Figure 6) and load into Plassys
8. With the shutter closed, evaporate Titanium for 2 minutes at 2 nm/s for gettering
9. With the shutter open, evaporate Niobium at 0.7 nm/s until thickness of 200 nm is reached (crystal monitor), with planetary rotation of 5 rpm
10. Close the chamber gate valve and expose sample to O_2 for 10 minutes at 10 millitorr (for repeatability of native oxide).

With the above evaporation procedure, we characterized the Niobium via resistivity measurements (previous quarter results) and then by patterning coplanar waveguide (CPW) resonators. The performance of the CPW resonators are described in the planar resonator section.

Angled Evaporation

For the top electrode (Mask 3), we have to consider the directionality of e-beam evaporation. Since we would like to have Niobium "posts" (see Figure 1 (D)) to make contact with the sapphire substrate, we need to change the evaporation process. These posts act as support for the top plate of the capacitor after the oxide has been released. Figure 7 shows a diagram of how the evaporation is conducted. The question mark indicates that the Niobium flux is incoming at an angle. We evaporated at a 30 degree angle, which can be further optimized by resonator measurements and by release yield. The evaporation angle is an important parameter because it has an impact on the corner stresses that the posts observe. If these stresses are too high, then the chance of fracture increases, reducing yield. Additionally, there are some potential shadow effects which are mitigated by the substrate rotation - we rotate at 5 rpm.

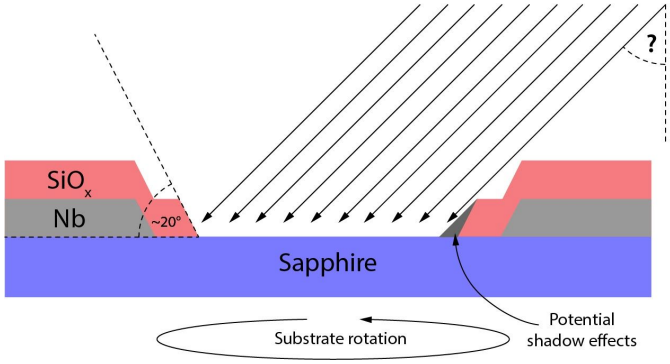

Figure 7. Diagram showing how the top electrode evaporation occurs. We evaporate at an angle of 30 degrees. The Oxide sidewall angle is ~ 20 degrees.

The aspect ratios we have fabricated successfully range from 10-30. We define aspect ratio as the width of the largest hole (diameter) on the capacitor divided by the thickness of the Silicon Dioxide layer. So the lower the aspect ratio, the skinnier the post because we keep the thickness constant throughout our fabrication.This is of particular interest for SNF because this process can also be used to galvanically connect two metal planes, rather than depositing the top Niobium layer to the substrate. Figure 8 shows an SEM image of the posts. We see that the planetary rotation and angled evaporation gave us the sidewall coverage we wanted and minimized the shadowing effects due to misalignment of the sidewall angle of the Oxide and the evaporation angle.

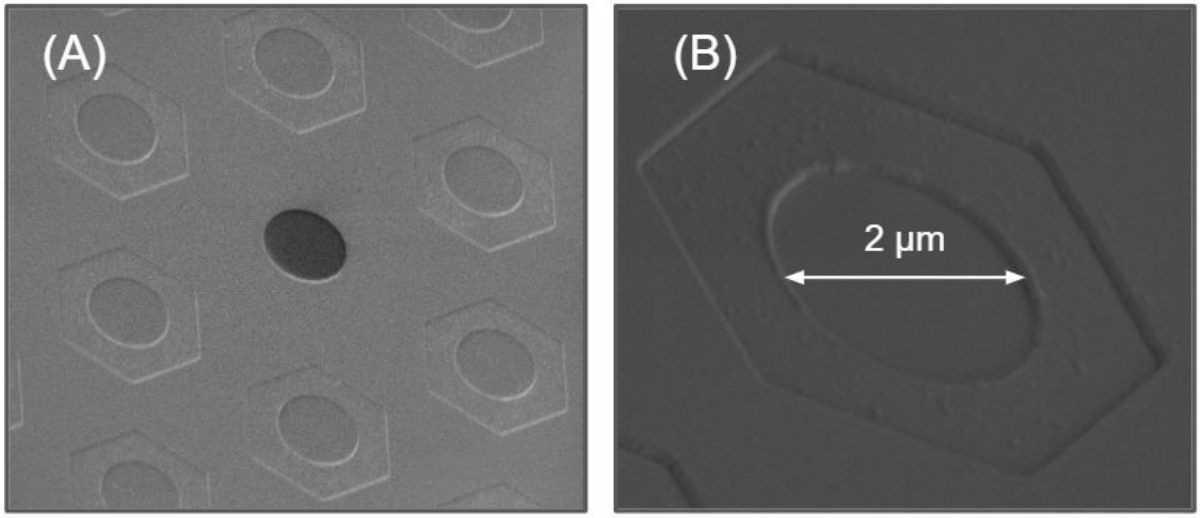

Figure 8. (A) Shows the posts which are circles within hexagons and a releasing valve, which is a circle. (B) Shows a close up of one of the posts, and we see acceptable sidewall coverage and Niobium where we expect. In these SEMs the diameter of the circles are 2 microns.

In addition to the angled evaporation, we conducted an ion milling step to clean the sample and mill the substrate so that we have ohmic contact for the posts. In Figure 9 we show the effect of the ion-milling. Figure 9 (A) shows a strain test-structure that was processed without ion-milling. We see in the corners of the structure that they are sharp and not rounded. In Figure 9 (B) we see a similar structure, which was ion-milled. We see rounded corners indicating that the top layer of the substrate was etched away due to the milling.

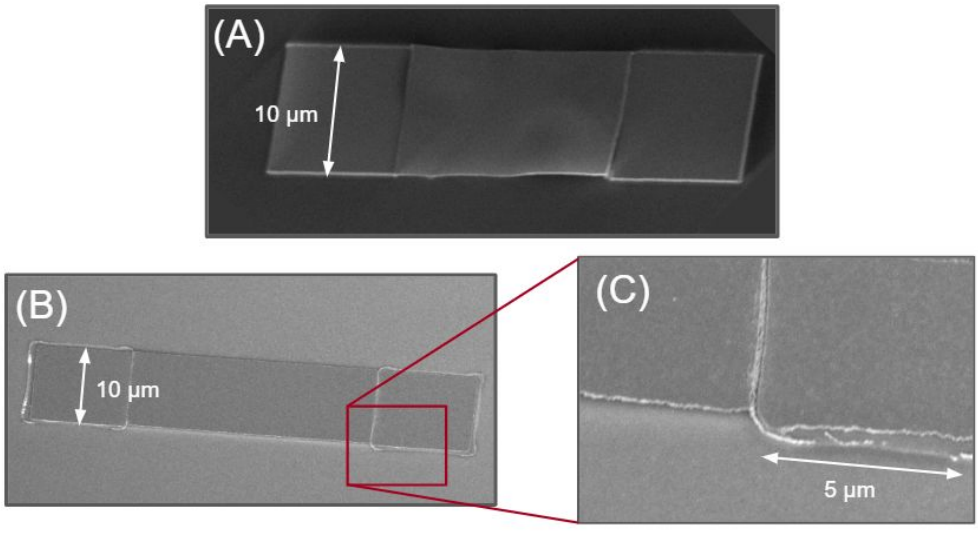

Figure 9. (A) SEM image of test strain structure without ion-milling before top layer evaporation. (B) SEM image of test strain structure with ion-milling before evaporation. (C) Zoomed in of image (B).

The evaporation procedure is similar to the previous section except now our sample is assumed to be at the post-oxide etch (mask 2) stage. An important note is that since we are evaporating at an angle, we have to consider the *sticking factor* of this Niobium. In other words, the way we deposit 200 nm thick Niobium, the setpoint we use is 255 nm = 200 nm/cos(30 degrees) * 1.1. We found that leaving a margin of 10% gets us to our target thickness relatively well. We confirm this with profilometry and confocal microscopy (see sections below). The procedure is:

1. Rinse sample with Acetone for 30 seconds
2. Wet transfer into Acetone dish > ultrasonic bath for 5 minutes
3. Rinse the sample with 2-Propanol (IPA) for 30 seconds
4. Wet transfer into IPA dish > ultrasonic bath for 5 minutes
5. Final rinse with IPA for 30 seconds, blow dry with N_2
6. Bake sample for 20 minutes at 180 C
7. Mount sample on the platten (Figure 6) and load into Plassys
8. 400 V, 20 mA Argon Ion Milling for 3 x 70 s @ 0 degrees, 20 degrees, -20 degrees
9. With the shutter closed, evaporate Titanium for 2 minutes at 2 nm/s for gettering
10. With the shutter open, evaporate Niobium at 0.7 nm/s @ 30 degrees until thickness of 255 nm is reached (crystal monitor), with planetary rotation of 5 rpm
11. Close the chamber gate valve and expose sample to O_2 for 10 minutes at 10 millitorr (for repeatability of native oxide).

3 Mask Process for Parallel Plate Capacitors

This section encapsulates a detailed process description for the development of a non-planar capacitor structure. For a concise overview, refer to the Runsheet.

Mask 1 Process

1. Evaporate a thin niobium film incident normally (roughly in the order of 200nm - refer to Normally Incident Evaporation for more details).
2. Sample preparation
    a. Fire up two hotplates and set temperatures to 180C and 90C respectively.
    b. Perform a solvent clean in the solvent bench (acetone+2-propanol for 30s each) and then use the N_2 gun to blow dry the sample followed by a dehydration bake for at least 5mins on the 180C hotplate.
    c. Blow dry and clean the interior and the tip of a glass pipette to remove any residual particles before transferring any photoresist (PR).
    d. Use sufficient SPR3612 photoresist to spin-coat the film with a ~1um thick film in any of the headway spinners (speed of 5500rpm and a ramp of 1500rpm/s suffice). **Try to avoid any bubbles while transferring the PR from the pipette to the sample, minimizing streaking effects from the spin-coating procedure.** This could easily be achieved by creating a streamlined flow of the PR over the Aluminium foil surrounding the spinner before transferring it to the sample.
    e. Perform a post-resist bake for 1min at 90C.
    f. Make sure that the backside of the sample is devoid of any photoresist. **This step is crucial since photoresist is notorious for reducing the performance of the vacuum system in heidelberg.** If there is any PR on the backside, put some acetone on a wipe, let the extra acetone evaporate away and gently rub the backside on the wipe until the stain is gone. Then repeat this process with 2-propanol to remove any excess acetone.
3. Photolithography
    a. In Heidelberg2, load the CAD file in the Designs folder.
    b. Choose appropriate sample size and convert the design using appropriate booleans and inversion (one can use the Viewer tab in the Convert Design window to see the regions of exposure).
    c. Follow the steps as prompted by the tool and load the substrate. The vacuum panel showing a suction in the “green” region (~-0.67) is considered good. Anything in “red” (~-0.5) needs to be reported (caused by backside photoresist which can play a role if 2.f is skipped).
    d. Expose the sample in Heidelberg2 with a dose of 100mJ/cm^2 and a defocus of 0. Using the exposure angle doesn’t make a huge difference but this needs to be consistent across all the three masks.
    e. Prepare glassware for developer MF26A and DI water in a development bench.

f. Develop the sample in MF26A for 50s and DI water for 40s (20s spray + 20s rinse)
g. Quickly inspect the developed sample under an optical microscope to confirm the pattern. Note the contrast between the developed and undeveloped regions to figure out.
h. If 1.g goes well, hard-bake the developed sample in an hotplate at 115C for 3mins

4. Plasma Etching
    a. In the **PlasmaTherm Metal** tool, run the **Cham_Clean_Def_Cl2_SF6_O2** sequence loading a dummy Silicon wafer for chamber cleaning.
    b. Next we need to condition the chamber before running the actual etching process on the sample. The same dummy wafer used for chamber clean can be used for this step without venting the load-lock. Typical chamber conditioning time is between 200-300s. The highlights of the sequence are:
        i. CF_4+O_2 : 70+2 sccm
        ii. Chamber pressure: 50 mT
        iii. RF Bias Power: 50 W
        iv. ICP Power: 1000 W
        v. Substrate Temperature: 20C
    c. Mount the sample on the conditioned wafer using the pump-diffusion oil. This viscous fluid has excellent heat conducting properties, hence providing a good thermal contact between sample and the carrier substrate. A good rule of thumb in determining the quantity of oil to apply for mounting is to use ½ a drop for a 5x10mm sample. A safe method to mount a sample can be outlined as follows:
        i. Apply an appropriate amount of oil on the carrier.
        ii. Carefully place the chip ballparking the center.
        iii. Use tweezers to move the sample vertically and horizontally by small amounts, in order to spread the oil uniformly under the working area of the sample. Additionally, prevent any exposure of the oil from the edges, which can cause chamber poisoning and might redeposit on the sample while being exposed to the hot plasma.
        iv. Slightly tilt the carrier wafer to confirm adhesion.
    d. Load the mounted sample into the load-lock and use the same sequence for etching with time decided according to the film thickness. This recipe has an etch rate of ~3.497nm/s. Although, this rate is well-calibrated but it comes with a tiny caveat. The pump-diffusion oil plays a significant role in determining this etch rate and can be pretty non-uniform (upto ~40%) in case of larger samples (for example, a 2” substrate). Extra attention needs to be given to sample mounting (4.c.iii) in such situations, so as to achieve the promised etch rate uniformly across the sample. Another method to tackle this non-uniformity is to estimate time using an over-etch buffer of ~20-30%. The best method is usually an informed combination of the two mentioned above.

e. Usually seeing an etch through the niobium film in the sample is a good metric to decide the success of the process. In case of any discrepancy, transferring the sample back to chamber and repeating 4.d with a new estimated etch time is advisable.
f. Once convinced, vent the load-lock, unmount the sample carefully from the carrier substrate (warning: sample could be sufficiently sticky: nudging from the different edges and then gently lifting it out can be a good idea) and perform a solvent clean of the carrier wafer (acetone+2-propanol for 30s each) and then use the N_2 gun to blow dry it. The pump-diffusion oil doesn't stick to the carrier and hence, suitable for reuse (although not advised to reuse over 3 times).

5. Sample Clean
    a. Post-etching procedure for mask 1 includes a five stage sample clean, in order to get ready for processing mask 2. First, is an **O_2 Plasma Clean** stage. The steps involved in this stage includes:
        i. Performing a regular chamber descum of the **Asher tool** in the flexible cleanroom with the following parameters:
            1. Power: 300
            2. Time: 60s
            3. O_2: 3sccm (less O_2 signify a directional gas flow in the chamber)
        ii. Place the sample on the sample holder associated with the tool and load the holder in the floating plate (bottommost) with respect to the plasma. This is commonly known as the indirect mode.
        iii. Now perform the sequence with the following parameters:
            1. Power: 100
            2. Time: 120s
            3. O_2: 10sccm (more O_2 signify an isotropic gas flow in the chamber)
        iv. Unload the holder and secure the sample when the system starts to "Bleed" (upon hearing a high-pitched noise from the system).
    b. Next stage is **Solvent Clean**. Perform a solvent clean in the solvent bench (acetone+2-propanol for 30s each) and then place the sample in a glassware containing acetone.
    c. The next stage is **Ultrasonic Acetone Bath.** Put the glassware with the sample in an Ultrasonic bath for 2 mins at lower power (~2). This is preferably done at SNC because it has a support for the holding the glassware, as opposed to the baths in SNF, which can cause the glassware to tumble easily. After the process, clean the residual acetone from the sample using 2-propanol for ~30s and then use the N_2 gun to blow dry the sample.
    d. The fourth stage is **10:1 HF Clean** in the acid bench, which is motivated from the attempt to remove the contamination from the PlasmaTherm Metal tool. Please refer to Hydrofluoric Acid clean for more details.
    e. The last stage is **Ultraviolet-Ozone Clean.** Load the sample in the **Samco Ozone Cleaner** at SNC with the following parameters:
        i. Time: 20mins

ii. Temperature: 60C (setpoint drifts to ~74C after 20mins, not a problem)
iii. O_2 flow rate: 0.75L/min.

After the system purges (takes ~3mins after setpoint), unload the sample.

Mask 2 Process

1. SiO_x deposition using ccp-dep tool in SNF (roughly ~200nm thickness)
    a. Run the chamber clean process **(CLN350)** for ~10mins, then end step
    b. Load exactly 4 dummy silicon wafers (dedicated for ccp-dep)
    c. Run the chamber conditioning process **(SIO350)** for 10 mins
    d. Vent and load the sample with its calibration Silicon counterpart (since the Si sample will help us inspect the thickness as Sapphire is a clear substrate)
    e. Pump the chamber and run SIO350 process for a dedicated time (advisable to use the rate used for the last fabrication run concerning ccp-dep for consistency, since the deposition rate walks around a little bit)
    f. Vent and unload the wafers and samples onto Al foil (Do not place wafers/samples in boxes or wipes since they are at ~350C just after the completion of the process).
    g. Pump and transfer the platen into the deposition chamber and run the **CLN350** process for ~3mins before disabling the tool while it gets ready for the next user.
    h. Measure thickness in nanospec (use model: **oxide on Si**). Focus to get a sharp image for calibration wafer with the nanospec tool and refocus on the calibration sample from ccp-dep before getting measurements at different points.
    i. Find the thickness, hence the rate which shall be used for calculating process time for the next deposition in ccp-dep.

2. Sample preparation
    a. Load the sample in one of the **Yes Ovens** at SNF for priming (~2nm of HMDS is applied on top of the sample to improve adhesion of photoresist to substate). This is an automated process taking ~35mins.
    b. Fire up a hotplate and set the temperature to 90C.
    c. Follow steps 2.c through 2.f similar to the mask 1 process for rest of the sample preparation.

3. Photolithography
    a. The converted design file will already be saved In Heidelberg2. Find and restart the job file used for mask 1 exposure. In case the job file is missing/cannot be found, create a job with the settings similar to mask 1.
    b. Add a new layer to the existing settings and create an alignment cross file by clicking the **Align Cross** tab.
    c. Enter the coordinates of the crosses from the CAD file. Two crosses suffice but four can be used to verify the alignment, enhancing the confidening in the exposure. At this point, it can be pretty arduous to find cross coordinates from the

CAD file. A trick which can come in handy is to store the cross centers well in advance in a file and enter the coordinates directly when prompted by the tool.

d. Further use the Low Res/High Res/Bull's eye mode to get better adjustments in the crosses, before accepting the measurements from the tool.
e. Follow steps 3.c through 3.f similar to the mask 1 process for the rest of photolithography.

4. Plasma Etching
    a. In the **PlasmaTherm Oxide** tool, run the **O2 Clean1** sequence loading a dummy Silicon wafer for chamber cleaning.
    b. Next we need to condition the chamber before running the actual etching process on the sample. The same dummy wafer used for chamber clean can be used for this step without venting the load-lock. Typical chamber conditioning time is between 200-300s. The highlights of the sequence are:
        i. CF_4+CHF_3 : 10+40 sccm
        ii. Chamber pressure: 20 mT
        iii. RF Bias Power: 150 W
        iv. ICP Power: 600 W
        v. Substrate Temperature: 20C
    c. Follow steps 4.c through 4.f similar to the mask 1 process for plasma etching repeating the same sequence for appropriate time (etch rate: 2.86nm/s).
5. Sample Clean
    a. Post-etching procedure for mask 2 includes a three stage sample clean. Follow steps 5.a through 5.c in the Mask 1 Process for rest of the sample clean procedure.

Mask 3 Process

1. Evaporate a thin niobium film incident at an angle, for more sidewall coverage (roughly in the order of 200nm - refer to Angled Evaporation for more details).
2. Follow steps 2 through 5.c in the Mask 1 Process for rest of the processing.

Post-metal etch cleaning procedure

After etching patterns in niobium film on sapphire substrate we noticed that the areas where we expected the entire niobium to be etched away are covered with unknown residue. It was not obvious right after the etching but was clear after covering the chip with PECVD silicon dioxide. Figure 10 shows an example of the residue, on (A) the dark area is sapphire, where the entire 200 nm niobium should have been etched away, but we still see uniform residue. Picture (B) shows a profilometer square etched in niobium, here we can see the same residue with clear lines that have been made by a profilometer probe. As we plan to fabricate sensitive superconducting devices we had to address the issue of chip cleanliness.

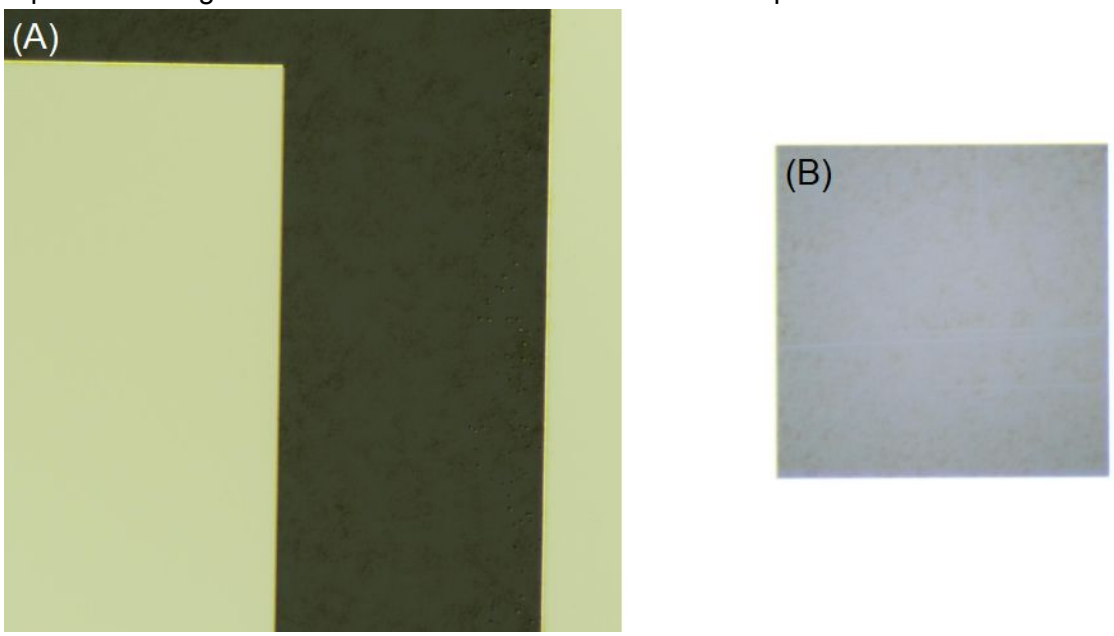

Figure 10. (A) Microscope picture of post-metal etch residue on sapphire between two Nb areas; (B) Profilometer box with visible residue, lines from profilometer measurements are visible

To learn more about the structure of the residue and ways to remove it we studied three methods of sample clean:

1. Solvent Clean with Acetone and 2-propanol
2. SRS-100 and PRS-1000
3. Hydrofluoric Acid

All of the methods included short oxygen plasma cleans as part of the processing, results are presented in the following sections.

Solvents and Ashing

Initially, we tried to clean samples with only acetone and 2-propanol rinses followed by an ultrasonic bath in acetone and another rinse. In this approach we started with a short oxygen plasma clean using March Instruments device in the flexible cleanroom, indirect ashing has been done with 100W of RF power and 10 sccm oxygen flow for 2 minutes, this step effectively

etches the top layer of baked resist and makes it easier to remove it with solvents. Next, we timed our rinses to be 30 seconds each, the ultrasonic bath took 5 minutes. This procedure was optimized for complete resist stripping, but it turned out that it is not effective for cleaning of the post-metal etch residue. Examples of SEM micrographs after this procedure are presented in Figure 11, picture (A) show the pattern of the bottom capacitor plates with holes, meant to form posts for the top plate support. Picture (B) shows one of the mentioned holes with visible residue in the center, according to the mask we would expect this area to be cleaned of niobium, etched down to a smooth surface of sapphire substrate. Picture (C) shows that the residue in the hole forms a thin film of unknown origin, there is very little contrast difference between it and Niobium, which suggests that it may be conductive. Picture (D) shows the etch edge covered with another type of residue, which might mainly come from a sidewall-polymer formed out of etching byproducts and baked resist.

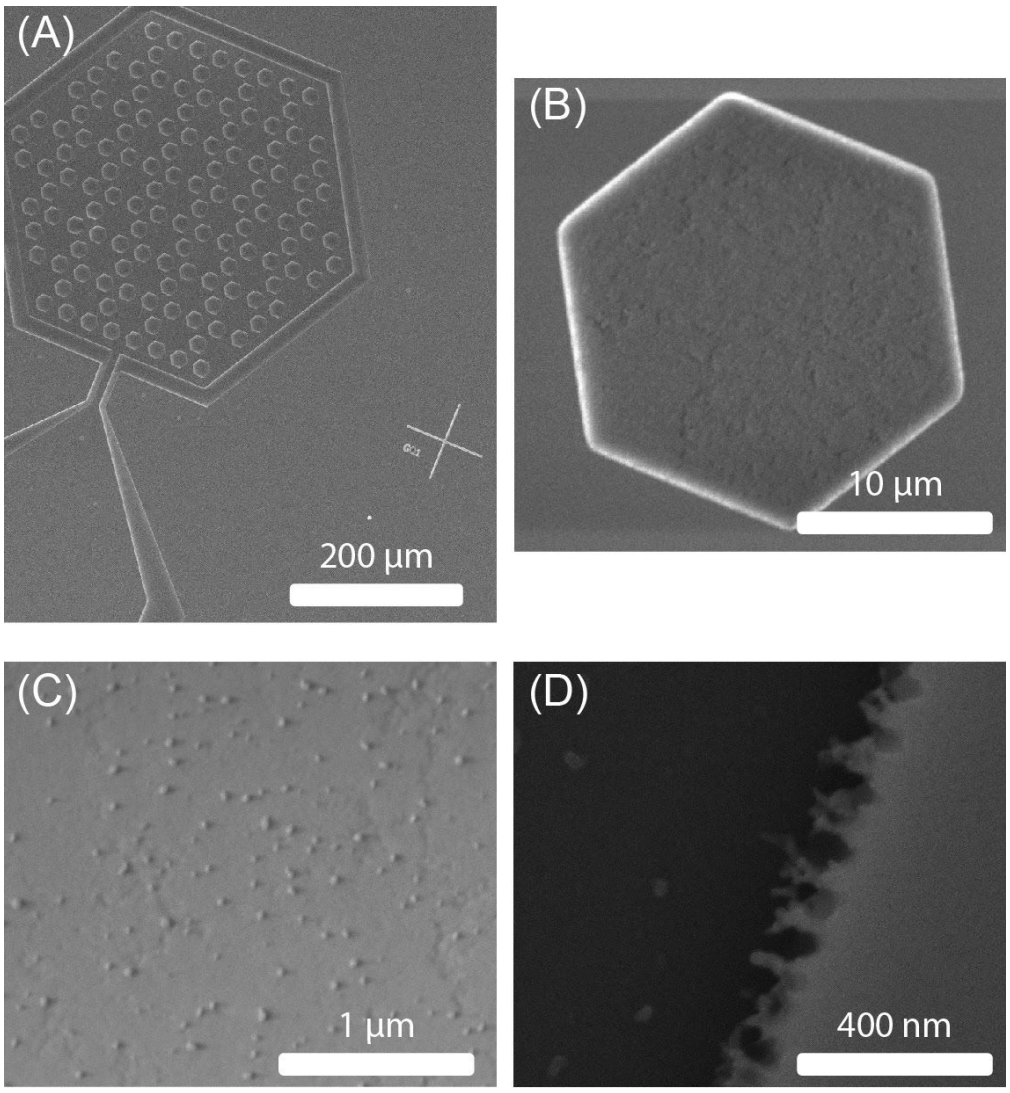

Figure 11. (A) Pattern of the bottom capacitor plate; (B) Zoom into one of the hexagonal holes meant for support posts of the top plate; (C) Zoom into the film formed in the hexagonal holde; (D) Etch edge contaminated by the resist-related residue.

SRS-100 and PRS-1000

In order to clean samples after the metal etch we tried to employ a standard cleaning procedure used in the Stanford Nanofabrication Facility - two step clean with SRS-100 and PRS-1000:

- SRS-100 contains:
  1-Methyl-2 pyrrolidinone, 40-60%
  Thiophene, Tetrahydro-, 1,1-dioxide, 30-50%
  2-Propanol, 1-amino-, 5-15%
- PRS-1000 contains:
  2-(2-Ethoxy-ethoxy)ethanol (10-30%),
  sulfolone (25-45%), 1-Methyl-2-Pyrrolidinone (35-55%),
  Tetraethylene Glycol (1-10%), monomethanolamine (<0.1%)

Before the clean we stripped resist as described in section Solvents and Ashing. The recipe that we used was SRS-100 at 60°C for 20 min followed by PRS-1000 at 80°C for 10 min. After this procedure, we dried our sample and analyzed the surface with SEM, results are presented in Figure 12, picture (A) shows the entire bottom capacitor plate pattern, on picture (B) we see hexagonal holes with edges contaminated with previously unseen residue. Zooming on the edge on picture (C) shows that the black residue is peeling off the edge, it is probably the same structure as we observed in Figure 11 (D), peeling off the edge. This suggests that it is indeed resist-related and can be influenced by the standard cleaners but it still sticks to the edge of the chip, this is likely a result of the conductive film that is resistant to solvents and covers the entire hole.

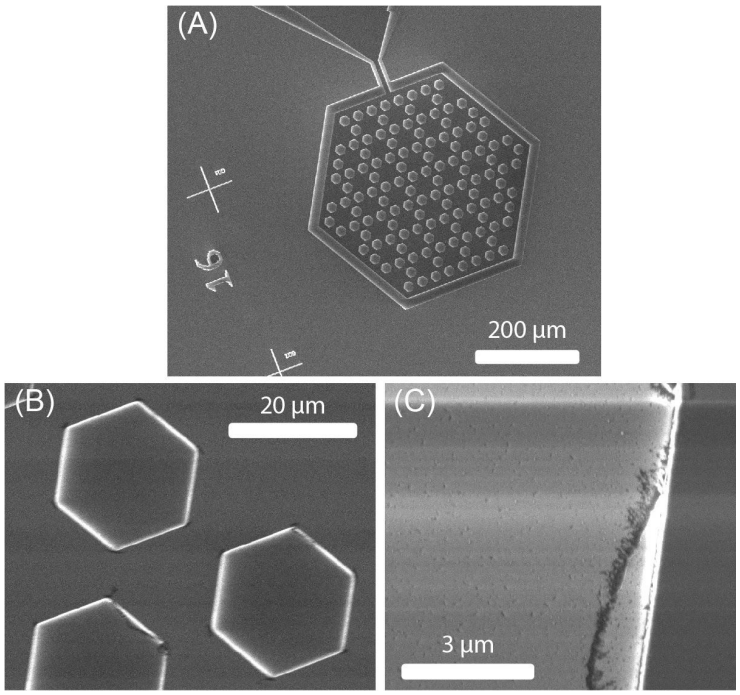

Figure 12. (A) Pattern of the bottom capacitor plate after SRS-100 & PRS-1000 clean; (B) Zoom into the hexagonal holes; (C) Etch edge contaminated by the resist-related residue.

Hydrofluoric Acid

As solvent-based cleaning procedures were not successful we decided to move to hydrofluoric acid it potentially can remove oxygen-containing compounds and, as we use oxygen in our etching recipe, we expected the film to be a mixture of oxygen, niobium and organic byproducts of the resist etch. In these tests we used two concentrations of the hydrofluoric acid solution in water:

- 10:1 HF:water
- 50:1 HF:water

Moreover, we explored utilizing the ultrasonic bath in post-HF water rinse, various times of the HF bath, placing the chip upside-down and additional ozone clean steps. All of the procedures were preceded by a standard resist strip in solvents, as described in section Solvents and Ashing. All of the cleaning procedures consisted of HF bath and 2-step water rinse afterwards to make sure that the entire acid is removed from the sample.

We started with a 10:1HF solution and checked results of 3, 6, and 9 minutes cleans followed by standard 2-stage water rinse under the SEM, results are presented in Figure 13. Picture (A) shows the state of a sample after resist stripping, inset shows the sidewall profile, picture (B) shows sample after 3 minutes clean in 10:1 hydrofluoric acid:water solution clean, (C) shows sample after 9 minutes clean in 10:1 hydrofluoric acid:water solution clean. It can be seen that 3 minutes in HF solution help to remove the entire residual film from the sapphire substrate, but leave small, black particles. This procedure very effectively cleans the sidewall residue and we can see a sharp edge of the Niobium film. The residue color suggests lower conductivity, hence, it might be a resist-related residue. After 3 minutes it is scattered uniformly around the chip, in small chunks, however, after 9 minutes we notice that it coagulates into larger particles.

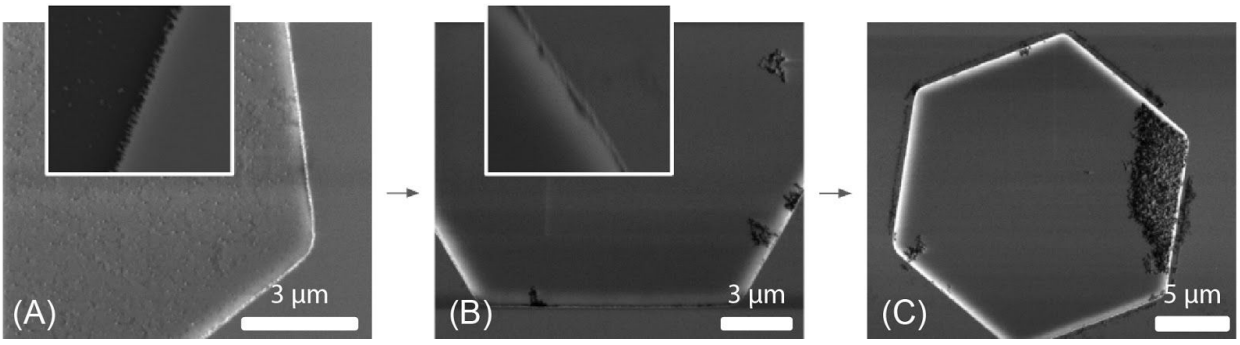

Figure 13. (A) Sample contamination after metal etch and solvent resist stripping; (B) Surface after 3 minutes of 10:1 hydrofluoric acid:water solution clean; (C) Surface after 9 minutes of 10:1 hydrofluoric acid:water solution clean. Insets show the etch sidewall.

After determining that the hydrofluoric acid can effectively remove the post-etch residue we focused on cleaning the small particle residue. To do this we tried 10:1 and 50:1 HF:water solutions and included an ultrasonic bath in hope that we can remove the particles. The general scheme of the procedure was:

1. Mounting chip upside-down on a teflon holder
2. HF rinse for a certain period of time
3. Water rinse for 30 sec
4. Water rinse for 30 sec
5. Transfer the beaker with water and chip to the ultrasonic bath, sonication for 5 minutes

The entire cycle was repeated twice for 50:1 and 10:1 HF solutions, for each we tried 3x30 sec and 3x3 minutes in HF. Results are presented in Figure 14. Image (A) shows the results of just solvent clean, (B) and (C) give results of 3x3 min in HF solution with ultrasonic baths in between for 10:1 and 50:1 solutions, respectively. The results of these procedures were not successful, 50:1 solution was not strong enough to remove the residual film, ultrasonic bath in between 10:1 solution cycles did not remove the small-particle residue but prevented their aggregation.

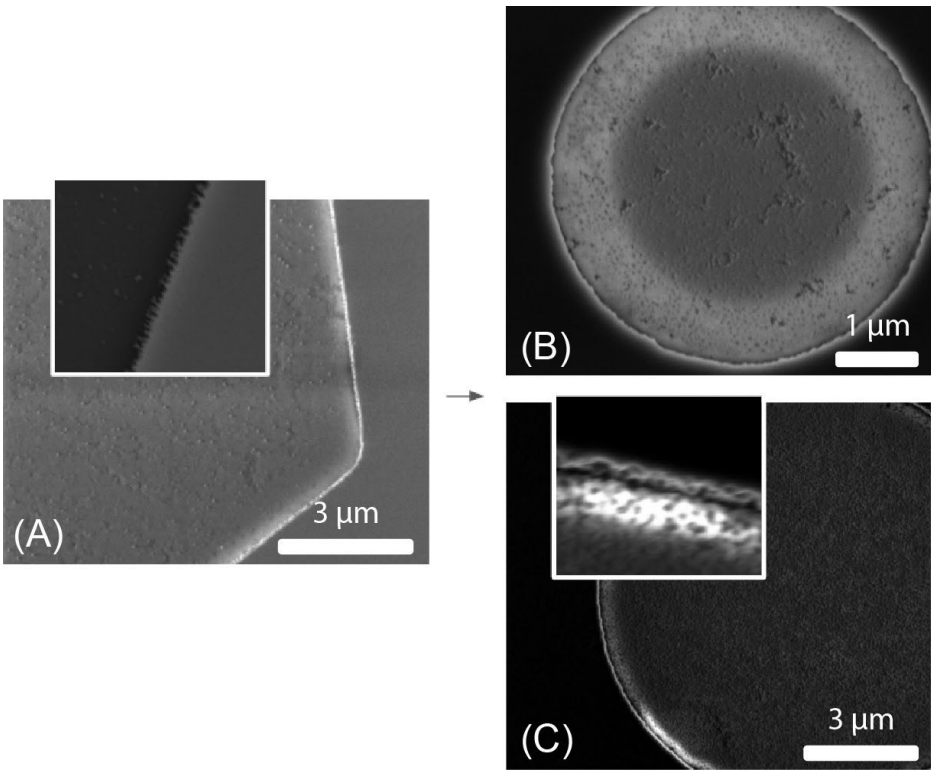

Figure 14. (A) Sample contamination after metal etch and solvent resist stripping; (B) Surface after 3x3 minutes of 10:1 HF:water solution clean and ultrasonic bath; (C) Surface after 3x3 minutes of 50:1 HF:water solution clean and ultrasonic bath. Insets show the etch sidewall.

Because modifications of the acid clean procedure did not give satisfying results we explored additional steps of UV ozone clean using *Samco UV Ozone Cleaner* in Stanford Nanopatterning Cleanroom. For this test we used samples that have been cleaned for 3 and 9 minutes in 10:1 HF:water solution. We tried ozone clean procedures at 60°C with UV lamp, time ranging from 5 to 20 minutes, and gas flow of 0.75 L/min. As a result of this study, we determined that 20 minutes of additional ozone clean after the 3 minute-long hydrofluoric acid clean is successful in removing the small residual particles from the sample. The results are shown in Figure 15. Images (A) - (B) show the initial state of the sample and result of 3 minute HF clean, picture (C)

is a result of 20 minute long Ozone clean procedure, it can be seen that it removes residual particles effectively.

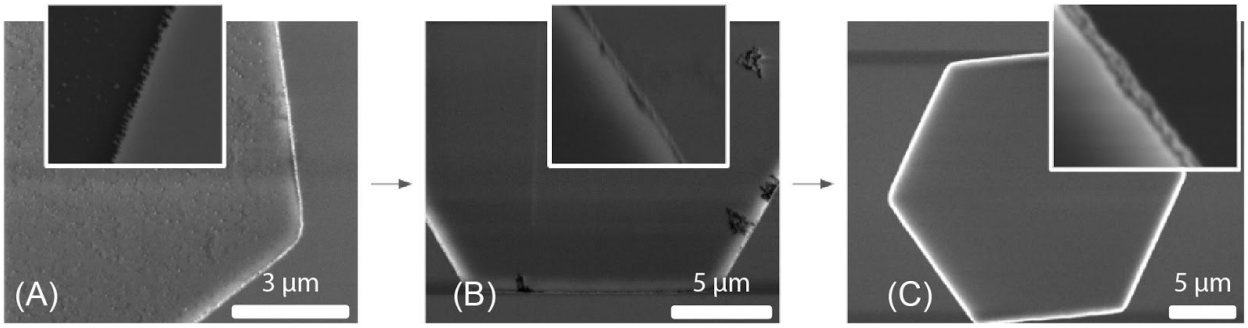

Figure 15. (A) Sample contamination after metal etch and solvent resist stripping; (B) Surface after 3 minutes of 10:1 hydrofluoric acid:water solution clean; (C) Surface after 3 min HF clean and additional 20 minutes UV Ozone procedure at 60°C, gas flow 0.75 L/min.

Releasing Non-planar Niobium Structures

Releasing these structures is a critical step in our process, thus most of our work for this quarter revolved around it. Removing the oxide layer is important because in general, dielectrics in superconducting devices give rise to extra loss and have a negative impact on the performance. The following section discusses how we managed to release these structures. Since we were a group of three people, we explored two methods of releasing simultaneously: Vapour HF (with the uetch tool in SNF) and Wet HF (as we described in the Post-metal etch cleaning procedure section).

Vapour HF

The SPTS uetch vapour system uses anhydrous HF and ethanol at reduced pressure and 45 Celcius to etch isotropically sacrificial silicon oxide layers, primarily to release silicon microstructure in MEMS devices. In our case, we are releasing Niobium microstructures with a silicon dioxide sacrificial layer. This dry process avoids sticition of released moving parts, which damages the structures - common issues with the conventional wet processing technology. The uetch is a single wafer system for 4 inch to 8 inch wafers and dies on a carrier wafer. As a user, we can control the following parameters in this tool:

- Recipe number: there are 5 pre-set recipes. If you want to create a new one, you need to contact Uli and have a very good reason.
- Etching time: minimum is 240 seconds, maximum is 600 seconds.
- Number of cycles: minimum is 1, maximum is 99.

It is **critical** to remove any polymer/organic material from your sample before putting it in the uetch. If you do not remove organics properly, then you contaminate the chamber and the tool will have to be shut down. There are two popular options to decontaminate your sample, before using uetch:

1. Bake 2 minutes @ 250 C
2. Gasonics (O_2 descum plasma)

Always follow the manual for your safety. Vapour HF is nasty and calcium gluconate cannot help you if it gets into your eyes/lungs, as with wet HF.

Important: Hinge of the uEtch is broken. So we need to hold the door and balance it on the base with two hands, before placing the sample inside.

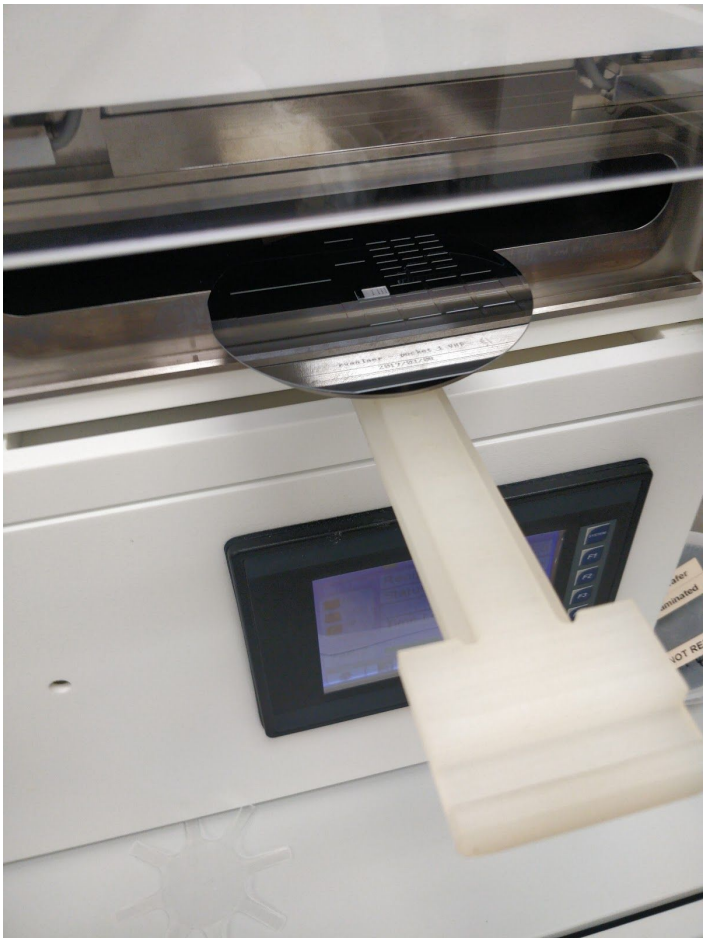

Figure 16. Image of our carrier wafer with a chip placed in one of the inserts. This chip is 5mm x 10 mm. The carrier wafer is a silicon wafer processed to have 1800 micron deep inserts of several dimensions.

Since we work with pieces in our fabrication procedures, we needed a method to hold the pieces in place, while the tool is etching. The reason we need a way to secure the chip is because the uetch shoots low volume, high pressure bursts of vapour HF, ethanol, and N2 in various steps of the etching process. These bursts may cause the chips to flip upside-down during the process destroying the sample in the process. In order to reduce the probability of this occurring, we place the chip in an insert etched in a Silicon carrier wafer. This carrier wafer has several die dimensions, so that we can reuse it for various piece sizes (see Figure 16). The inserts are 1800 micron deep, etched via an RIE process. This wafer was provided to us by a post-doc in the Safavi-Naeini group.

In our first releasing attempt, we used the calibrated etch rates provided in the instruction manual for recipe 5 (R5). According to the manual this is the fastest etch. We pre-processed the sample by doing a standard O_2 descum using the Gasonics. We did 5 cycles of 600 s of etching time per cycle. This was a beautiful failure, as shown by Figure 17. The optical microscope image (Figure 17 (A)) shows interference fringes, indicating that there is a thin layer of unknown origin deposited on the chip which has local and global height variations across the sample. The SEM micrographs show the entire pattern covered with a layer that exhibits microcracks (Figure 17 (B, C)). The fracturing patterns we observe in these SEMs do not follow intuition of how the

Niobium should fracture - we do not expect such brittle fracturing. From this we had two conclusions (1) that the Gasonics did not respond well to our material stack and that in the future, we will use the 250 C bake to drive off polymers; (2) 5 cycles of 600 s etching is too much.

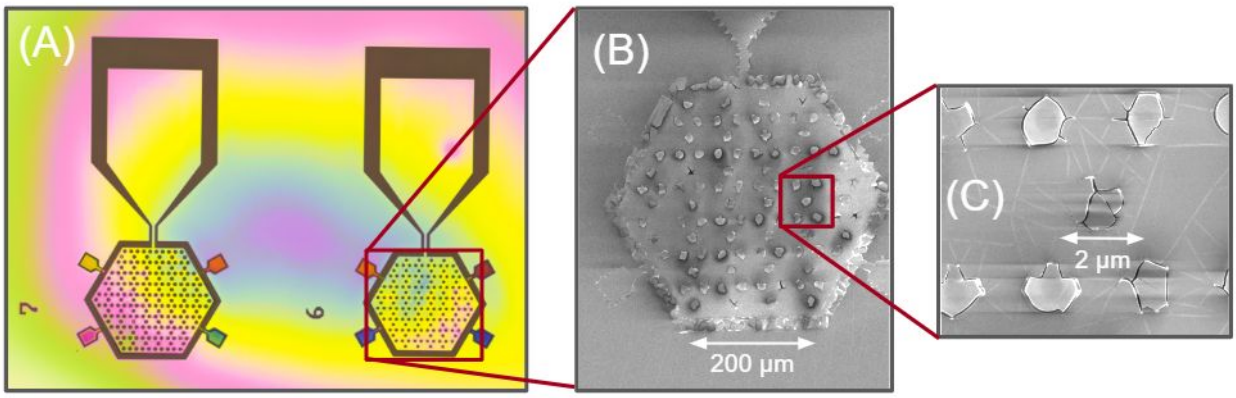

Figure 17. (A) Optical microscope image of a sample that was processed by 600 s x 5 cycles of VHF. (B) SEM image of the top layer, showing that there may be a thin-film of another material on the surface. (C) Zoomed in of (B) showing the cracked holes.

Next, we tried two more conditions for releasing. Figure 18 (A) shows the first condition: R5, 300s x 1 cycle. This time there were no interference patterns as shown above. Under the SEM, we see there exists partial undercut, but lots of bending of the film on the edges of the capacitor (peeling effect). This indicates that there exists local stress gradients. The inset in Figure 18 (A) shows a close up of the HF release valve (hole) and the posts. Figure 18 (B) shows the second condition: R5, 600 s x 1 cycle. Here we see that the undercut reaches so far inside that the local stress gradient snaps the posts and causes the top Niobium film to curl up - exaggerating the peeling effect seen in Figure 18 (A).

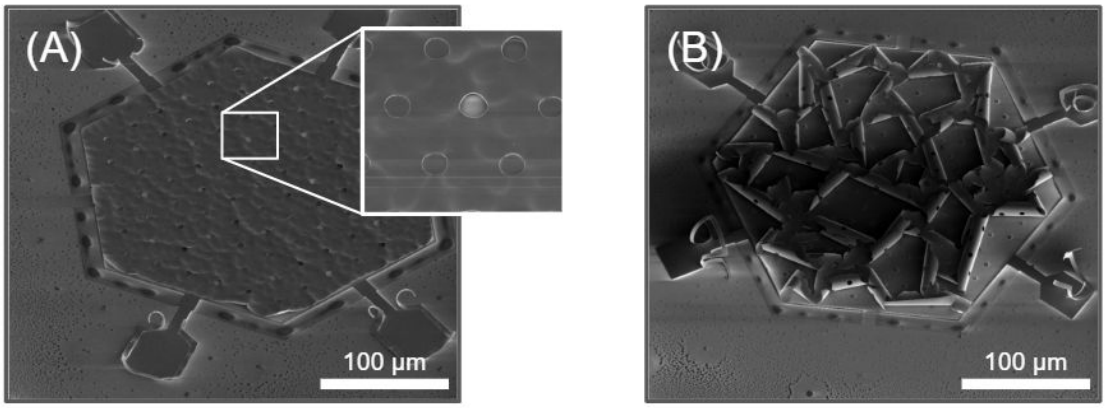

Figure 18. (A) SEM image of a test capacitor processed with 5 minutes in VHF using Recipe 5 in uetch. (B) SEM image of a test capacitor processed with 10 minutes in VHF using Recipe 5 in uetch.

Since these released capacitors have high local stress gradients we did not characterize the rate for R5. We postulated that this bending, peeling, and curling was due to the uncontrolled, high etch rate intrinsic to R5. So, we decided to use R1 on the tool.

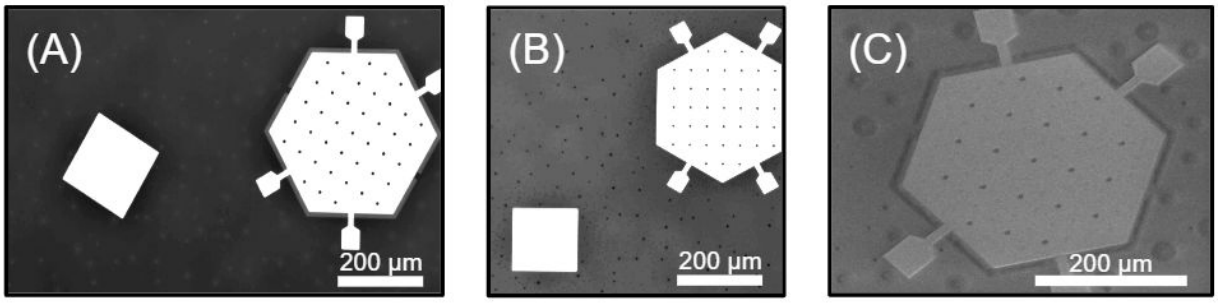

Figure 19. (A) Optical microscope image of profilmetry box and test capacitor. We can see speckles in the surrounding space - which are point defect sites caused by debris. (B) SEM image of the same location as the optical image, after R1 300s x1 cycle VHF. We see that the craters closely match up with the debris sites. (C) Zoomed in image of a test capacitor after R1 300s x 1 cycle VHF. This SEM image shows the craters in higher detail.

Finally, we attempted release using one more condition: R1, 300s x 1 cycle. We conducted profilometry measurements before and after exposure to VHF and determined the etch rate for this recipe to be 28.2 nm/min in the z-direction. We make the distinction that this rate is in the z-direction because the etch is generally faster along the plane and we did not characterize this rate. Note that rate is calculated by dividing the height difference with the set etch time, 300s (5 minutes). This VHF condition seemed to be acceptable, except there is one big issue: we observe 'craters' all across the chip. We tracked these craters to be debris sites that are present before the VHF. The VHF finds these sites and etches them much faster than the surrounding area. Figure 19 (A-C) shows the progression of these craters. We care deeply about the cleanliness of our chips and realized that if we release our structures in uetch, and know that there are point defects present it will be very difficult to do any type of cleaning procedure. This is because with released structures, we cannot pursue wet cleaning procedures, like the post metal etch cleaning procedure. Therefore, we decided to focus on the pursuit of the wet HF release, where we can clean and release simultaneously.

Liquid HF

In parallel to the vapour HF process we have been developing a releasing recipe using a 10:1 solution of hydrofluoric acid and water as we already determined that it does not harm the niobium surface. In this approach we utilize a HF etch step, when the chip is mounted on a teflon holder, following this we do 2-stage rinse with fresh water. After two rinses we remove the chip out of the holder and rinse it two more times with fresh water and leave it in a water beaker for 5 minutes to make sure that we remove all of the acid out of the released structures. After this procedure we typically transfer the sample to a beaker filled with 2-propanol to prepare it for a critical point drying.

To determine the proper releasing time we ran short etching steps in 10:1 HF to estimate the etch rate of the solution. We have run 30 seconds and 2 minutes procedures for this purpose, results are presented in Figure 20 (A), (C); and (B), (D), respectively. After a 30 second process it can be seen that some of the oxide layer is still present on the sample, we measure the etch depth with a profilometer and determine the etch rate to be 200nm/min. The 2 minute long process effectively removed all of the planar oxide layer (picture (B)) and resulted in an undercut that is visible in picture (D) and its inset.

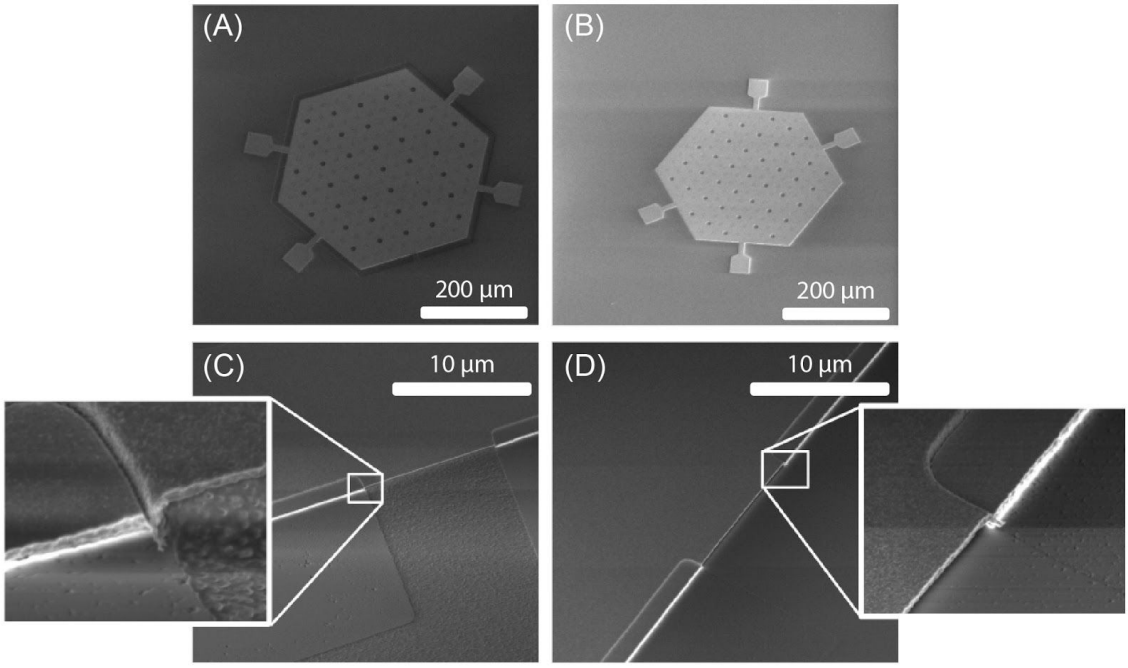

Figure 20. (A) Capacitor plate after 30 sec 10:1 HF treatment; (B) Capacitor plate after 2 min 10:1 HF treatment; (C) Zoom into the plate shown in (A), part of the oxide layer is still visible; (D) Zoom into the plate shown in (B), all of the planar oxide is removed, niobium structure shows an undercut.

Based on the etch rate we estimate that to etch under all of the structures we would need around 38.5 minutes, however, we anticipated that the horizontal etch can be faster than the vertical as the acid can potentially penetrate the structure faster along defect sites. For this reason we ran etching processes ranging from 7.5 to 38.5 minutes. The longest etch destroyed the sample and caused the top niobium layer to lift off, what can be seen in Figure 21 - only the parts of the pattern that are supposed to be in contact with the substrate survived. This can be potentially used as a liftoff procedure of niobium, as using typical resist liftoff is difficult due to the high temperature of the material during evaporation.

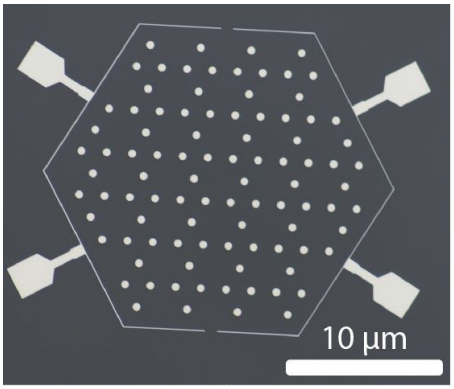

Figure 21. Damaged sample after 38.5 minutes processing in 10:1 HF solution.

Shorter processes ranging between 7.5 and 14.5 minutes seemed to etch silicon dioxide without damaging niobium. Example results of a 13.5 minute long etch process are presented in Figure 22. Picture (A) is a top-view on the complete 3-layer released capacitor, it can be seen that the support posts, formed by a circular structure evaporated in a hexagonal cutout of the bottom plate on picture(B), are intact. From picture (B) we can also see that the circular hole is cleared of the silicon dioxide, this is where the hydrofluoric acid penetrated underneath the top niobium plate. In the picture (C) we can see that the parts of the top niobium that didn't have firm support were released and are bending up. In picture (D) we see that the top capacitor plate is clearly undercut and the top plate is not shorted with the input wire going underneath it to the bottom plate.

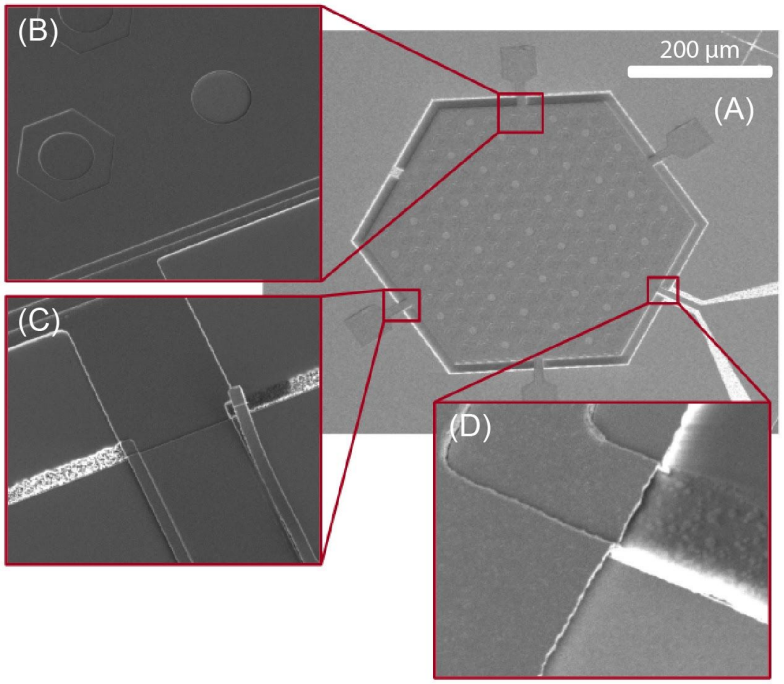

Figure 22. (A) Top view of the released parallel plate capacitor, top plate is attached to the ground plane with pads on edges, (B) and (C) show zoom in two of these; (D) zoom into an input line going under the top plate showing an undercut.

After the release we verified that the entire structure is released by cleaving the chip across a row of devices and imaged it under the SEM, results are presented in Figure 23. We cleaved the chip at an angle, which allows us to see different cross sections for neighboring devices, as shown in picture (A). Next we image three of them at a high angle (~88°) - pictures (B)-(D), it can be seen that the device on the picture (B) is not cleaved and we can clearly see the input wire going under the top capacitor plate. The next device - (C) is cleaved very close to it's edge and (D) is cleaved across the capacitor. Pictures (E) and (F) show the capacitor gap at higher magnification, we see that the gap is uniform which means that all of the silicon dioxide was removed. Picture (E) shows one of the posts that was cleaved through.

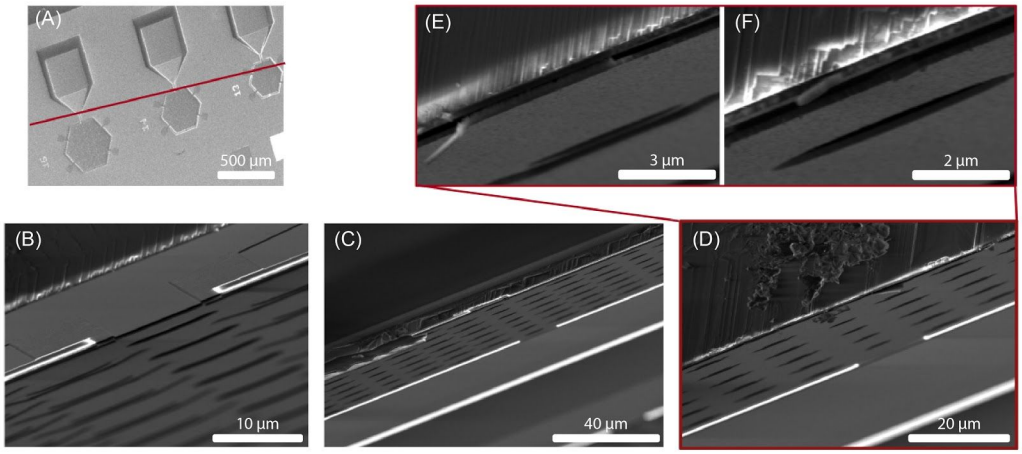

Figure 23. SEM images of a cleaved capacitor chip: (A) Cleaving line across a row of devices; (B)-(D) high angle SEM images of the chip facet; (E)-(F) zoom into (D) showing a gap between capacitor top and bottom plates.

Another method of verification of our releasing process was mapping the structure with a scanning confocal microscope, shown in Figure 24 (A)-(B). In the results we observe a smooth surface of the top niobium plate with height vs. the sapphire substrate (blue areas in the map) around 530 nm. The smooth surface suggests that the capacitor was not collapsed, the top plate does not bend downwards in the direction of the bottom plate. Moreover, the measured height profile suggests that the capacitor gap shrunk from 200 nm to about 130 nm, possibly due to the strain induced into the top plate after releasing, this value has been verified experimentally during the capacitance measurements in section Capacitance Measurements.

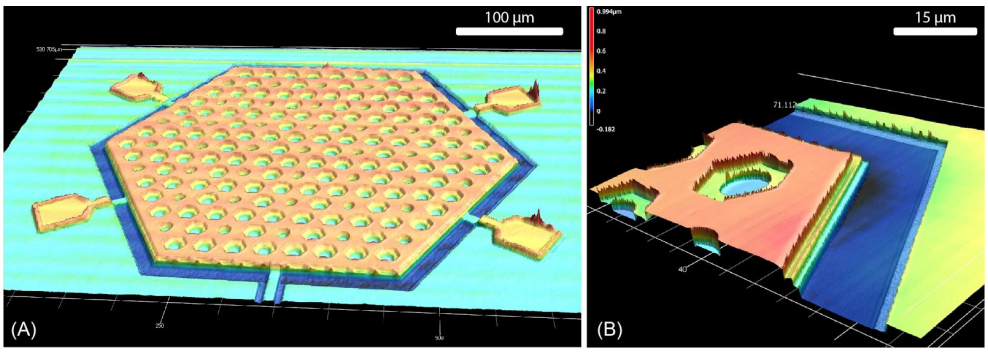

Figure 24. (A) 20x magnification laser confocal microscope mapping of a released capacitor; (B) 150x map, zoomed into a corner of the capacitor from (A).

Critical Point Drying

Drying released structures at a critical point is a promising way to prevent microstructures collapse as a result of capillary forces during a typical drying process. In the SNF we had an opportunity to use Tousimis 915B Critical Point Dryer (badger: *cpd*). The principle of this process is to fill the chamber with a sample with liquid carbon dioxide and move it above its critical point, where capillary forces do not occur, and finish the process in the gas state.
While using the critical point dryer we noticed two issues:

- The tool generates a significant amount of particles that get deposited on samples.
- The tool exchanges the 2-propanol into the liquid carbon dioxide quite rapidly, resulting in liquid turbulence which might hurt delicate structures.

To solve the first one we cover the basket with our samples with a dummy wafer that catches most of the residual particles. To address the second issue we start the process with a closed “Fill” valve and gradually open it during the filling step to reduce turbulent flow.

We compared results of releasing with and without critical point drying, results are presented in Figure 25 using test strains structures as an example. We notice that the results after critical point drying do not seem better under optical microscope and the yield is lower for thin structures - top two rows, devices thickness equal 5 micrometers.

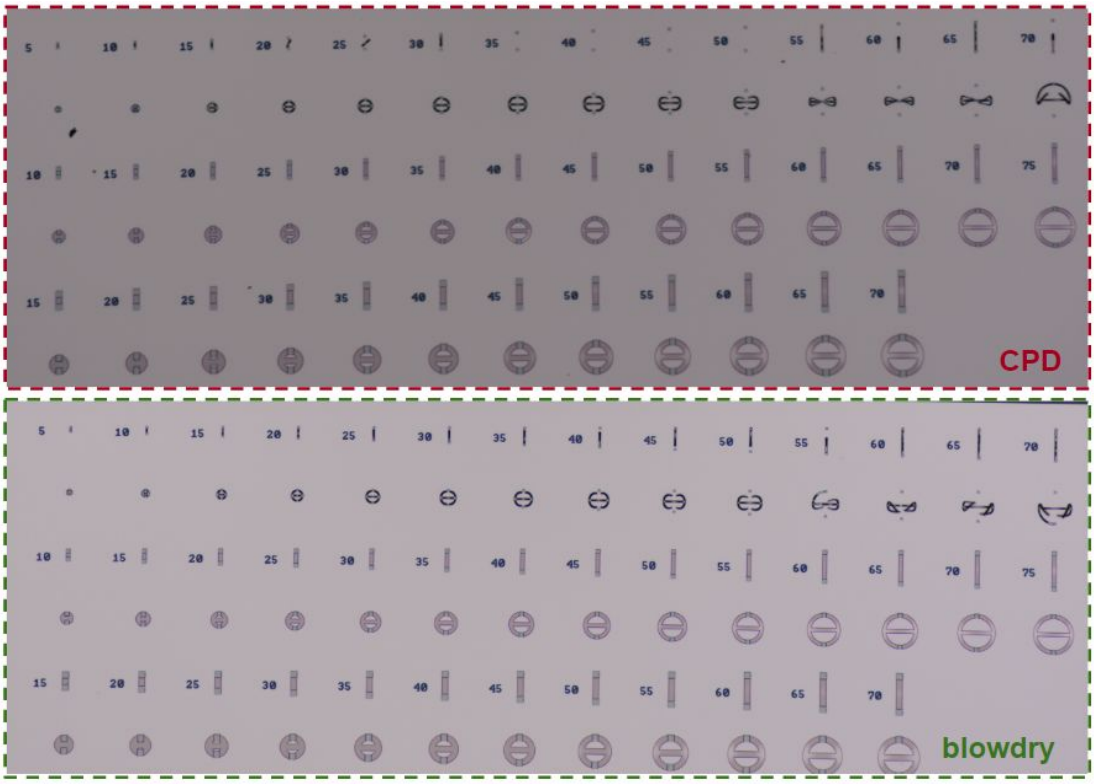

Figure 25. Comparison of released structures dried at the critical point (upper panel) and using nitrogen gun (bottom panel).

Critical point drying does not seem to impact released capacitors negatively and we confirmed that devices work so we decided to keep using it, however, it might be worth comparing devices that have been dried at the critical point and using a nitrogen gun to verify if using CPD is necessary.

Critical Point Drying SOP

As we have been using the Tousimis 915B Critical Point Dryer in SNF we improved the standard operating procedure as described above. The basic version of the Standard Operating Procedures for this tool is already available online but we propose a modified version that ensures higher yield of successful releasing and better overall cleanliness of the process on small chips:

1. Sample Preparation
    1.1. Rinse sample at least 3x in DI water at the flexible corrosive wet bench.
    1.2. Place the sample in Isopropyl Alcohol for at least one hour at the flexible solvent wet bench
    1.3. Place a dummy wafer in 2-propanol for at least 1 hour.
2. Prepare the tool and load samples
    2.1. Contact staff in charge and ask about availability of LCO2 (99.99%).
    2.2. Enable cpd.
    2.3. Record LCO2 weight in log sheet. One run uses 3 to 4 pounds of LCO2.
    2.4. Check valves:
        Fill 1.1
        Bleed 0.14
        Purge-Vent 0.15
    2.5. Turn off the Fill knob.
    2.6. “Chiller Power” press ON, wait for *30 minutes*.
    2.7. Press “Condenser Power” ON**.**
    2.8. Press “Chamber Power” ON (VENT light on), wait for *3 – 5minutes*.
    2.9. Remove the chamber lid and place it on aluminum foil.
    2.10. Check inside of the chamber lid, o-ring, inserts, and baskets for particles. Rinse off particles using IPA at the solvent bench, wbflexsolv, or use IPA on a thin cleanroom wipe.
    2.11. Check o-ring, if the o-ring is flat, shutdown the system and contact maintenance.
    2.12. Place 2 largest inserts, 4” basket and small, 4-chip basket, and 4 4” spacers in the chamber.
    2.13. Press VENT (VENT light will blink).
    2.14. Fill with 150 ml of 2-propanol.
    2.15. Transfer up to 4 chips directly from an IPA dish to the small basket.
    2.16. Cover the chips with a dummy wafer from IPA, placing it on 4 stacked spacers.
    2.17. Lower chamber lid onto chamber and use fingers to evenly tighten the 8 nuts.
    2.18. Tighten 8 nuts in a numbered sequence using the wrench and repeat until nuts are unable to tighten further. Don't overdo it.
3. Run the critical point drying process
    3.1. Set PURGE time to 10 minutes (15 minutes is max).

3.2. Press COOL (VENT light goes off, COOL light goes on), Temperature drops to 10°C within 4 minutes.
3.3. Once Temperature reaches 10°C press FILL (COOL light off, FILL light on).
3.4. Pressure starts going up, when it reaches 400 psi start opening the FILL valve gradually until you reach 1.1, you need to do this within 8 minutes of the initial FILL time. Pressure goes up to 800 to 900 psi.
3.5. Automatic switch to PURGE (FILL light off, PURGE light on), LCO2 will continue to fill the chamber, preset purge time will run.
3.6. Automatic switch to POST-PURGE-FILL (FILL and PURGE lights on), 4 minutes, LCO2 will continue to fill the chamber.
3.7. Automatic switch to HEAT. HEAT light will be on until the system reaches Critical Point, pressure rises above 1072 psi and temperature above 31°C. Pressure goes up to 1400 psi and temperature can reach up to 40°C.
3.8. Heat will blink for 4 minutes. Automatic switch to BLEED (HEAT blinking light off, BLEED light on), pressure drops in a rate of 100 – 150 psi/min, ~ 10 minutes.
3.9. Around 360 psi, automatic switch to VENT (BLEED light off, VENT light on), ~ 3 minutes.
3.10. Open chamber at 0 psi and loosen 8 nuts in reverse pattern (8,7…1).
3.11. Remove wafer, wafer should be dry, if not, contact SNF staff.

4. Turn off the tool
4.1. Clean chamber, lid, inserts, and basket with IPA and blow dry.
4.2. Place the lid back on the chamber, don't tighten nuts.
4.3. Press "Chiller Power" OFF
4.4. Press "Condenser Power" OFF
4.5. Press " Chamber Power" OFF
4.6. Fill out the log sheet.
4.7. Disable cpd.

Role of Annealing in Nb Structures Releasing Process

As metal films deposited on the sacrificial layer can be strained in a way that causes structures to buckle or collapse after releasing, we explored annealing as a way to relieve this built-in stress. For this purpose we have used an oven working in the atmosphere and annealed samples at 300°C for 30 and 60 minutes with a 3°C/min ramp down and up. It is important to include the annealing step before the releasing process, as doing it afterwards does not help. To show how critical the annealing procedure is, we compare results of the devices released with no annealing and with 30-minutes long annealing step in Figure 26 (A)-(C) and (D)-(F) for not-annealed and annealed chip, respectively. In pictures (A)-(C) we see buckling and structural damage of the top niobium plate as a result of stress in the film. In the SEM picture - (A) we observe that some support posts were destroyed and niobium is bending, mostly around the holes in the top plate, what can be also seen as 'bubbles' under optical microscope - picture (B) or hills and valleys in the scanning confocal microscope picture (C). When the sample is annealed before releasing - pictures (D)-(F) the surface is very uniform and smooth, we do not observe any buckling or damage under SEM (D), optical (E) or confocal (F) microscope.

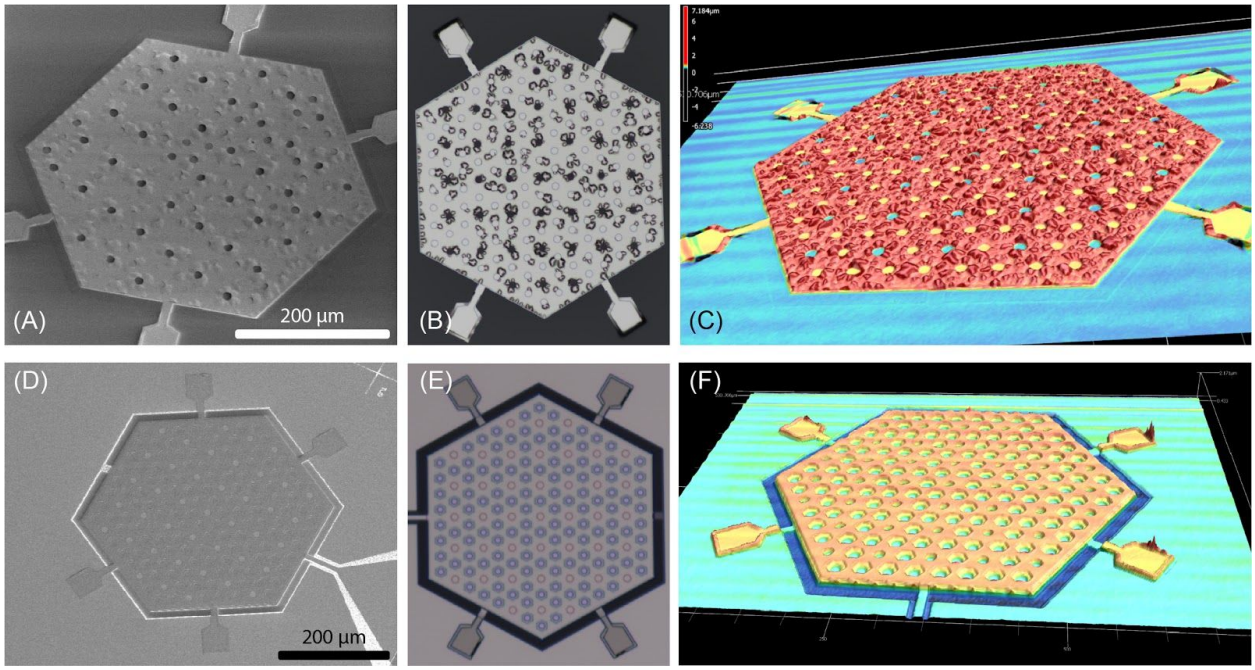

Figure 26. Pictures of a capacitor released without any annealing step (A)-(C) and with 30 min, 300°C anneal (D)-(F) under SEM, optical microscope, and scanning confocal microscope, respectively.

Niobium structures releasing SOP

As a summary of sections Liquid HF, Critical Point Drying, and Role of Annealing in Nb Structures Releasing Process we worked out a method for releasing niobium structures with high yield. We provide a runsheet of this process in Table 11 and present a standard operating procedure for this microfabrication process:

1. Prepare the samples for release
   - 1.1. Microfabrication with 2 or 3 mask processes with patterned sacrificial layer and niobium can be done following our runsheets.
   - 1.2. Anneal the sample at 300°C for 30 minutes in the atmosphere, 3°C/min ramp down and up. Keep the chip in an aluminum box during the process
   - 1.3. Mount the chip on a teflon holder, 1 teflon screw can hold 5x10mm^2 chip
2. Release samples
   - 2.1. Enable wbflexcorr
   - 2.2. Prepare the chemicals:
     - 2.2.1. Put the full PPE on
     - 2.2.2. Transfer a bottle of hydrofluoric acid using a cart
     - 2.2.3. Check the bench for any spills and blow them away
     - 2.2.4. 4 beakers of fresh DI water
     - 2.2.5. 1 beaker with 10:1 HF solution, recommend 100 ml of water and 10 ml of hydrofluoric acid. Add acid to water
   - 2.3. Releasing
     - 2.3.1. When transferring the chip between beakers be very gentle to avoid damaging released structures with turbulent flow

2.3.2. Immerse the holder with a chip in the HF solution for calibrated amount of time (13.5 minutes in our case), do not agitate
2.3.3. Transfer the holder to the first water rinse, agitate very gently for 30 seconds
2.3.4. Transfer the holder to the second water rinse, agitate very gently for 30 seconds, leave the holder in the water
2.3.5. Prepare tweezers and take the holder out of the water bath and remove the chip, do not let it dry
2.3.6. Rinse the chip in the third water beaker for 30 seconds
2.3.7. Move the chip to the fourth water beaker and leave it there for 5 minutes

3. Critical point drying
   3.1. Prepare a beaker with 2-propanol
   3.2. Transfer the chip from the fourth water rinse to the IPA
   3.3. Let the chip soak for at least one hour
   3.4. Load the chip into the cpd and run the drying procedure following the cpd SOP
4. Characterize results
   4.1. Take optical microscope pictures, check for film uniformity
   4.2. If film looks suspicious check under the scanning confocal microscope

Niobium Superconducting Resonators

Our main goal is to fabricate superconducting devices using Niobium. Since we established the Plassys e-beam evaporator tool as having acceptable room temperature resistivity last quarter, we wanted to characterize the superconducting properties this quarter. To do this, we fabricated standard superconducting quarter-wave resonators and measured them cryogenically. Our main goal was to characterize the transition temperature, T_c and the quality factor. To develop a holistic understanding of the measurement results, we would like to begin with a theoretical treatment of various designs involved in the setup and then discuss the measurements in detail.

Quarter Wave Resonators

A quarter-wave resonator at a specific frequency is a transmission line circuit generating standing waves when $l = \frac{\lambda}{4}$ with a short circuit termination ($Z_l = 0$). Whenever the frequency of the oscillator attempts to fluctuate above or below the resonator's center frequency, the $\frac{\lambda}{4}$-wave section looks like a low impedance that works to attenuate other frequency components. Hence this resonator typically has higher-Q factors.

CPW Geometry

For coupling the resonator to a feedline, we are going to use the **Coplanar Waveguide (CPW)** geometry (see Figure 27). This geometry ideally has a center strip conductor with semi-infinite ground plane on either sides, allowing the propagation of Quasi-TEM modes. CPW geometry has quite a few advantages over conventional microstrip circuits (a conductor fabricated on top of a dielectric layer, with a conductive metal ground plane on the bottom of the dielectric material). Some of these include easier fabrication techniques, avoiding vias, attaining an extra level of grounding and isolation, and avoiding radiation losses.

Due to its configuration, the CPW geometry has a capacitance associated with it. To simplify things, consider a conventional CPW structure having a signal trace S and gap W with an infinitely thick dielectric substrate. The capacitance of this CPW can be determined using conformal mapping techniques[15] will be given by:

$$C_{CPW} = 2\varepsilon_0(\varepsilon_r + 1)\frac{K(k_0)}{K(k_0')}$$

where: $\varepsilon_0, \varepsilon_r$ are dielectric constants of free space and the substrate respectively, $K(x)$ is the complete elliptic integral the first kind, $k_0 = \frac{S}{S+2W}$ and $k_0' = \sqrt{1 - k_0^2}$ (see Figure 27) .

Another important parameter that we like to keep track of is the characteristic impedance of this CPW structure, which can be given by[15]:

$$Z_{0\,(CPW)} = \frac{30\pi}{\sqrt{(\varepsilon_r+1)/2}} \frac{K(k_0')}{K(k_0)}$$

Hence we can see that the capacitance and characteristic impedance can be modified very easily by change W and S.

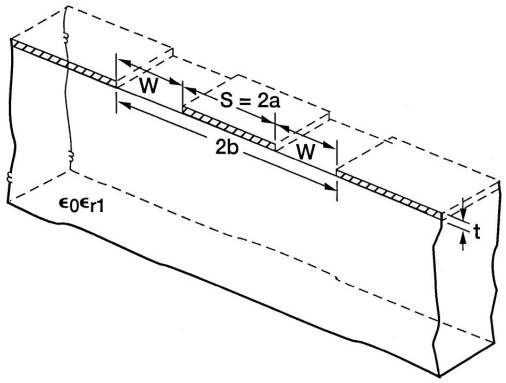

Figure 27. Conventional CPW geometry with semi-infinite ground planes on both sides of a strip conductor and infinitely thick dielectric substrate

Side-Coupler Design

Having discussed the CPW technology, we can now dive into coupling a $\frac{\lambda}{4}$-wave resonator to the microwave feedline. We have used a method called "side-coupling" to couple to the resonator, as shown in Figure 28[16]. In this diagram, we feed the signal using the feedline between ports 1 and 2, which interacts with a load Z_l at port 3.

This coupling is capacitive in nature and can be determined using the following formula:

$$e = \frac{2\,|S_{31}|^2 \omega_0}{\pi}$$

where, S_{31} is the scattering matrix element between ports 1,3 and $\omega_0 = \frac{1}{\sqrt{L_{CPW} C_{CPW}}}$; L_{CPW} being the inductance associated with the coupling section and C_{CPW} being the capacitance.

Figure 29 is the model designed for SONNET (software to perform high frequency EM simulations) following the general network model shown in Figure 28. In our case, we want to connect a λ/4-wave resonator, hence one of its ends is shorted as the theory of Quarter Wave Resonators suggests (notice the stripes in Figure 29).

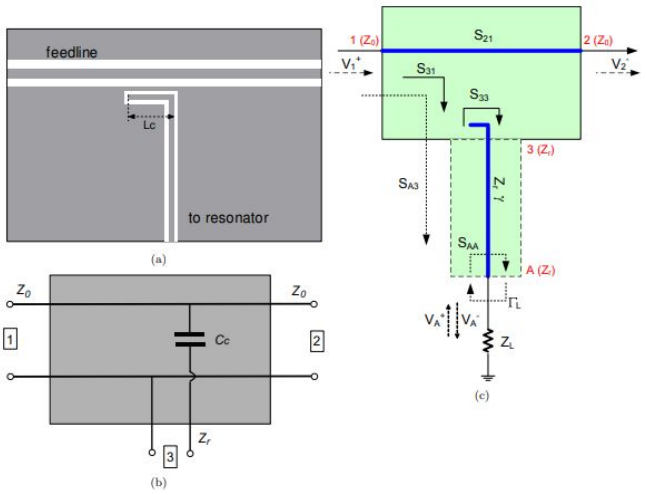

Figure 28. Network model of a λ/4-wave resonator coupled to a feedline using a side-section. (a) Design of the side-section coupler; (b) Equivalent lumped element model of the coupler; (c) Network model and signal flow graph of the coupler

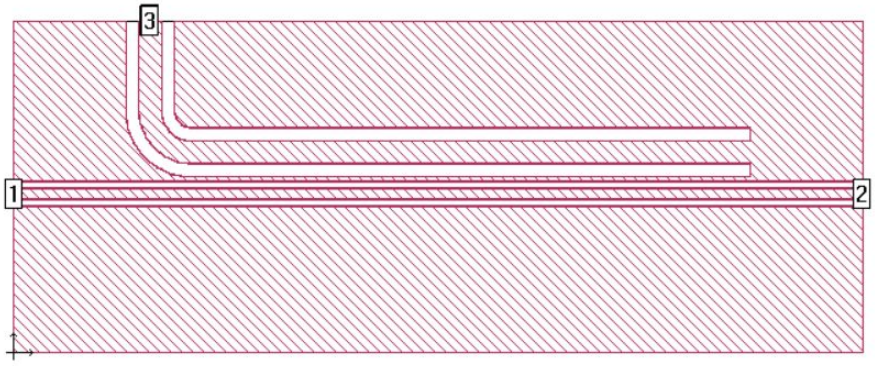

Figure 29. Shows the design of the side-coupler (one end shorted) with the signal feedline. Here, the striped section is metal (Niobium) and the blank section is substrate (Sapphire).

Cryogenic Measurements of Niobium CPW Quarter Wave Resonators

Based on the theory above, we modified a design made by Agnetta Cleland (Safavi-Naeini group). The design is a multiplexed quarter wave resonator device (see Figure 30). There are six resonators coupled to the main feedline (see Figure 3), 200 nm thick Niobium on 430 μm thick C-plane sapphire. The feedline is then wirebonded to a PCB signal trace, which is soldered to an SMP connector - Wentao Jiang (Safavi-Naeini group) helped us with wire bonding and Nathan Lee (Safavi-Naeini group) helped us with soldering to the SMA connector. We then use SMA cables to connect to a Vector Network Analyzer (VNA) which measures transmission and reflection coefficients. Figure 30 shows the design layout for the resonators. Note, the feedline and resonator were designed to have a characteristic impedance of 50 Ohms.

There are thicker resonators and thinner resonators, this was to test if scaling the thickness of the signal traces would have an impact on the quality factor of the resonator (scaling the signal trace width/ground plane spacing ratio does not change the characteristic impedance). The thinner resonators have a 10 μm signal trace and the thicker resonators have a 20 μm signal trace.

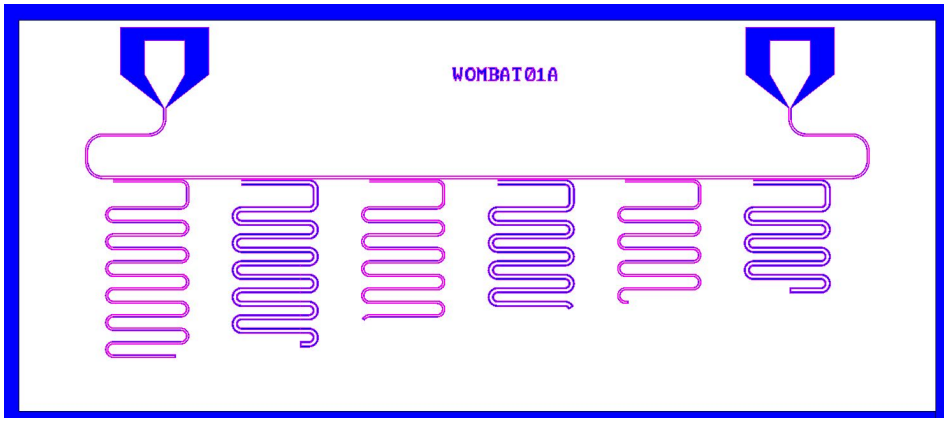

Figure 30. Shows the layout of the planar resonator device (named WOMBAT01). The areas that are filled in are the areas that will be etched to substrate (Sapphire).

During the fabrication, a piece of debris covered the leftmost resonator's signal trace and rendered it out-of-commission. So we do not expect to observe a resonance from this resonator.

To conduct cryogenic measurements we placed our device in a Montana Instruments Cryostation, which has automated temperature control and can reach 4 K base temperatures. Figure 31 shows data taken at base temperature. We see five resonances near the frequencies we engineered them to be (see Table 1). The thin resonators are designed to be separated 1 GHz apart with respect to each other and the thick resonators are also designed to be separated 1 GHz apart.

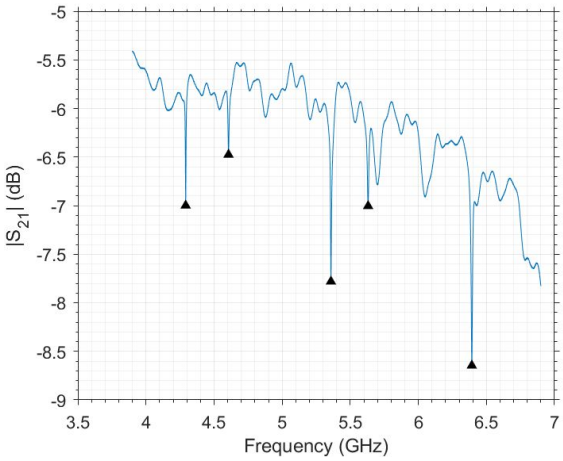

Figure 31. VNA trace at 4K of the planar resonator device. There are only five resonances because one of the resonators (the leftmost one in Figure 33) had a broken signal trace.

Here is a tabulated summary of the measurement results:

Frequency (GHz)	Signal Trace Width (μm)	Qe	Qi
4.291644247	20	5896	845
4.60557925	10	5762	496
5.357801569	20	3662	724
5.631447014	10	3762	419
6.393568254	20	2442	627

Table 1. Measurement results for the multiplexed planar resonator device.

We see that the frequency spacing is what we expected. Additionally, we find that the thicker traces have systematically higher internal quality factor (Q_i), which answers one of the questions we had about these resonators. Additionally, Figure 32 shows a temperature sweep experiment we conducted to determine the superconducting transition temperature of our Niobium. The colors indicate the absolute value of the transmission coefficient in a decibel scale. We observe that at ~ 7.1 K there is a sharp change in the transmission, which indicates a superconducting transition. As we consider lower temperatures (near the top of the figure) we find 'streaks', which are the resonators. We expect the resonators to red shift and broaden in frequency as temperature goes up because of increased loss. At some point the temperature becomes so high that we cannot resolve the resonances anymore - which is what we observe.

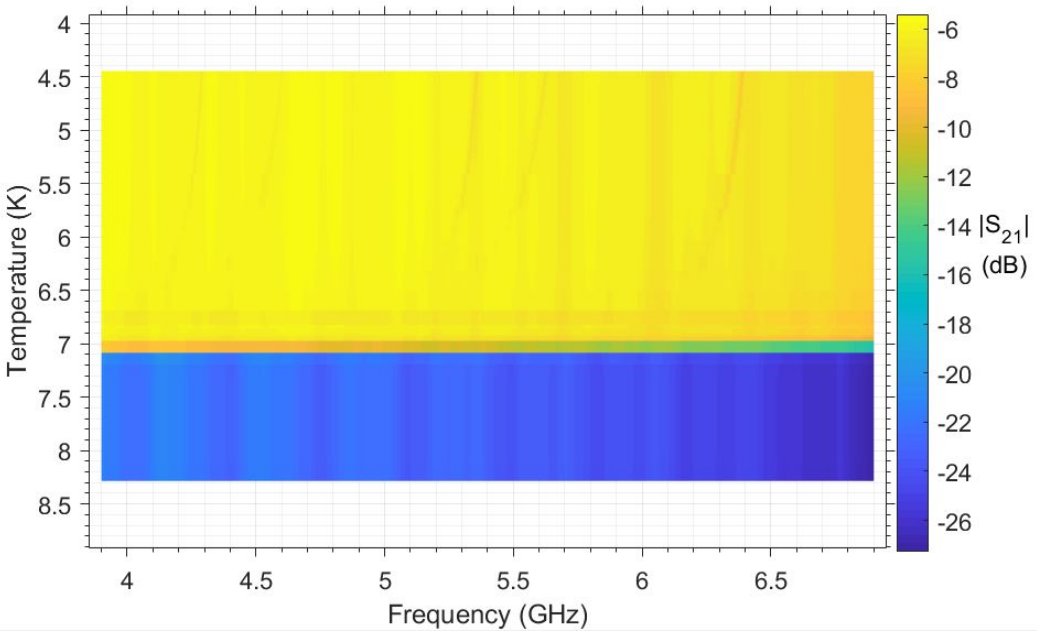

Figure 32. Temperature sweep experiment for WOMBAT01 device. We can see 5 streaks at lower temperatures showing that the resonators red shift (lower frequency) as temperature increases. At ~ 7.1K there is a sharp change in transmission, which we attribute to a superconducting phase transition.

Non-Planar Design

In this section we describe some principles on how we model the parallel plate capacitor and the process of how we're engineering the resonators that incorporate the parallel plate capacitor. Our capacitors are modeled as standard parallel plate capacitors:

$$C_0 = \frac{A\,\varepsilon}{d}$$

Where A is the net area, $\varepsilon = k\varepsilon_0$, k is the dielectric constant, and d is the distance between the plates. We make the distinction that A is the *net* area because our parallel plate capacitors have holes (to let the HF through and release the structure). Additionally, we have posts as well that contribute to some parasitic capacitance. We subtract the area of the HF release holes and posts. We don't include the contribution of the parasitic capacitances because we are modelling these as capacitors shunting a large capacitance, so their contribution is negligible. In the measurement section, we will see that the parasitic capacitance argument breaks down when we release the capacitors.

To make resonators out of these capacitors, we need to design inductances. In the first iteration, while we still develop lumped element spiral inductors, we decided to use wire inductances from a CPW geometry. The CPW geometry lends itself to conformal solutions of the field-equations so we can calculate inductance and capacitance per unit length of such configurations using standard closed form solutions[15]. We can derive a quadratic equation for the length of wire needed for a particular parallel plate capacitance, C_0, resonance frequency f_0, inductance per unit length L_{cpw}, and capacitance per unit length C_{cpw}:

$$l^2\,(L_{cpw}\cdot C_{cpw}) + l\,(L_{cpw}\cdot C_0) - \frac{1}{4\,\pi^2 f_0^{\,2}} = 0$$

This equation incorporates the capacitance per unit length of the CPW and the solution gives us the length of CPW needed to have a resonance frequency at f_0 given a parallel plate capacitance C_0.

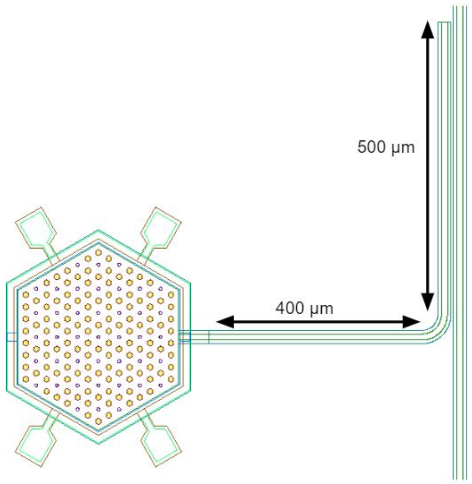

Figure 33. A resonator design using a wire inductor, coupled to a feedline. The total length of this resonator was calculated to be 900 microns, to give a resonance frequency of 5.1 GHz.

Figure 33 shows an example of one of our nonplanar designs with two dimensions labelled. The different coloured lines indicate different layers in the CAD design file. Here we see all of the layers (bottom, middle, top) superimposed on top of each other - see Mask Design section for details. The coupling section of the resonator is denoted by the 500 micron wire segment. The length of this was determined by the SONNET coupling full-wave simulations discussed previously. We care about the length of this section because it directly is related to external quality factor Q_e - the ratio of the energy stored in the resonator and the energy lost to the feedline (over one resonator period). Knowing this number accurately lets us understand the internal quality factor Q_i of the resonator, which gives us a metric to compare the quality of our devices. The 400 micron segment is to have a total wire length of 900 microns, calculated by the quadratic formula above. This design, with capacitance C_0, and inductance given by the 900 micron wire supports a resonance at 5.1 GHz.

Parallel Plate Capacitors

The main purpose of this project was fabricating released, vacuum-gap parallel plate capacitors described in detail in section Superconducting Parallel Plate Capacitors. In the following paragraphs we address our approach to the mask design (Mask Design section) and present measurement results for dielectric-gap and released devices (Capacitance Measurements section).

Mask Design

In the design process we had to arrive with a mask layout that allows for:

1. Firm support of the top plate without shorting it with the bottom one;
2. Quick access to the sacrificial layer for the HF solution in the entire SiO_2 area;
3. Patterning other components in other areas of the chip;

To address all of these challenges we design a 3-mask process, each mask is visible in Figure 34. Niobium bottom plate is patterned with mask 1 - picture (A), oxide sacrificial layer is patterned with mask 2 - picture (B), and niobium top plate is etched with mask 3 - picture (C).

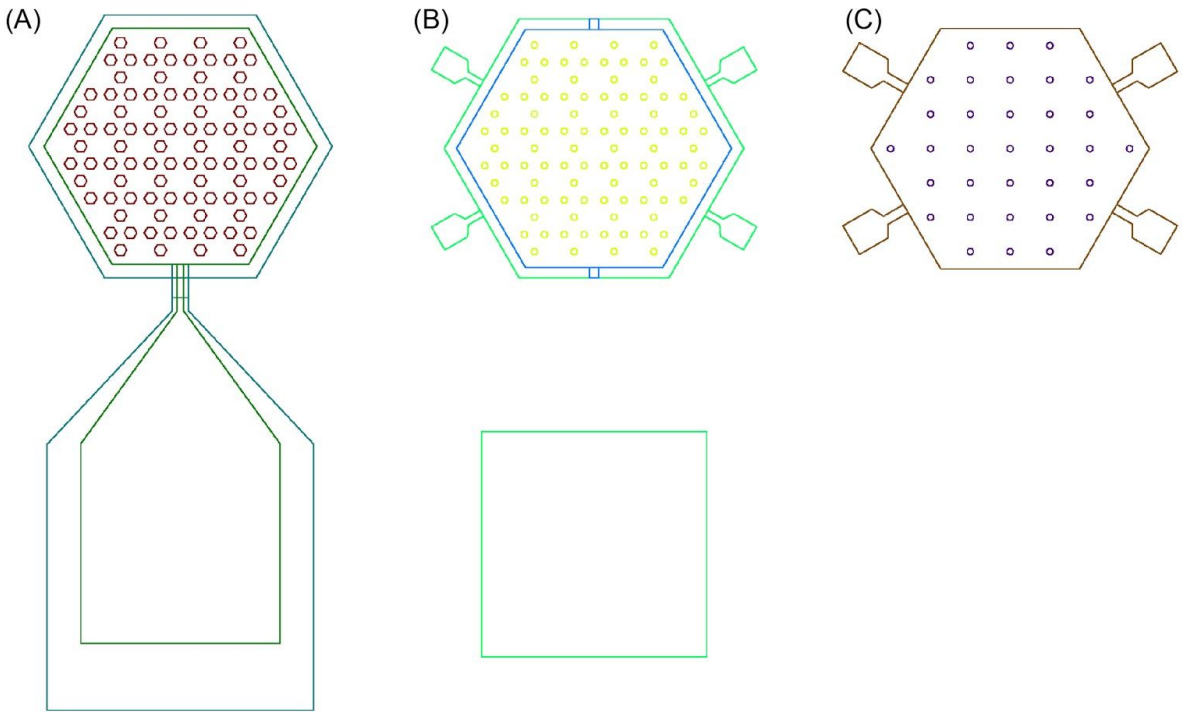

Figure 34. Example test capacitor masks, (A) Bottom Nb plate mask; (B) Sacrificial layer mask; (C) Top Nb mask.

In mask one we cut the blue layer out of the ground plane, add the green layer to form the bottom plate and a contact pad, and cut the red hexagonal holes out of it. These holes allow to form posts for support of the top plate. Ground plane is patterned with this mask as well and

allows for patterning any other Nb structures, they will be protected during the rest of the processing by an oxide layer which will finally be removed in the HF solution.

In mask two we cut the light green pattern out of a ground plane - the large rectangle allows us to access the contact pad and small pads around the capacitor make vias in oxide for ohmic contact between the ground plane and the top plate from mask 3. Next we add the blue layer to form the sacrificial layer between capacitor plates and make holes using the yellow layer. These holes are aligned with red hexagons from mask 1 but their size is smaller, this ensures that the top plate cannot be shorted with the bottom one.

Finally, mask three is a pattern given by the brown layer with circular cutouts done with the purple layer. The topl plate covers the entire sacrificial layer and forms contact with the ground plane of mask 1 with pads on the edges. Circular cutouts are aligned with empty space on masks 1 and 2 and their purpose is to give easy access of HF solution to the sacrificial layer for effective removal.

Capacitance Measurements

We characterized our capacitors using the micromanipulator6000 tool in the SNF. This tool is a complete IV and CV measurement solution from basic IV to various capacitance measurements such as CV, capacitance versus time (C-t), capacitance versus frequency (C-f) and Quasi-Static CV (QS-CV) in a box. Additionally, there is also a guard switch unit (GSWU) which is used to short the guard of the measurement cable while CV measurements are performed. The GSWU switch opens automatically during IV measurements to prevent potential SMU damage, since otherwise the guards of the two SMUs (which are presumably at different potentials) would be shorted together. To conduct CV measurements you *must* use SMU3 and SMU4 on the tool. Additionally, this tool takes care to de-embed the capacitances of the tool, so we do not need to remove these parasitic capacitances in post-processing.

Figure 35 shows a camera phone image through the microscope of the micromanipulator6000 tool. We place one of the probes on the signal pad and one of the probes onto the ground plane and take a CV measurement. We place the second probe directly to the ground plane to check if there is good contact between the top layer of Niobium and the ground plane. To confirm the measurements were consistent, we checked the capacitance values of when we placed the second probe directly on the top layer of niobium by probing one of the four contacts on the edges of the capacitor. Additionally we double checked our capacitance measurements by varying frequency - the capacitances remain constant with frequency.

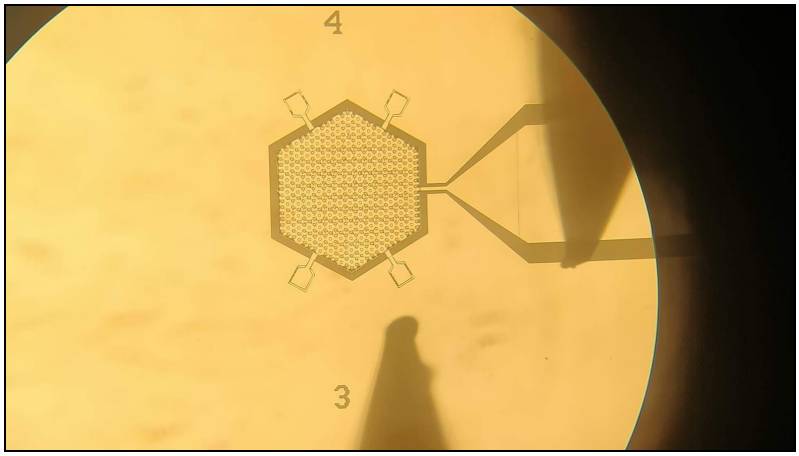

Figure 35. Camera phone image of probe station measurement.

We took CV measurements of the same sample before releasing and after releasing and the results are summarized in Figure 36. Our releasing yield is 14/16, meaning only 2 capacitors were measured as shorts-circuited elements. We expect a linear slope with the area of the capacitor, which we observe in Figure 36 (A). After the release, we also observe a general linear trend except with larger variation. We note that the variation can be caused due to extra strain of the top plate when the release occurs, pulling the top layer down and compressing the posts. We verified this effect using confocal microscopy.

The slope of the unreleased and released capacitors to be 150 pF/mm^2 and 98 pF/mm^2, respectively - these slopes will help us select design values for our capacitors apriori so that we can engineer our devices to our specifications. To verify that the capacitors were released, on a random released capacitor, we increased the voltage so high that we shorted it. Indicating that the top and bottom plates touched due to the electrostatic force between them.

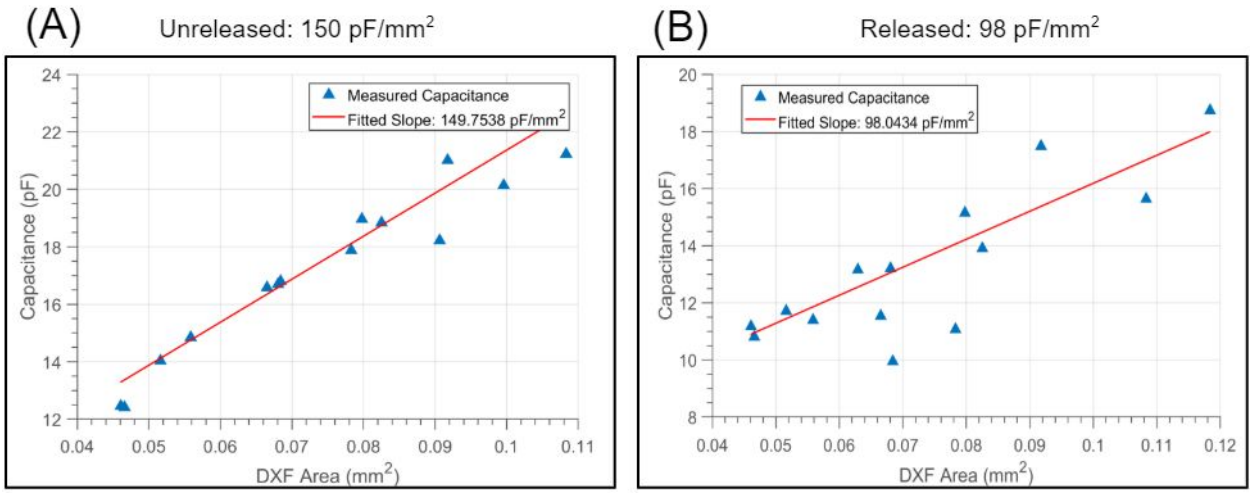

Figure 36. (A) Capacitance vs. Area measurement results of unreleased capacitors. (B) Capacitance vs. Area measurement results of released capacitors.

We also compared the capacitance values to our simple theoretical model for the capacitor. These comparisons are presented in Figure 37. Note the blue line is a reference line with slope

equal to 1, to serve as a guide. We find that when the capacitors are unreleased, our simple parallel-plate model works well. Most of the points are along the reference line, which is to say that it matches theory quite well. To generate Figure 37, we can fit the dielectric constant of the Silicon Dioxide that we deposited from ccp-dep using the data from Figure 36. It is a one-parameter fit because we can use measured values for the distance between the plates. We find that the dielectric constant is $\mathbf{k_{SiO2} = 5.6}$. Figure 37 (B) indicates our simplified model doesn't quite hold since the measured capacitance is much higher than expected. To calculate the theoretical capacitances we measured the distance between the plates (130 nm) and assumed a unity dielectric constant. We suspect the higher-than-expected measured capacitance is due to fringing electric fields from the posts (since there are many of them) adding to the total capacitance. Another reason could be that we haven't completely released the capacitors, but we have tested via high-voltage shorting and SEMs that we have released these structures. In conclusion, we need to update our capacitor model to account for all of the capacitances, which is left for future work.

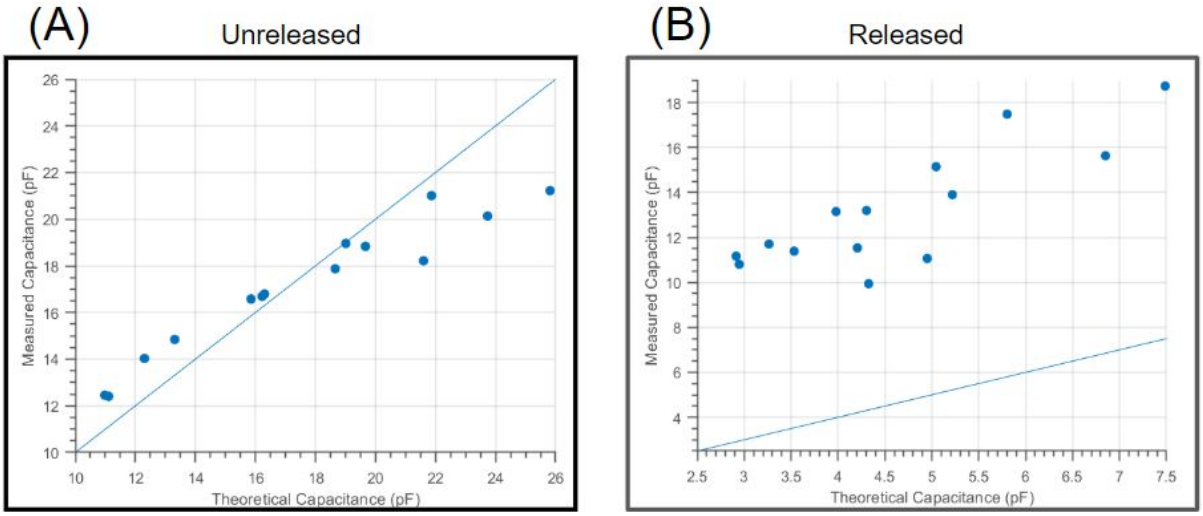

Figure 37. A) Measured capacitance vs theoretical capacitance for unreleased capacitors. The line is a reference line with slope 1. (B) Measured capacitance vs theoretical capacitance for released structures. The blue line is a reference line with slope 1.

Spiral Inductors

Theory

Inductance (or geometric inductance) is a measure of the distribution of the magnetic field near and inside a current carrying conductor. It is a property of the physical layout of the conductor and is a measure of the ability of the conductor to link magnetic flux, or store magnetic energy. In microwave circuits, one of the methods to realize inductive elements is by using planar spiral inductors (see Figure 38a). Although square and rectangular spirals are popular in the literature, this doesn't limit the structure to having four sides. Research has shown that polygons with more than four sides (hexagons,octagons - see Figure 38b,c) or circular spirals (see Figure 38d) improve performance.

The inductance of a polygon spiral inductor can be completely specified by the number of turns n, wire-width w, inductor spacing s and any one of the diameters (d_{in} or d_{out}). Using modified Wheeler's formula, we can get the inductance of the various spirals as[17]:

$$L_{spiral} = K_1 \mu_0 \frac{n^2 d_{avg}}{1+K_2 \rho}$$

where, K_1, K_2 are dependent on the geometry of the spiral (shown in table below), $d_{avg} = (d_{in} + d_{out})/2$ is the average diameter and $\rho = (d_{out} - d_{in})/(d_{out} + d_{in})$ defines a fill factor.

Layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

Table 2. Proportionality factors for the spiral inductance of various geometries.

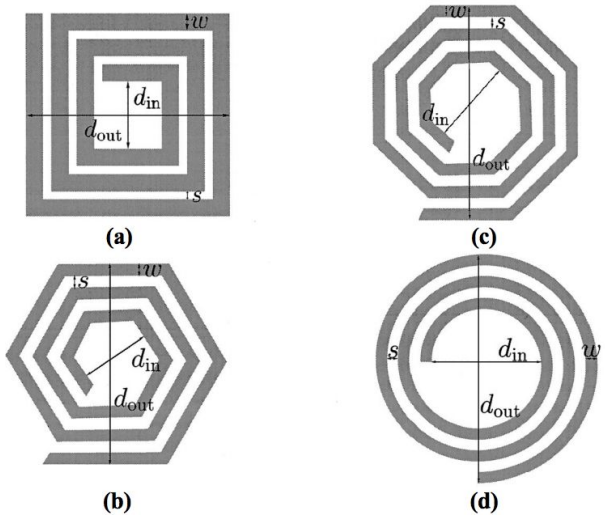

Figure 38. Typical polygon spiral inductors: (a) Square; (b) Hexagonal; (c) Octagonal; (d) Circular

Mask Design

Similar to the parallel plate capacitor, a planar spiral inductor is also 3 mask design. This is more subtle and arises from the fact to establish electrical contact to the center of the spiral. Hence, we need to make jumps in the wires out of the plane to prevent shorting of wires. Figure 39 shows an example mask design for a spiral inductor. We preferred short jumps in wires because these will be more robust to intrinsic stress gradients after releasing the sacrificial layer. Figure 39a shows a spiral inductor with niobium with a contact arm to the center of the spiral, Figure 39b shows pattern in the oxide layer and finally Figure 39c shows the mask in layer 3 (again niobium).

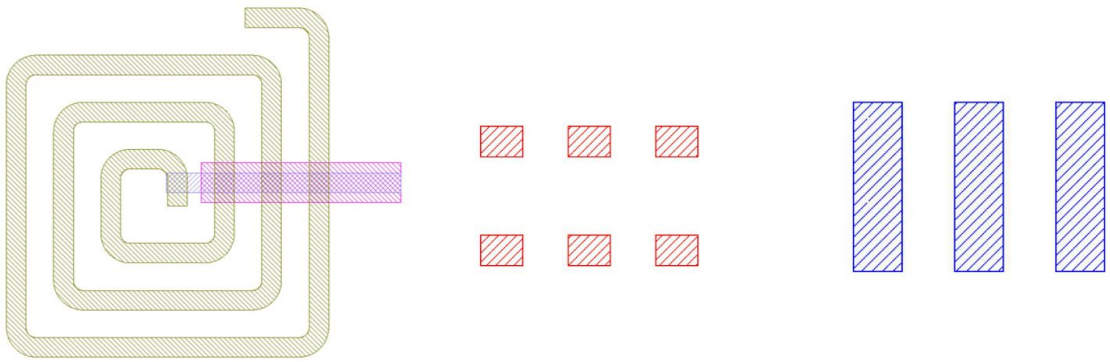

Figure 39. Mask design for a spiral inductor NBSNAKE01 (a) Bottom Nb plate mask; (b) Sacrificial layer mask; (c) Top Nb mask (not to scale)

Let us discuss briefly about the patterns for various masks shown in Figure 39. To clarify nomenclature, “add” a pattern suggests the area where the photoresist is not developed and saved from getting etched, whereas “remove” signifies the opposite. The white background suggests the design ground planes for the respective layers. With that being discussed, we can dive into the mask designs.

In mask 1, we add the pale green spiral, remove the slightly smaller magenta rectangle (to prevent shorting of wires in the bottom layer) and finally add the longer blue one (to create a contact arm connecting to the center of the spiral). In mask 2, we cut the red pattern out of a ground plane (which helps us to create holes in the oxide layer to create contact with the top layer). Finally, in mask 3 we add the blue rectangular patterns (acting as top wires to create out-of-plane jumps in the spiral inductor, after removing the sacrificial oxide layer.

Fabrication

The fabrication of a spiral inductor is exactly similar to the parallel-plate capacitor, which can be found here. Figure 40a,b shows optical microscope images of the first generation unreleased spiral inductors after mask 1. The dark gray/black background in this figure indicates substrate (sapphire) whereas white indicates Niobium. As we can see, post solvent clean of the sample leaves behind contamination from the metal plasma etching tool (PT-MET) which can be removed using the prescribed HF clean recipe. Figure 41a shows image after solvent clean for mask 2 where the color of the holes are distinctly different from the background. Finally, figure 41b shows the dark-field optical microscope image post solvent clean for mask 3.

Future work

The intention of these first generation devices was to test the release procedure developed here and find the base parameters essential structural integrity of the spirals (like jump length and wire width). In the future, we would like to finish the complete electrical characterization of more polygon spiral inductors like hexagonal and octagonal devices, in addition to square spirals (both in simulation and in experiment). FInally, we can integrate it with parallel-plate capacitors to create resonators and perform cryogenic characterization (like Q-factor).

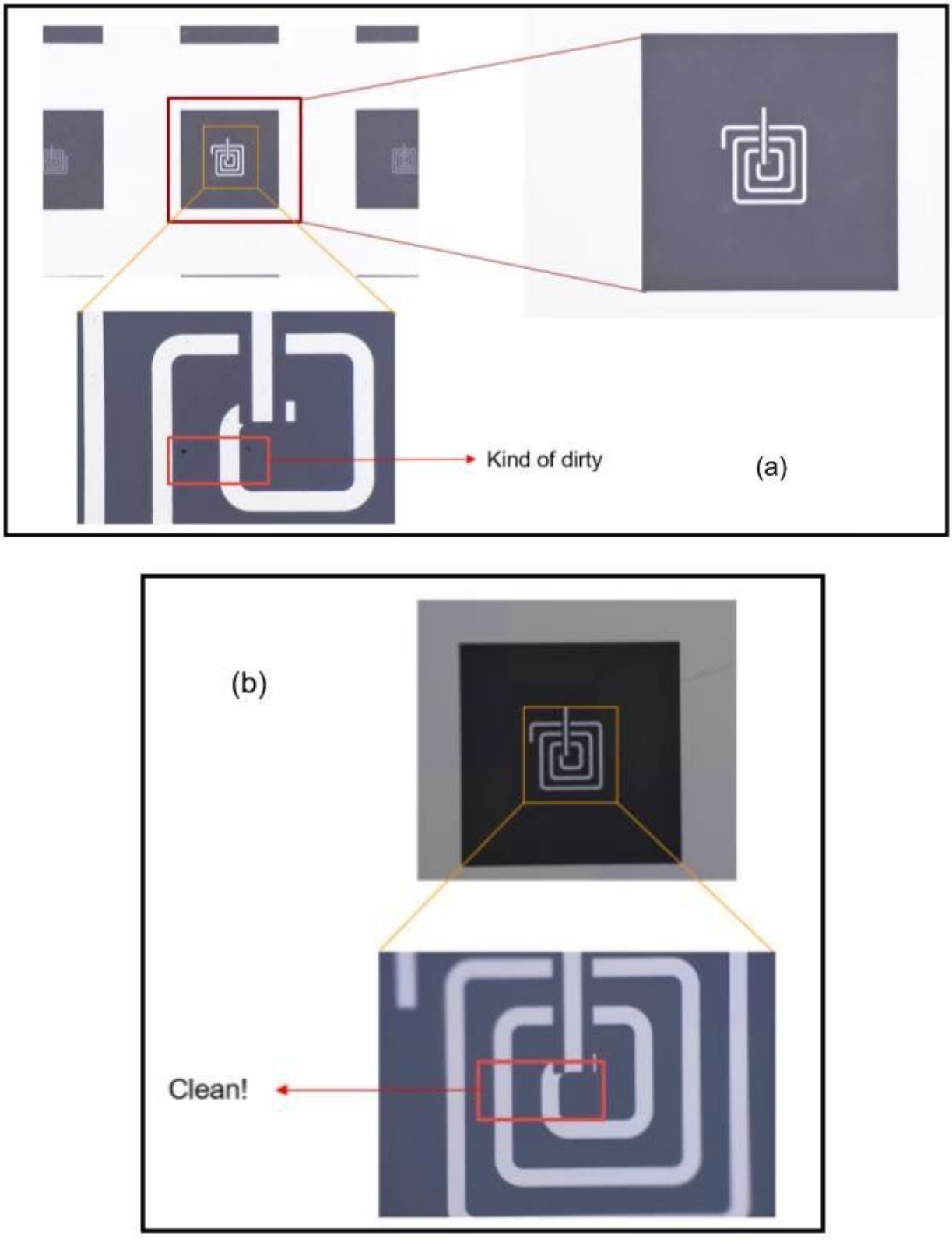

Figure 40. Spiral Inductor NBSNAKE01 fabrication (a) Bottom Nb layer post solvent clean; (b) Bottom Nb layer post HF clean

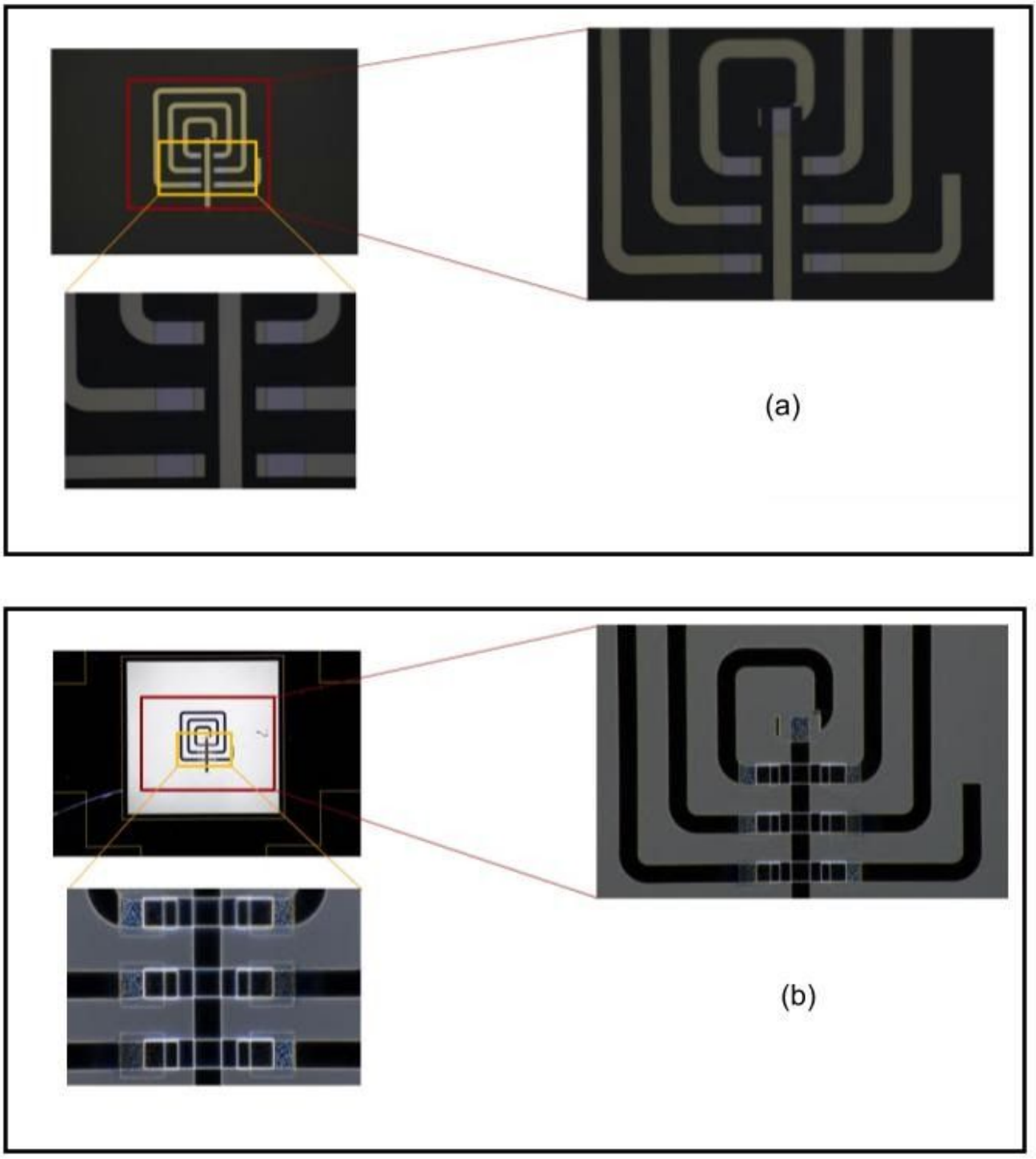

Figure 41. Spiral Inductor NBSNAKE01 fabrication (a) Sacrificial oxide layer post solvent clean; (b) Top Nb layer post solvent clean (dark field image)

Summary

In summary, we produced a detailed process in order to fabricate vacuum gap parallel-plate capacitors using a Niobium-Sapphire material stack. We were able to deposit Niobium to fill the posts so the top-plate of the capacitor is supported after the SiO_2 is released. Using the Plassys e-beam evaporator, we deposited the top-plate of Niobium at a 30 degree angle with respect to the normal of the sample, while rotating the platten at 5 rpm. This procedure yielded aspect ratios from 10-30. This procedure is valuable to the SNF community as it provides a template to galvanically connect two Niobium planes (for example).

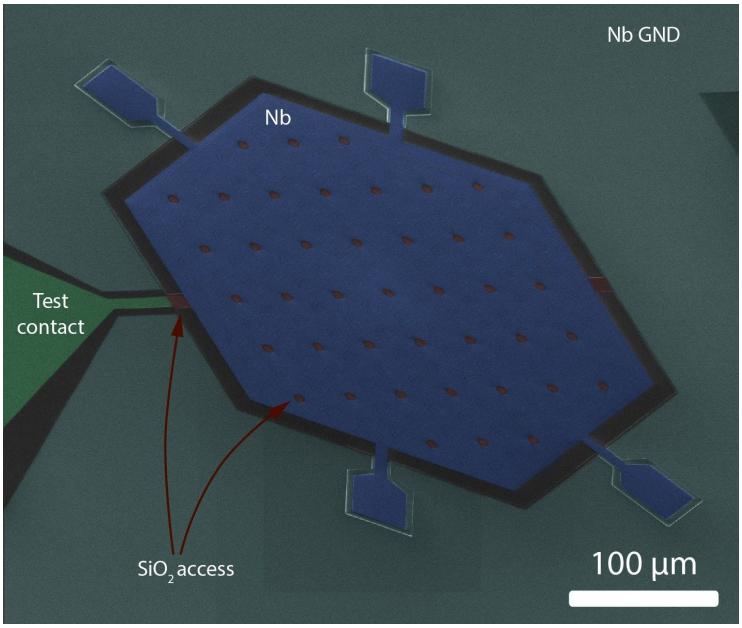

Figure 42. False-coloured SEM micrograph of our parallel-plate capacitor after release. The blue area designates the top electrode of the capacitor. The green area designates the bottom electrode of the capacitor. The black area designates the Sapphire substrate and the grey area designates the ground plane.

Most of our time this quarter was spent determining a post-etch cleaning procedure, and the release procedure of the capacitor. The key to both of these processes was Hydrofluoric Acid. HF (10:1, water:HF) was very effective to remove the thin-redeposited film after the PT-Met etch of the first mask, leaving larger clumps of debris. This debris was removed by an Ozone descum. After this procedure we find a clean substrate and smooth sidewalls. To release the capacitor, we tried vapour-HF at first. However, we observed issues with this approach and switched to wet-HF. We used the same 10:1 (water:HF) mixture as the clean procedure for the release, which was successful. With characterization of the capacitors pre- and post-release, we verified that the release yield was acceptable. Figure 42 shows an SEM micrograph of the parallel plate capacitor. Along with these procedures, an improved Critical Point Drying SOP was developed for small pieces, available to the SNF community. We came a long way from the start of this course to the end and we are looking forward to utilizing this procedure to fabricate interesting superconducting devices in the future.

Runsheet

Process	Step	Substep	Parameters	Tool
Sapphire dicing (optional)	Dice	Wafer/chip clean	Standard ACT + IPA.	Solvent Bench
		HMDS prime	Standard	YES oven
		Spin coat dicing resist	**SPR220-3 on Laurell: 2000 rpm, 40s. 5s 500 rpm spread step. (normally recipe S). 2 min @ 115 C bake**	Headway 2
		Dice	Diamond blade (VT07-SD400-VC100-*), recipe: stoko_5x10, 0.5 mm/s, 20k rpm, low cutting water (0.3)	DISCO

Table 3. Pre-process sapphire dicing runsheet.

Process	Step	Substep	Parameters	Tool
Niobium Evaporation M1	Clean	Wafer/chip clean	Standard ACT + IPA.	Solvent Bench
	Bake	Wafer bake	Bake the wafer/chip, 180C, 20 min	E-beam evaporator
	Evap	Loading wafer/chip	Load the sample on the evaporator stage, 1 clamp for chip, 3 for 2" wafer, blow the sample before loading in	
		Pumping down	Load the stage with sample into LL, pump overnight (12h)	
		Evap	Evap - set target thickness to 1.1*(target)/cos(theta), where theta is the tilt angle	

Table 4. Mask 1 niobium evaporation runsheet.

Process	Step	Substep	Parameters	Tool
Nb patterning M1	Photolitho	Dehydration baking	Dehydrate bake 5 mins at 180C	Hotplate
		Spin coat	SPR3612 1.0 um; 40 s at 5500 rpm	Headway
		Pre bake	Bake 1 min at 90C	Hotplate
		Exposure	Dose 100, defoc 0	Heidelberg 2
		Development	50s MF26A, 20 s DI spray, 20 s DI water rinse, N2 blowdry	wbmiscres
		Pattern verification	Observe the developed pattern under the optical microscope	Optical microscope
		Hardbake	3 min at 115C	Hotplate
	Etching Nb	Chamber cleaning	Load carrier wafer, run clean sequence *Cham_Cln_Def_Cl2_SF6_O2*	Solvent bench
		Chamber conditioning	Run the target recipe for 5 minutes with the dummy wafer inside	PT-MTL
		Mounting on carrier	Small drop of the diffusion pump oil on the back of the chip, place on the wafer and spread the oil, gently moving the chip in x, y.	
		Etching	CF4/O2 70/2sccm 50W 50mTorr, 20C	
	Sample clean	Oxygen plasma clean	Indirect (bottom plate) ashing with 100W, 10 sccm O2 flow, 120 s	Asher
		Step measurement	Range: 6.5 micrometers, length: 800, duration: 10s, stylus force: 2 mg	Dektak
		Stripping resist	Spray acetone + IPA, 30 s each; fill a short beaker with fresh acetone and put chips in, ultrasonic bath for 5 minutes, level ~2; N2 blowdry	Solvent bench
		Acid clean	10:1 HF at room temperature, 100 ml DI + 10 ml HF, add acid to the water beaker. Mount the sample on a teflon holder, rinse for 3 min in HF, 2-stage water rinse, 30 sec each. Flow fresh water over the sample when done, blow dry after removing from the holder.	Acid bench
		Ozone clean	0.75 L/min, 60C, UV on Ozone on, 20 min	Semco ozone cleaner
		Step measurement	Range: 6.5 micrometers, length: 800, duration: 10s, stylus force: 5 mg	Dektak
		Microscope Pictures	Take microscope pictures	Optical microscope

Table 5. Niobium patterning runsheet for mask 1.

Process	Step	Substep	Parameters	Tool
SiO2 deposition M2	Chip preparation	Chip clean	Spray Acetone + IPA, 30 s + 30 s. N2 blow dry; do this for the target chip and a summy Si piece	Solvent bench
	Oxide deposition	Chamber cleaning	Unload any dummy wafers, procedure CLN350, 30 min (should be as long as the last deposition step)	ccp-dep
		Chamber conditioning	Load 4 carrier wafers, run the target recipe (SiO350_0) for 10 min	
		Sample loading	Place the chip on the top of the bottom-left wafer, close to the center of the stage, put a calibration Si chip on the top-left wafer	
		SiOx deposition	SiO350_0, deposition rate 72.59 nm/min	
		Chamber cleaning	Unload dummy wafers, procedure CLN350, 30 min (should be as long as the last deposition step)	
	Thickness verification	Thickness measurement	[65,70,75] deg, 40 rev/meas, high-accuracy	Woolam or Nanospec

Table 6. Silicon dioxide deposition runsheet.

Process	Step	Substep	Parameters	Tool
SiO2 patterining M2	Photolitho	HMDS prime/Bake	Standard HMDS for wafers/Dehydrate bake 5 mins at 180C for chips	YES oven
		Spin coat	SPR3612 1.0 um; 40 s at 5500 rpm	Headway2
		Pre bake	Bake 1 min at 90C	Hotplate
		Exposure	Aligned write, Dose 100, defoc 0	Heidelberg 2
		Development	50s MF26A, 20s DI spray + 20 s rinse. Develop wafers upside-down to avoid resist redeposition.	wbmiscres
		Pattern verification	Observe the developed pattern under the optical microscope	Optical microscope
		Hardbake	3 min at 115C	Hotplate
		Cleaving	cleave Si into pieces (if applicable)	Cleaving station
	Etching SiO2	Chamber cleaning	Load dummy wafer, run oxygen plasma sequence ~20 min *Recipe: O2 Clean1*	PT-Ox
		Chamber conditioning	Run the target recipe for 5 minutes with the carrier wafer inside	
		Mounting on carrier	Small drop of the diffusion pump oil on the back of the chip, place on the wafer and spread the oil, gently moving the chip in x, y.	
		Etching	CF4 10 sccm, CHF3 40 sccm mix, total 50 sccm, 20 mT, 150 W bias	
	Sample clean	Step measurement	Range: 6.5 micrometers, length: 800, duration: 10s, stylus force: 2 mg	Dektak
		Oxygen plasma clean	Indirect (bottom plate) ashing with 100W, 10 sccm O2 flow, 120 s	Asher
		Stripping resist	Spray acetone + IPA, 30 s each; fill a short beaker with fresh acetone and put chips in, ultrasonic bath for 5 minutes, level ~2; N2 blowdry	Solvent bench
		Step measurement	Range: 6.5 micrometers, length: 800, duration: 10s, stylus force: 5 mg	Dektak
		Microscope Pictures	Take microscope pictures	Optical microscope

Table 7. Silicon dioxide patterning runsheet for mask 2.

Process	Step	Substep	Parameters	Tool
Niobium Evaporation M3	Bake	Wafer bake	Bake the wafer/chip, 180C, 20 min	E-beam evaporator
	Evap	Loading wafer/chip	Load the sample on the Evaporator stage, 1 clamp for chip, 3 for 2" wafer, blow the sample before loading in	
		Pumping down	Load the stage with sample into LL, pump overnight (12h)	
		Evap	Evap - set target thickness to 1.1*(target)/cos(theta), where theta is the tilt angle	

Table 8. Mask 3 niobium evaporation runsheet.

Process	Step	Substep	Parameters	Tool
Nb patterning M3	Photolitho	Dehydration baking	Dehydrate bake 5 mins at 180C	Hotplate
		Spin coat	SPR3612 1.0 um; 40 s at 5500 rpm	Headway
		Pre bake	Bake 1 min at 90C	Hotplate
		Exposure	Aligned write, Dose 100, defoc 0	Heidelberg 2
		Development	50s MF26A, 20 s DI spray, 20 s DI water rinse, N2 blowdry	wbmiscres
		Pattern verification	Observe the developed pattern under the optical microscope	Optical microscope
		Hardbake	3 min at 115C	Hotplate
	Etching Nb	Chamber cleaning	Load carrier wafer, run clean sequence *Cham_Cln_Def_Cl2_SF6_O2*	Solvent bench
		Chamber conditioning	Run the target recipe for 5 minutes with the dummy wafer inside	PT-MTL
		Mounting on carrier	Small drop of the diffusion pump oil on the back of the chip, place on the wafer and spread the oil, gently moving the chip in x, y.	
		Etching	CF4/O2 70/2sccm 50W 50mTorr, 20C	
	Sample clean	Step measurement	Range: 6.5 micrometers, length: 800, duration: 10s, stylus force: 2 mg	Dektak
		Oxygen plasma clean	Indirect (bottom plate) ashing with 100W, 10 sccm O2 flow, 120 s	Asher
		Stripping resist	Spray acetone + IPA, 30 s each; fill a short beaker with fresh acetone and put chips in, ultrasonic bath for 5 minutes, level ~2; N2 blowdry	Solvent bench
		Step measurement	Range: 6.5 micrometers, length: 800, duration: 10s, stylus force: 5 mg	Dektak
		Microscope Pictures	Take microscope pictures	Optical microscope

Table 9. Niobium patterning runsheet for mask 1.

Process	Step	Substep	Parameters	Tool
Sapphire dicing	Dice	Wafer/chip clean	Standard ACT + IPA.	Solvent Bench
		HMDS prime	Standard	YES oven
		Spin coat dicing resist	**SPR220-3 on Laurell: 2000 rpm, 40s. 5s 500 rpm spread step. (normally recipe S). 2 min @ 115 C bake**	Headway 2
		Dice	Diamond blade (VT07-SD400-VC100-*), 0.5 mm/s, 20k rpm, low cutting water (0.3)	DISCO

Table 10. Post-process sapphire dicing runsheet.

Process	Step	Substep	Parameters	Tool
Releasing	Annealing	Annealing	Put chip in aluminum box, anneal for 30min @300C, ramp 3	General use oven
	Sacrificial layer releasing	Mounting the chip	Mount the sample on a teflon holder for Nb, clamp small chips with one washer. Make sure that you don't clap on any devices	Acid bench
		HF etch	10:1 HF at room temperature, 100 ml DI + 10 ml HF, add acid to the water beaker. No agitation.	
		Water rinse 1	Carefully transfer the holder with chip to water beaker, 2 stage rinse - 30 sec each, gentle agitation. Leave the holder in the second water beaker.	
		Unmounting the chip	Prepare tweezers; take the holder out of the water beaker and unscrew the chip, make sure it doesn't dry.	
		Water rinse 2	Rinse the chip in a fresh water beaker, 30 seconds; transfer to a small water beaker and let it sit there as you clean the bench.	
	Critical Point Drying	Transfer to IPA	Transfer the chip directly from water to a jar with IPA, let it sit in IPA for at least one hour.	Solvent bench
		Critical Point Drying	Set up the cpd, use two largest teflon spacers, 4" basket, a couple of 4" spacers, and 4-piece basket on the top. Use 150ml of IPA. Load the chip to a small basket and cover it with a dummy wafer sitting on the spacers. Time: 10 min.	CPD
		Ozone clean	0.75 L/min, 60C, UV on Ozone on, 20 min	Semco ozone cleaner
		Microscope Pictures	Take microscope pictures	Optical microscope

Table 11. Niobium structures releasing runsheet.

Process	Step	Substep	Parameters	Tool
Packaging	PCB Prep	Prepare PCB	Solder SMP connectors and ACT+IPA sonciate 15/10 mins	N/A
		Chip glue	GE Varnish diluted with ethanol	N/A
		Wirebond	330/270/30/30 (Nb2pcb), 270/300 (pcb2Nb)	Westbond

Table 12. Chip packaging runsheet.

Financial Report

Fall Quarter

	Budget – Fall Quarter 2019				
TOOL TIME	**Tool**	**Training Cost ($)**	**Time (h)**	**Rate ($/h)**	**Subtotal ($)**
	wbexfab_solv	0	2.95	10	29.50
	Heidelberg	480	6.60	35	711.00
	woolam	160	0.42	50	180.83
	ccp-dep	0	0.75	50	37.50
	PT-MTL & PT-Ox	0	22.33	50	1116.67
	uetch	0	0.00	50	0.00
	lesker-sputter	80	51.90	35	1896.50
	disco-wafersaw	0	2.70	35	94.50
	prometrix	0	2.42	50	120.35
	Headway2	0	0.17	50	8.33
	Headway3	0	0.83	10	8.33
	YES Oven	0	2.05	50	102.50
	SNF Safety Tour	120	-	-	120.00
	All-litho	160	-	-	160.00
SUPPLIES	**Name**	**Count**	**Price ($)**		**Subtotal ($)**
	Silicon 4" wafers	12	17		204.00
	Sapphire 4" wafers	1	55		38.00
	Containers and covers	116			116.00
	Nb target	2	320		640.00
	Tweezers	48			48.00
			Fall Total:		**5632.02**

Table 13. Financial report for Fall Quarter.

Winter Quarter

	Budget – Winter Quarter 2020				
TOOL TIME	**Tool**	**Training Cost ($)**	**Time (h)**	**Rate ($/h)**	**Subtotal ($)**
	Heidelberg	0	19.13	35	669.67
	ccp-dep	0	5.60	50	280.00
	PT-MTL & PT-Ox	100	21.63	50	1181.67
	uetch	0	4.30	50	215.00
	disco-wafersaw	160	9.17	35	320.83
	prometrix	0	0.52	50	25.83
	Headway3/wbflexsolv	0	5.88	10	58.83
	Headway 2	0	0.18	50	9.17
	Wbflexcorr	180	0.00	50	0.00
	SEM	63.75	0.00	50	0.00
	micromanipulator6000	0	6.53	5	32.67
	Woolam	0	0.18	50	9.17
	cpd	0	6.67	50	333.33
	YES/YES2 Oven	0	2.72	50	135.83
SUPPLIES	**Name**	**Count**	**Price ($)**		**Subtotal ($)**
	Silicon 4" wafers	5	17		85.00
	Sapphire 2" wafers	4	38		152.00
	Other		338		338.00
			Winter Total:		**4350.75**
			Total Project Budget:		**9982.77**

Table 14. Financial report for Winter Quarter and Total project summary.

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We would like to thank our amazing mentors - Usha Raghuram, Swaroop Kommera, Mark Zdeblick, and Don Gardner, we appreciate your guidance throughout this quarter and readiness to help. We would also like to acknowledge all of the SNF staff, external mentors and the ENGR 241 course staff - Prof. Jonathan Fan, Prof. R. Howe and the Teaching Assistant - Dr. C. Chia and Xiyuan Chen. Authors would like to thank Prof. Amir Safavi-Naeini and Prof. Emilio Nanni for their ideas and help in planning the project. We also appreciate all of the valuable comments that we received from the members of the Laboratory of Integrated Nano-Quantum Systems (LINQS).

Authors Contributions

All authors were fabricating the wafer-scale and chip-scale 3 mask and 2 mask devices later used in developing the acid clean procedure and release of the sacrificial oxide layer. D.D. finished the fabrication run for the first set of spiral inductors (still unreleased) while working on the electrical simulations of CPWs and spiral inductors in SONNET.

H.S. focused on exploration of various chemicals in the post metal-etch cleaning procedure, developed the HF and UV Ozone clean procedure, Nb annealing, liquid HF releasing process, and critical point drying of capacitors. H.S. prepared CAD files for capacitor and non-planar resonators tests.

K.M. developed the Niobium deposition procedure, explored releasing structures via Vapour HF, fabricated and characterized the planar resonators, designed and characterized the non-planar capacitors, and designed non-planar resonators.

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