Low Temperature Bonding for Neural Implant Fabrication

Project Report for E241—Advanced Micro and Nano Fabrication Laboratory

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1. MOTIVATION

Neural interfacing devices that can be directly implanted into live brains have been important tools for both understanding and modulating neural circuits [1]. These devices have promising potential for the development of therapeutic devices to treat neurological disorders such as Parkinson's disease and obsessive-compulsive disorder, as well as to restore motor control among patients suffering from spinal cord injuries [2]. Recent work by Mina Hanna in the Melosh group at Stanford has shown that neural implants with unprecedentedly-high channel counts can be created by connecting massively-parallel microwire bundles to CMOS arrays [3]. To enable high-quality signal recording from these assemblies, mechanically stable Ohmic contacts need to be created between individual microwires and the CMOS array. Previous methods of establishing such contacts involved applications of compressive forces to press the microwire bundles against the CMOS array. However, maintaining constant and spatially-uniform forces in the dynamic environments of the brain remains a challenge, whereby even transient buildups of excessive forces present an additional risk of damaging the thin and fragile CMOS arrays. This project therefore aims to develop a method for using solder to create rigid and electrically conductive bonds between thin slices of microwire bundles and CMOS substrates, in order to minimize the required contact forces and ensure the integrity of these assemblies.

Due to the sensitive CMOS electronics involved and biocompatibility requirements, a low-temperature (sub-200 °C), non lead-based solder system is required. In this project, the gold-indium ("Au-In") solder system was selected based on (a) the low melting temperature of In at 156.6 °C; (b) the biocompatibility of Au; (c) the high reflow temperature of the $AuIn_2$ intermetallic at 540.7 °C (Figure 1-1); and (d) the improved material stability of the $AuIn_2$ intermetallic (marked by arrow on Figure 1-1) relative to pure Au or In. To create bonding sites between the microwire bundle and the CMOS array, a periodic array of Au-In solder can be patterned onto the CMOS substrate using lithographic methods (Figure 1.1). With the device geometry differing significantly from that involved in traditional wafer-wafer bonding, this project also investigates the feasibility of extending flip-chip bonding techniques beyond bonding between wafers.

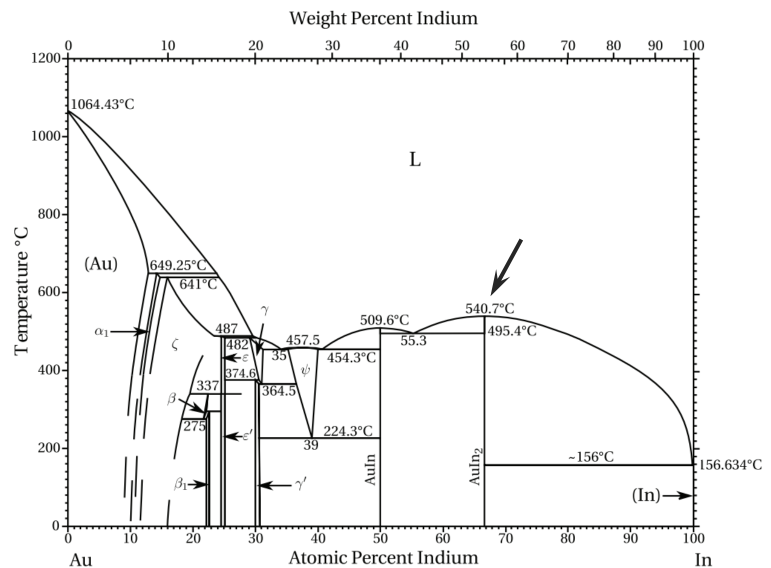


Figure 1.1 Phase diagram of Au-In binary system [4]

2. FLIP-CHIP BONDING CAPABILITIES IN SNF

The flip-chip technique, also termed "Controlled Collapse Chip Connection" (C4), was first developed by IBM in 1964, and has since shown greater reliability and efficiency than traditional manual die and wire bonding. Usually intended for building interconnections between semiconductor chips and substrates, the technique bonds the two objects together by first patterning solder bumps onto the chip, then aligning said bumps to the corresponding metal pads on the substrate, and finally heating the combined assembly to form soldered bonds [5]. In light of the similar interconnections required for the device of interest in this project, the flip-chip technique can in theory be applied to create bonding between microwire bundles and CMOS arrays, with the solder bumps patterned onto the CMOS substrate and then bonded to exposed metal microwire tips at the surface of microwire bundles.

The ExFab within the Stanford Nanofabrication Facility houses a Finetech Lambda Flipchip bonder ("Flipchip bonder"), whose modular design offers great versatility for device prototyping. Its three key components—a heated bottom stage, a heated pivoting upper arm, and a moving optical microscope—provide sub-micron precision for bonding alignment and fine control of bonding parameters via independent modulation of temperature profiles at the bottom stage and upper arm [6]. Alignment is performed using a combination of the optical microscope and a two-way mirror mounted on the tool, which results in a superimposed composite image of the two substrates to be bonded. The substrate mounted on the bottom stage is aligned to that on the upper arm using triaxial micrometer screw knobs. For bonding, the tool interface allows users to graphically customize temperature profiles to obtain desired ramps rates (dT/dt), bonding temperatures (T_{bond}), and bonding times (t_{bond}). Separate profiles can then be applied to the bottom stage and upper arm to meet specific user needs, such as interfacial temperature gradients, temporally-staggered heating steps, and so on.

3. PROJECT STAGES

This project comprised three distinct stages of iterative design and experimentation. First, creating thin and rigid slices of microwire bundles with adequately-exposed individual wire tips required experimentation with epoxy packaging techniques, different machining/polishing procedures to obtain clean and level cross-sectional surfaces on the bundles, and different etching recipes to obtain optimal and uniform etch-back profiles of the glass coatings on individual microwires. Second, designing and fabricating a test chip that would allow for detailed evaluations of mechanical and electrical contact between microwire bundles and individually-patterned solder bumps. Third, exploring the bonding parameter space on the Flipchip bonder to ascertain the viability of good bond formation within the aforementioned thermal and force constraints imposed by our devices of interest.

4. MICROWIRE BUNDLE FABRICATION

Fabrication of the gold microwire bundle followed the recipe developed by Mina Hanna [3], with 15-µm gold microwires (WMT-Wire Machine Technologies, 5-µm gold, 5-µm glass insulation) spooled into 100-mm long bundles measuring 1.5 mm in diameter. We chose a diameter such that there were enough wires for a proof-of-principle on the scalability of the bonding process, while also keeping it at a manageable number to expedite subsequent design/fabrication steps and simplify potential diagnostic and troubleshooting procedures. We then packaged the bundles in shrink wrap and encapsulated them in glass tubes using epoxy (EPO-TEK® 310M)..

Considering the dimensional limitations on substrates to be bonded with the Flipchip bonder as well as those on neural implant devices, we decided to saw the bundles into 2-mm slices. For ease of handling, these slices were mounted onto 5 mm × 8 mm silicon handles. The top surfaces of the bundle slices were further processed in the following steps to ensure good contact between them and the test chips. We first polished the top surfaces of each bundle slice with sand papers of grit sizes

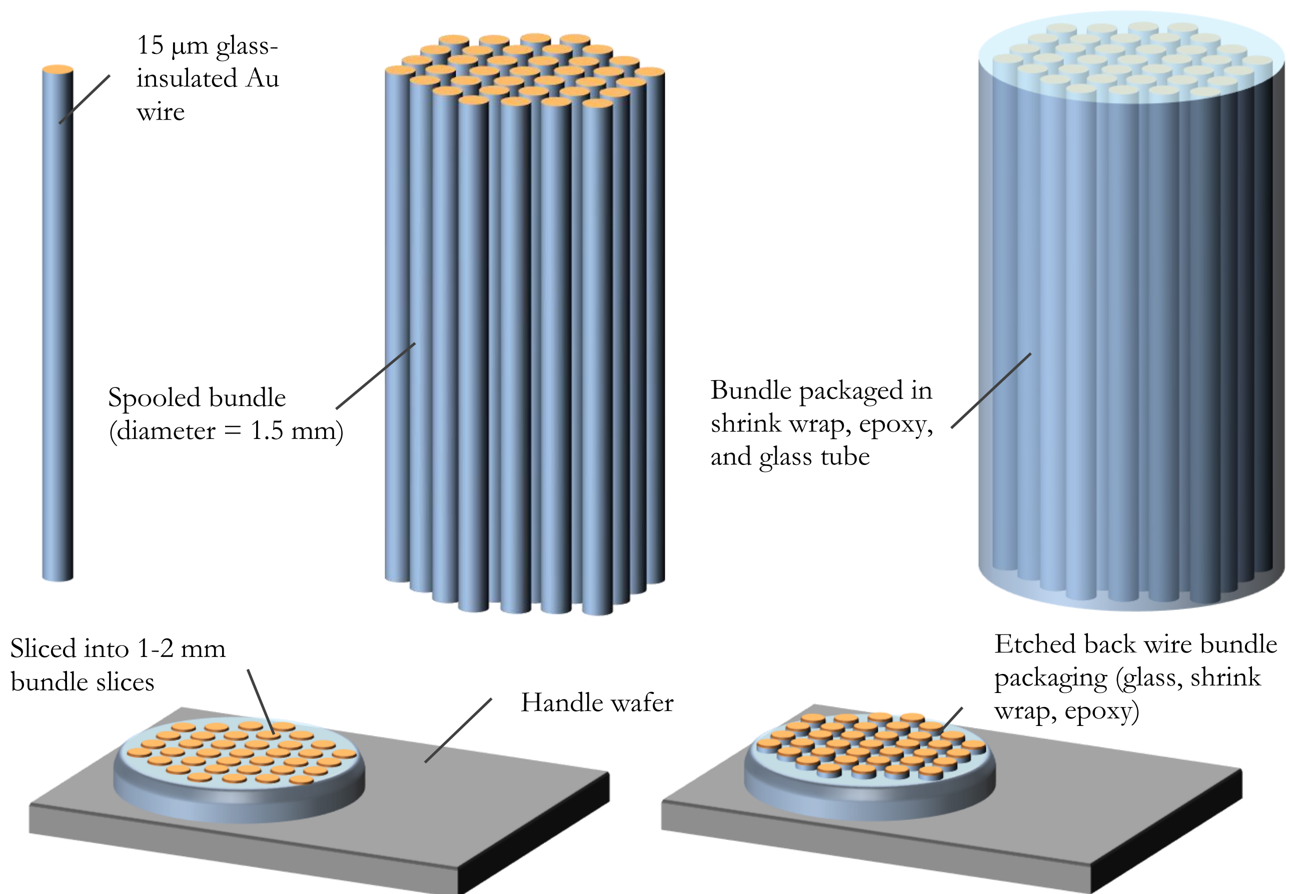


Figure 4.1 Schematics for microwire bundle slice fabrication

P400, P600, P1000, and P1200 successively to obtain uniformly-flat cross sections. To increase the surface area of individual microwires in contact with the solder, we performed an etch-back of both the glass coating and epoxy packaging at the bundle surfaces to expose the tips of individual microwires, using a combined wet-and-dry etch process involving 6:1 Buffered Oxide Etch ("BOE") and O_2 plasma on the Drytek2 Model 100 dry etcher. Figure 4.1 shows the schematics of the fabrication process above.

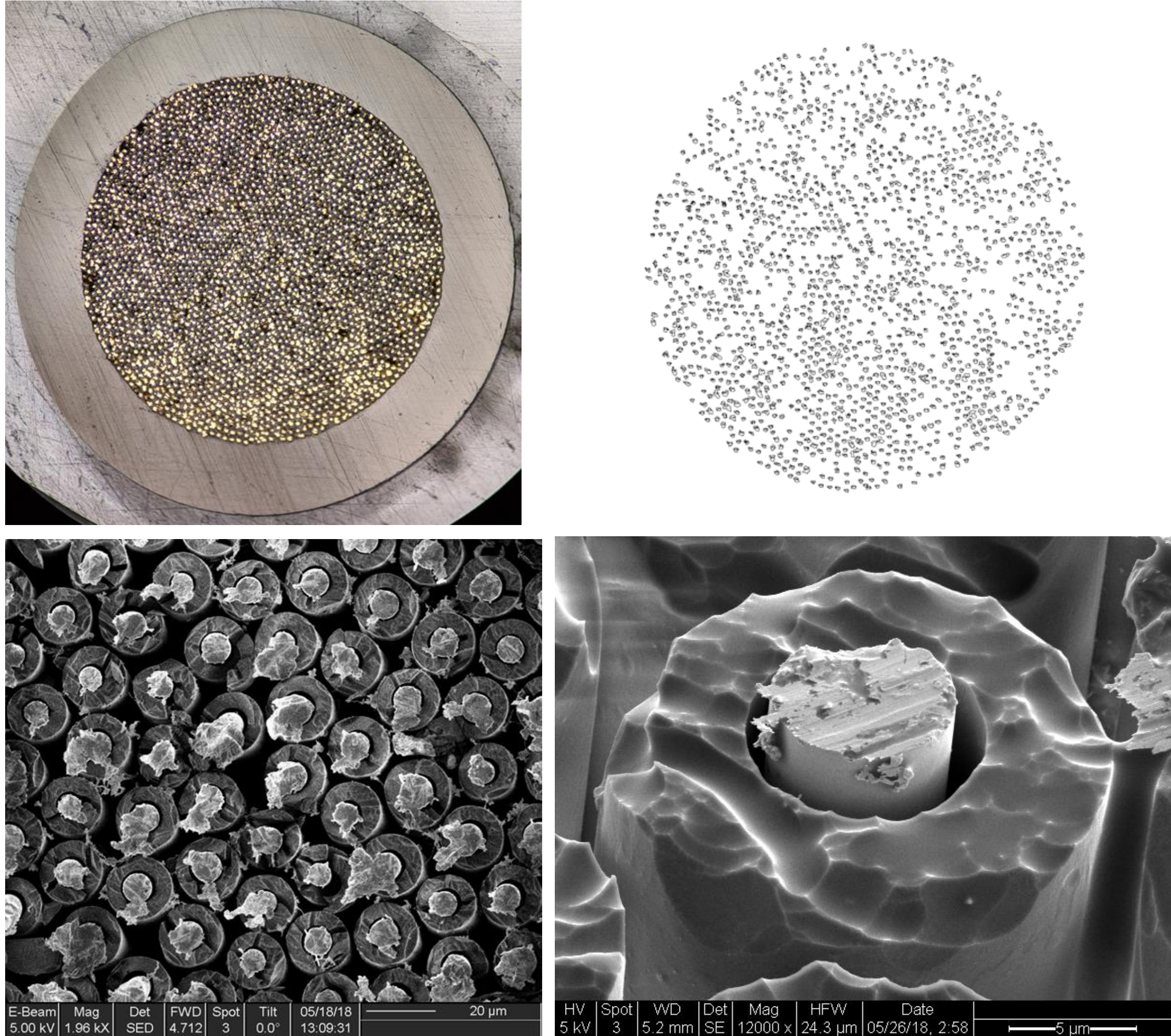


Figure 4.2

Top row: Optical microscope images of a microwire bundle slice (left), and post-processed image (right) used for counting number of wires

Bottom row: SEM images of the etched-back microwires, showing exposed microwire tips (left), and residual marks from mechanical polishing on the microwire tips (right)

Optical microscope images of post-polishing bundle slices revealed that there were ~1500 microwires in a 1.5-mm bundle (Figure 4.2). Closer inspection via scanning electron microscope ("SEM") images showed exposed gold microwires after the etch-back process, with machining marks from the mechanical polishing steps clearly visible on the surfaces of individual microwires. We also observed varying degrees of lateral smearing of gold on some of the microwires, which was likely a product of the sawing and/or polishing steps, as well as the inherent softness of gold. While this smearing was not a significant concern for the purposes of bonding, an additional chemical polishing step with gold etchant can be applied to reduce any smearing if needed.

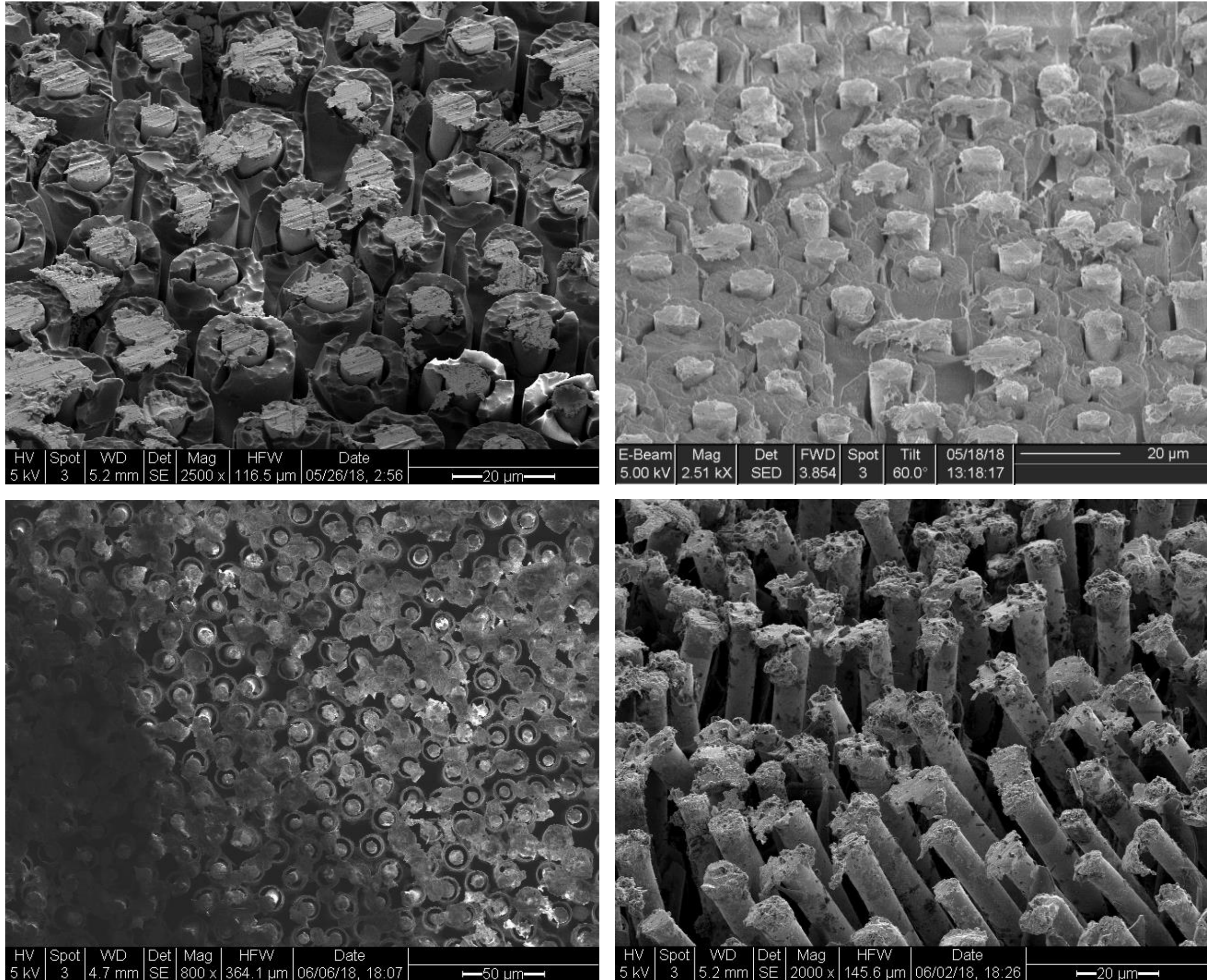


Figure 4.3
SEM images showing variations in etch-back profiles under identical etch parameters, with the glass coating on some slices barely removed (top left), and some completely removed and exposing large lengths of bare Au wires (bottom right)

For the BOE glass etching, however, we observed large variations in etch rates and profiles across different wire bundle slices. Figure 4.3 shows different wire bundle slices that underwent identical etch parameters but yielded significantly-different etch-back profiles. To explain these inconsistencies, we

developed several potential hypotheses. First, the differential etch rates of the glass coating in different directions (e.g. radial vs. longitudinal) may have been due to residual stresses within the coating from the manufacturer's coating procedure. Second, accidental traces of epoxy or other materials left on the bundle surfaces from previous steps may have prevented the etchant from attacking the glass coating uniformly. To ensure more consistent etch rates across different bundle slices and better calibration of the etch-back profiles as a function of etch duration, measures should be taken to ensure tighter quality control of the glass coatings, and the top surfaces should be thoroughly cleaned before etching.

5. TEST CHIP FABRICATION

Given the prohibitive costs of CMOS arrays, we elected to instead employ a surrogate test chip ("TC") to be bonded with the microwire bundle slices for testing the bonding performance both mechanically and electrically. We designed our TC as shown in Figure 5.1 for lithographic fabrication. At the center of each TC, we patterned a 1 mm × 1 mm square array of 20-μm pitched, circular bonding pads ("BP"), each measuring 10 μm in diameter. To evaluate the quality of the bonds formed and identify potential spatial heterogeneities in bond formation across the microwire bundle surface, we selected a radially and angularly-dispersed subset of 64 BPs that were then individually connected via conductive leads ("CL") to larger, more easily-accessible 2 mm × 2 mm measurement pads ("MP")

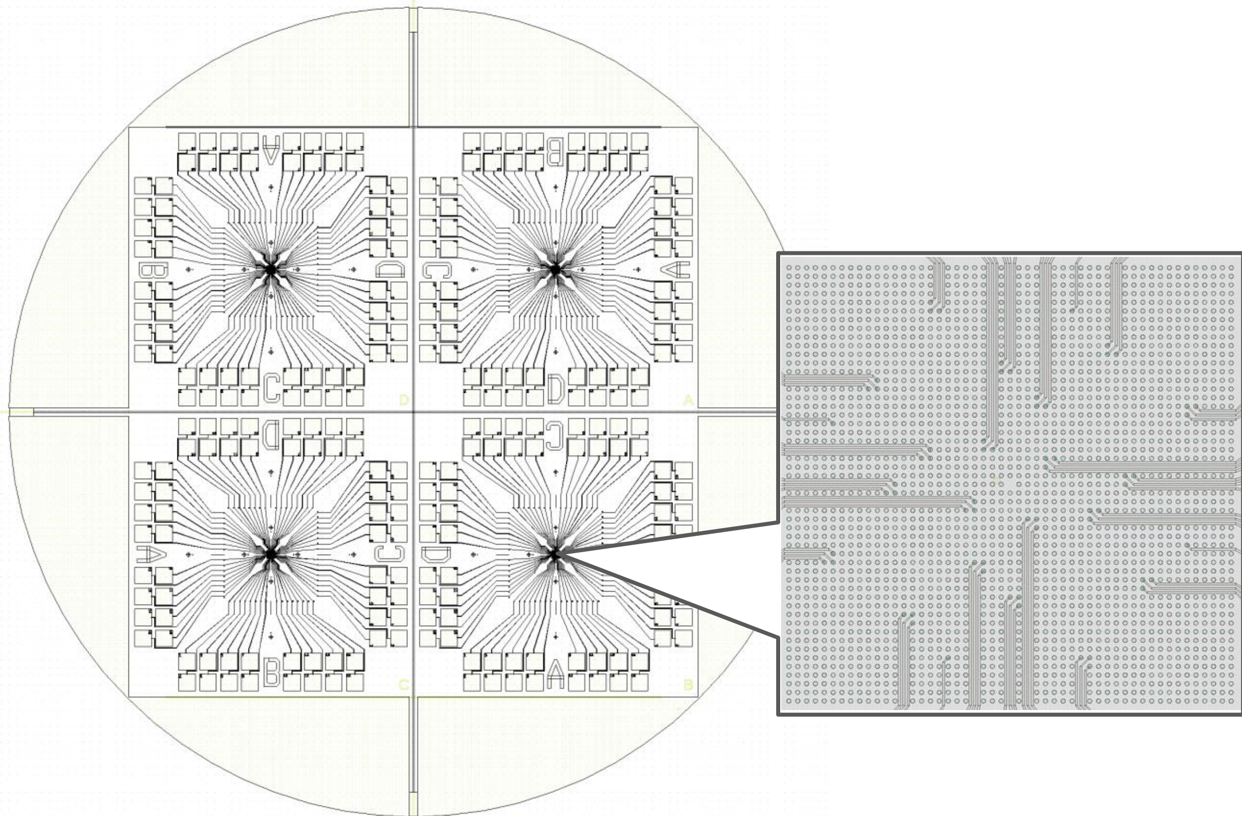


Figure 5.1

Mask pattern for 4 TCs on a single wafer, with inset showing the 1000 BPs at the center, 64 of which individually connected to MPs in clusters of three to enable tests for shorting between adjacent BPs.

on the periphery of the TC. These BPs were also selected in adjacent clusters of three to allow for subsequent assessment of potential shorting between BPs.

Creating the initial electrical circuit on our TCs began with using the Heidelberg MLA150 maskless aligner to pattern 2 by 2 arrays of the design in Figure 5-1 onto bare 4" quartz wafers using a 1.6-μm layer of Shipley 3612 photoresist. After developing the photoresist, we put the wafers through a brief descum run with O_2 plasma in the Drytek2 Model 100 dry etcher to remove any organic residues that would impair metal-wafer adhesion. We then used the Innotec e-gun evaporator to deposit a 10-nm Ti adhesion layer onto the wafers, followed by 50 nm of Pt to create our CLs and BP/MP surfaces. The resulting wafers were then briefly sonicated in an acetone bath and left to soak for an additional 2 hours to complete the first of two photoresist liftoffs. Due to the close proximity (~5 μm) between the longer CLs and neighboring BPs along them, we decided to add a passivation layer to prevent any unwanted electrical contact between them, particularly during the bonding process that was likely to displace flowing solder away from individual BPs. We proceeded to apply a 1-μm layer of SiO_2 to our TCs using the PlasmaTherm CCP plasma-enhanced chemical vapor deposition tool.

Next, we needed to etch away the SiO_2 on our BPs/MPs to re-expose their electrically-conductive Pt surfaces, and to deposit our Au-In solder onto the individual BPs. To minimize the number of lithographic steps required, we decided to use a single photoresist layer to perform both the selective SiO_2 etching and solder patterning. To ensure that a sufficient volume of solder was deposited onto each BP and to maximize the bonded surface area on individual gold microwires, we decided to target a cumulative Au-In solder stack height of 4-7 μm. A 3:1 proportion of In to Au was chosen in order to facilitate formation of the Au-In intermetallic highlighted in the Au-In phase diagram in Figure 1.1. Our first challenge in achieving these tall features was to create high-aspect ratio trenches in a thick 7-10-μm photoresist layer with minimal hanging sidewall profiles, both to facilitate solvent permeation and minimize damage to our features during liftoff. After some experimentation, we decided on a 10-μm layer of Megaposit SPR 220-7, to which we applied an increased 800W power output during Heidelberg exposure and 3 consecutive developing cycles on the SVG Developer. We then performed a 15-minute wet etch with 20:1 BOE, which was sufficient time to not only re-expose the metallic BP/MP surfaces, but also create overhanging SiO_2 sidewall profiles (Figure 5.2) around each BP that were desirable to facilitate solvent permeation for photoresist liftoff, as well as to contain and localize any solder flow during bonding.

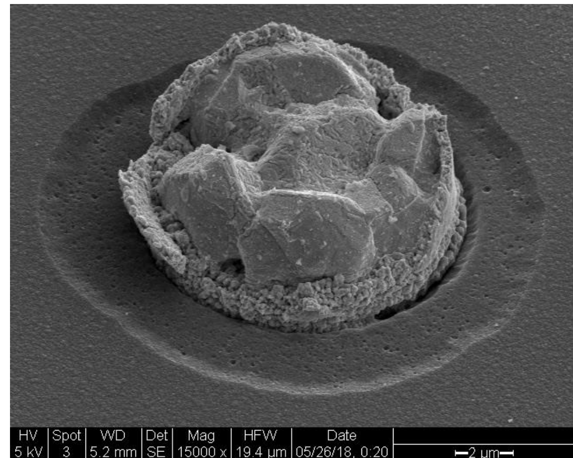


Figure 5.2
SEM image showing the SiO_2 hanging for facilitating liftoff and localizing solder flow

Our second challenge was to develop an alternate means of monitoring deposition thickness for the tall solder stacks we were targeting. Due to the large amounts of Au-In and long deposition times required, the quartz crystal microbalances ("QCM") used in the Innotec e-gun evaporator (and metallization tools in general) to monitor deposition rates and thicknesses would fail prematurely in the middle of our depositions. While we considered the option of replacing the QCM mid-deposition, this required venting the tool's sample chamber and forming unwanted native oxidation layers on our In solder. Hence, to overcome these limitations on QCM lifespans, we reserved our longest deposition from a single source crucible—In—for the last deposition step, and used the steady-state deposition rates prior to QCM failure to extrapolate the total deposition times required to achieve our desired solder stack heights. We were therefore able to deposit within a single pump-down an overall BP stack comprising 10 nm of Ti for Pt-Au adhesion, 1 μm of Au, 5 μm of In, and 500nm of Au as a capping layer to prevent In oxidation. As before, the resulting wafers were then briefly sonicated in an acetone bath and left to soak for an additional 2 hours to complete the second and final photoresist liftoff. The wafers were then diced into individual TCs using the DISCO Wafer Saw. A complete process flow is included in the Appendix at the end of this report.

6. BONDING EXPERIMENTS

We mounted the bundle slice and fabricated test chip onto the bottom stage and upper arm of the Flipchip bonder, respectively. This placement was chosen due to the thickness of the bundle slices that exceeded the maximum thickness of substrates that can be mounted on the upper arm. This also proved to be beneficial due to the larger thermal inertia of the bottom stage and the large amounts of thermally-insulating components (i.e. epoxy, glass) in the bundle slices compared to the test chips. Immediately before each test chip and bundle slice were placed in contact for bonding, we applied a layer of liquid flux (FP-500, Indium Corporation) to the bonding interface in order to dissolve any native indium oxidation layers that may have formed and maximize the flow of metallic indium.

Application of the flux turned out to be a crucial prerequisite to achieving successful bonding. In our initial experiments that we conducted without the use of flux, we observed minimal flowing of the indium solder and thus failed to create any noticeable bonding with the bundle slices. Figure 6.1 compares the morphology of the bonding pads before and after the bonding tests without the use of flux. Minimal changes in the surface textures indicate very limited amounts of indium flow and recrystallization during the bonding test.

The identified key variables affecting the bonding performance were: bonding temperature T_{bond}, bonding time t_{bond}, heating ramp rate dT/dt, and applied bonding force F. Given the limited thermal budget of the devices of interest, we chose a T_{bond} of 170 °C, slightly above the melting temperature of indium. Additionally, since indium oxidizes readily in atmospheric conditions [7], we chose the maximum available ramp rates permitted on the Flipchip bonder in order to limit the amount of time the indium solder was exposed to atmospheric conditions while at elevated temperatures below its melting point. Table 6.1 shows the bonding conditions used for the bonding tests and the corresponding results we obtained.

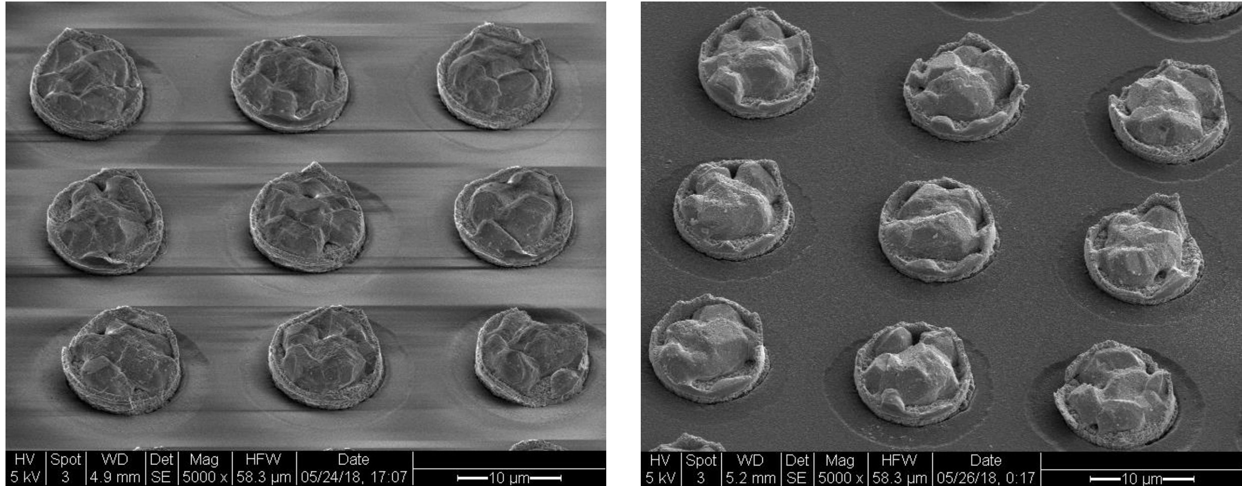


Figure 6.1 Comparison between solder stacks before (left) and after (right) bonding without flux applied

The temperature profiles we used for the bottom stage and upper arm are shown in Figure 6.2. We delayed the heating of the upper arm by 20 seconds in order to compensate for the lower observed thermal conductivity of the bundle slices on the bottom stage, and to minimize any temperature gradients between the microwire tips and solder at the bonding interface.

Table 6.1 Conditions and results for bonding on Flipchip bonder

Indium solder height (μm)	**Ramp rate** dT/dt **(°C /sec)**	**Bonding temperature** T_{bond} **(°C)**	**Bonding time** t_{bond} **(min)**	**Bonding force** F **(N)**	**Results**
5	6 (solder chip) 20 (bundle)	170	3	0	No bonding
			3	10	No bonding
			3	25	No bonding
			3	50	No bonding
			6	25	Weak bonding
			6	50	Strong bonding

TA successfully-bonded bundle slice-test chip assembly is shown in Figure 6.3 (a). The bonding created was mechanically durable, as we were able to ascertain via an improvised "shake test"—the assembly was put inside a plastic box, which was then violently shaken to jolt the assembly inside the

box and apply large impulsive shear stresses to the bonds. Assemblies for which weak or no bonding was achieved fell apart with little effort, while the successfully-bonded assembly survived prolonged shaking with no visible changes. After these mechanical tests, we manually broke the bonded assembly apart to examine the bonding surfaces. Optical microscope images (Figure 6.3 (b-c)) indicated that large amounts of the indium solder were "transferred" to the surface of the bundle slice, which was not observed for assemblies that failed to bond. Further SEM imaging and energy-dispersive X-ray spectroscopic ("EDS") measurements (Figure 6.3 (d-f)) confirmed the transfer of indium solder from the test chip to the bundle slice.

A rudimentary impedance test was also performed on the bonded assembly using an electrochemical potentiostat (EC-Lab) with a two-electrode configuration. We added a droplet of phosphate-buffered saline ("PBS") onto the top surface of the bundle slice, and placed a counter electrode in contact with said droplet. When a testing probe was put in contact with a MP to close the measurement circuit, we obtained measured impedance values of ~10^9 Ohm, which significantly exceeded the 10^4-10^5 Ohm values usually reported for neural implants, thereby indicating poor electrical connection. Further measurements conducted on an unbonded test chip with the PBS droplet directly on the BPs produced similar results. We inferred from these results that the test chips were not ideal for electrical testing, and that further troubleshooting on the design and fabrication of the test chips would be needed for more accurate assessments of the electrical contacts formed by the bonding process.

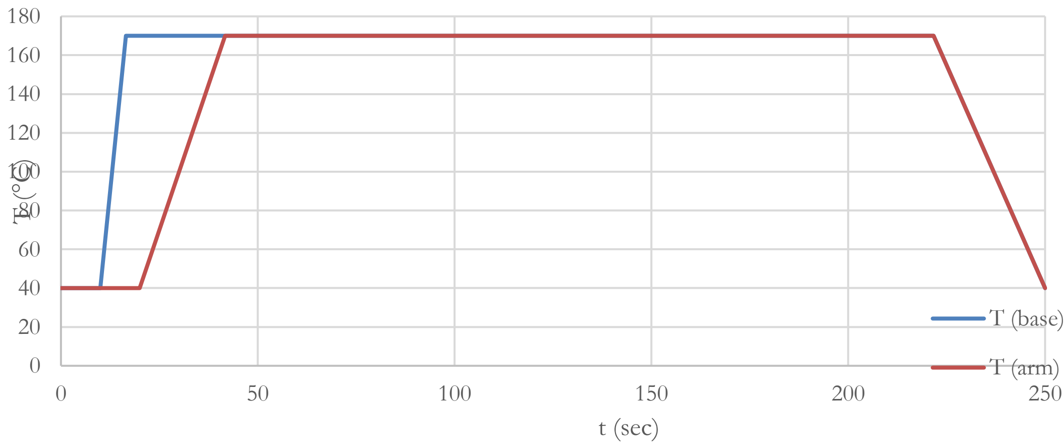


Figure 6.2 Representative temperature profiles for a test with bonding time of 3 minutes

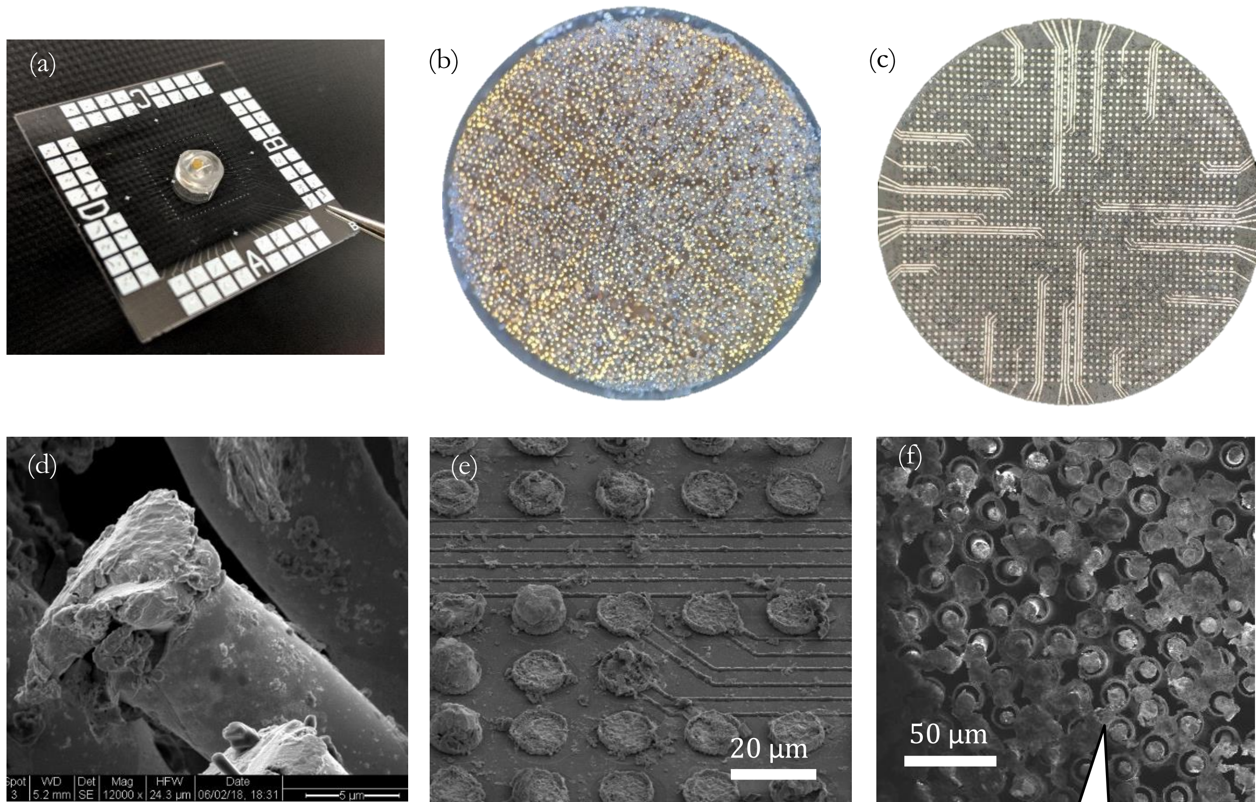
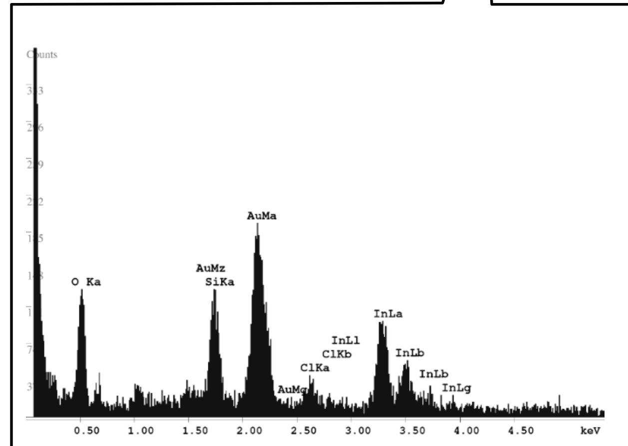


Figure 6-3
(a) A bonded bundle slice-test chip assembly
(b), (c) Microscope image shows indium transferred from TC (c) to wire bundle (b)
(d) SEM image showing indium on top of gold wire
(e) Solder bumps were "missing" from most of the pads on the TC
(f) SEM image showing indium on wire bundle, with inset showing the EDS spectrum obtained from the same region confirming the existence of indium



7. SUMMARY OF FINDINGS AND FUTURE WORK

In this project, we were able to achieve successful mechanical bonding between ~1500-microwire bundle slices and surrogate test chips that approximated CMOS arrays, with a micron-level 2D array of 6.5-µm tall gold-indium solder bumps. The bonding attained was able to withstand large impulsive loads above and beyond those expected for neural implant devices. SEM imaging and EDS analysis

on successfully-bonded assemblies revealed large transfers of solder from the test chips to the gold microwires. Preliminary electrical testing revealed little information on the conductive behavior of the bonds formed, which will be further investigated for future electrical testing and eventual bonding to CMOS arrays.

Given that indium oxidizes readily in atmospheric conditions, we propose several modifications to the Flipchip bonder that would enable further explorations of the low-temperature, low-force parameter space for bonding. First, an ultrasound module can be used to induce local frictional forces at the solder-substrate interface to mechanically break any oxide layers and improve the quality of bonds formed between the solder and microwire tips. Second, a controlled-environment housing can be used to flow inert or forming gases over the substrates during bonding to prevent further oxidation of indium and potentially reduce any oxides back to metallic indium.

Neural implant devices generally require long-term thermal and mechanical stability, as well as low toxicity of any material systems used. Formation of the $AuIn_2$ intermetallic not only stabilizes the bonding by drastically increasing the reflow temperature of the solder to above 400 °C, but potentially also reduces the biotoxicity of indium, as in the case of Ti-In alloys for dental implants [8]. Confirmation and characterization of intermetallic formation can be performed with reflow experiments and transmission electron microscopy analysis on the cross sections of bonded assemblies.

In conclusion, this project provides a proof-of-principle demonstration of extending the applications of flip-chip bonding techniques to unconventional substrates beyond wafer-to-wafer bonding, specifically between microwire bundles and micron-level individual solder bumps. This bonding method enables the selection of microwire materials previously determined to be incompatible due to their inability to withstand large compressive forces. The lower bonding forces involved also decrease the risks of damaging fragile CMOS arrays, which may enable further experiments with ultrathin CMOS arrays for use in flexible neural implants.

8. ACKNOWLEDGEMENTS

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Appendix—Process Flow for Fabricating Testing Chips