Si and Glass Flip Chip Bonding with Solder Paste and Laser Cut Tape Stencils

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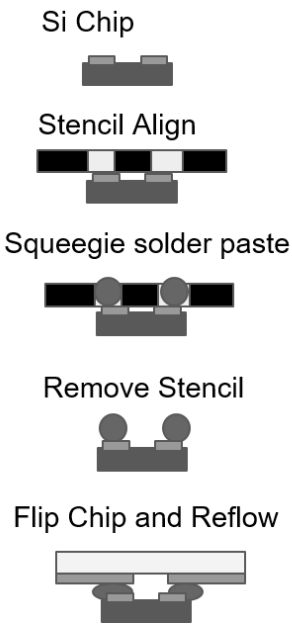
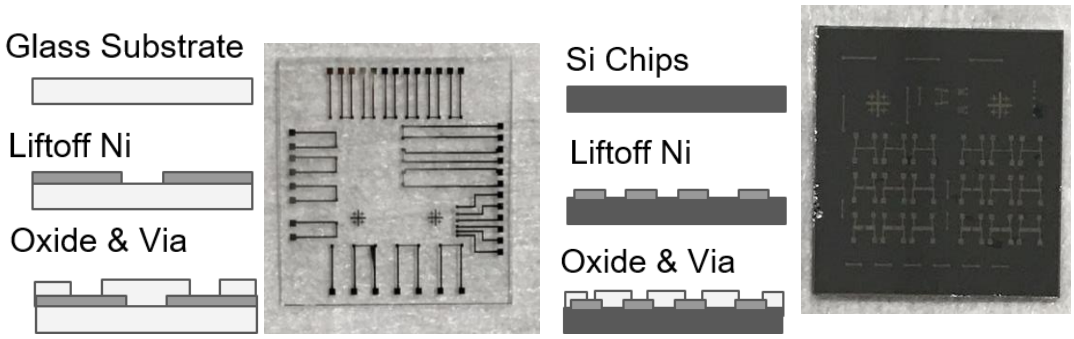
Introduction

The goal of this project was to utilize the new finetech bonder to create a flip chip bonding (FCB) process for Si chips to substrates, using solder connections. This will help the SNF community utilize packaging techniques common in industry at a research level. FCB is beneficial in technology for sensor arrays (e.g. imaging chips and ultrasonic transducers), and allows for more robust packaging than traditional wire bonding. This is important for us because it will enable future packaging of MEMS, microfluidics, and solid state devices developed in our lab groups. While this technology is mature in industry, there is a multitude of methods for doing this and our main goal was to develop a working FCB process by the end of the quarter that SNF users can leverage on the finetech bonder. The process we developed follows the drawing on the right, this procedure involves aligning a stencil (tape laser cut by the epilogue laser), aligning the stencil (via the finetech), applying solder paste via a squeegie, and flipping the chip onto a substrate using the Finetech and reflowing the solder using heat.



Die Fabrication

The device and substrate dies are fabricated in the Stanford Nanofabrication Facility (SNF). Glass and Silicon wafers are cleaned using piranha solution and then the surfaces are roughened in a 50:1 H2O:HF solution for 10 seconds. To prepare for a liftoff process, the wafers are primed using Hexamethyldisilazane (HMDS) before spin coated with 200 nm of LOL 2000 and 1.6 um of SPR 3612. Device patterns are transferred to the photoresist by a 3 second Karl Suss MA-6 exposure of transparencies mounted to blank pyrex masks. After photoresist development, 10 nm of titanium and 150 nm of nickel are evaporated using the Innotec ES26C E-Beam Evaporator. Excess metal is lifted off by soaking the wafers in acetone overnight. Residual photoresist and metal is removed by sonicating the wafers in isopropyl alcohol and Microposit Remover 1165. Finally, the surfaces of the wafers are passivated with 200 nm of SiO2 using the PlasmaTherm Versaline HDPCVD. Lastly, oxide on the contact pads are opened up using the PlasmaTherm Oxide Etcher. The device fabrication is complete, but the wafers must be prepared for wafer dicing before flip chip bonding. To protect the wafer surfaces from particles during the sawing process, coat the wafers with 1 um of SPR 3612. After dicing with the DISCO wafer saw, the photoresist and particles are removed with acetone and isopropyl alcohol soaks and rinses.

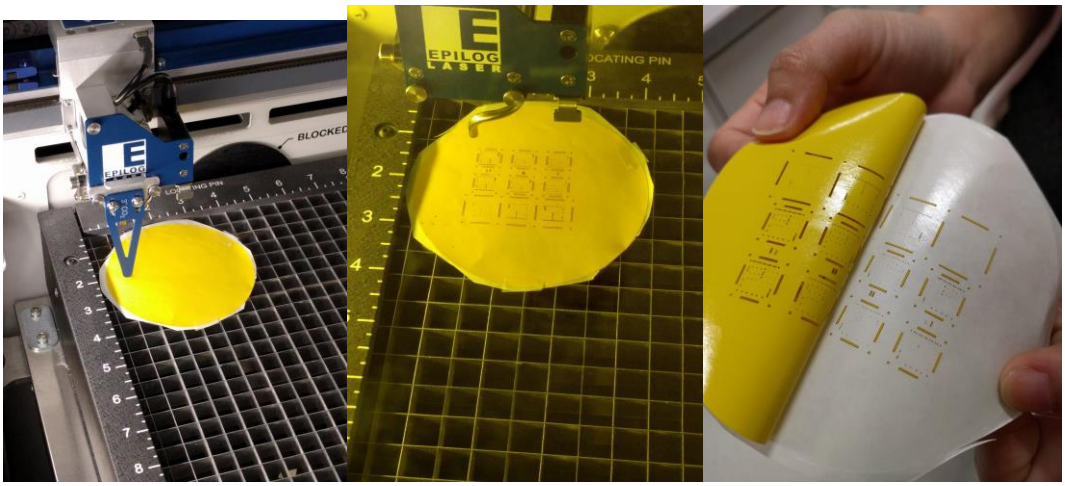


Fabrication schematics and the finished glass and silicon die for bonding experiments.

Laser Cutting Tape

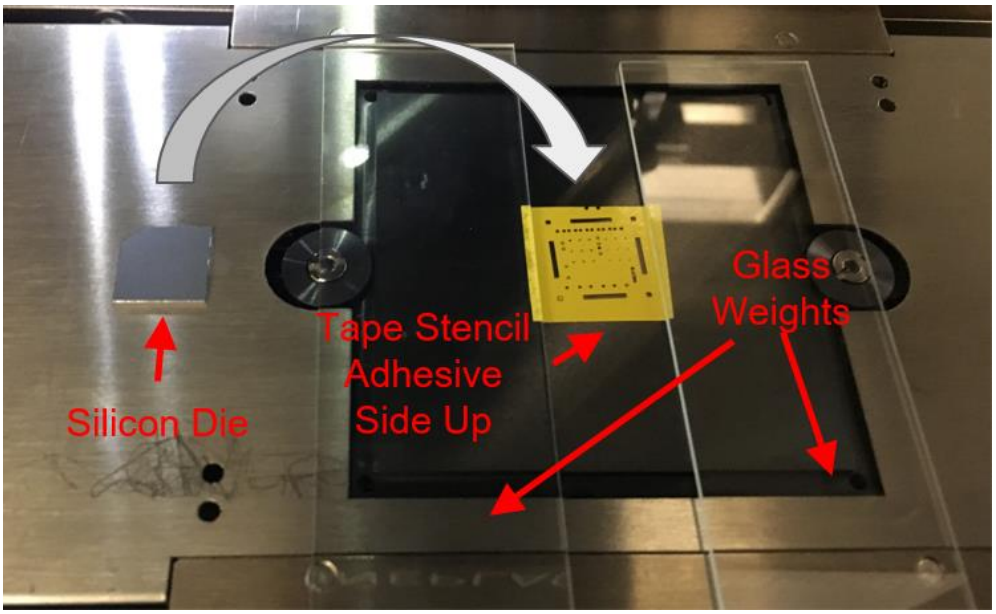
While ideally a metal stencil would be used due to precision-designed things, we developed a quick turnaround process using yellow and blue tape to create stencils for solder paste application. The procedure involves the following

1. Design drawing of cuts (Adobe illustrator, dxf, and pdf are a few of the design types)
2. Import into epilog laser cutting software (XX), keeping track of scaling
3. Define objects as curves, set line width to “hairline”
4. “Print” the design, set cut to vector cut only
5. Mount sample on a flat surface (Silicon wafer or cardboard were used) with tape
6. focus/align laser as normal
7. Cut!
8. Successful tape cuts will have removed or peel-able interiors



After this, we aligned the tape to our samples using the finetech as an aligner. In order to keep the tape flat, we used two glass slides to hold the sample in place. Future designs should

include alignment marks intended for this step - we aligned to rather large bond pad openings.



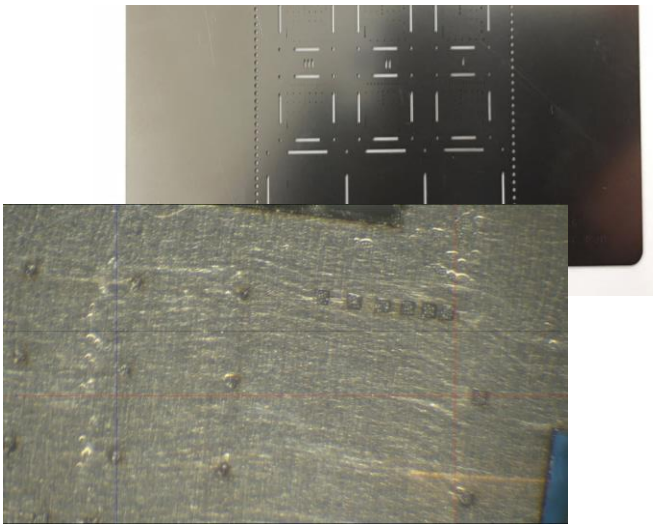
We applied many laser cuts to the tape, and while many values worked well for creating large holes to allow solder through, we chose one sample (J) to proceed forward with:

Label	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S
Speed (%)	7	7	2	3	7	1	4	4	4	1	7	3	4	2	1	7	7	7	4
Power (%)	4	2	1	1	3	1	2	1	1	1	2	1	2	1	1	2	3	4	1
Tape	2 Yellow Dots								Blue Tape			1 Yellow Dot							

Images from some these runs could be included in the appendix? It should be noted that the feature sizes we designed for were smaller than the features that were actually cut - this could be further characterized in a future edition of this course.

Metal Stencils

We had originally designed a metal stencil for use on our die, and we ordered one from pcbunlimited.com, at a thickness of 0.012". We had thought a thick stencil would not warp and thus maintain its flat shape, but this was not the issue..



Left - stencil purchased for project *Right* - close up optical image of solder paste stuck in apertures of our stencil

However, we came across a few challenges with this stencil, summarized below:

1. Alignment of a 2" stencil to a 1 cm die was challenging by hand
2. Keeping the stencil in place during solder paste application was not simple
3. The large stencil vs small feature caused the stencil to not lie flat, but pivot at one edge.
4. Our type 3 solder paste had 20-40 um spheres, and these spheres did not fit through our smallest aperture (50 um x 100 um), and the capillary forces caused the spheres to stick to the side walls of the stencil, instead of the substrate. The spheres could only be removed after an ultrasonic bath.

We compile the following suggestions for future users of metal stencils:

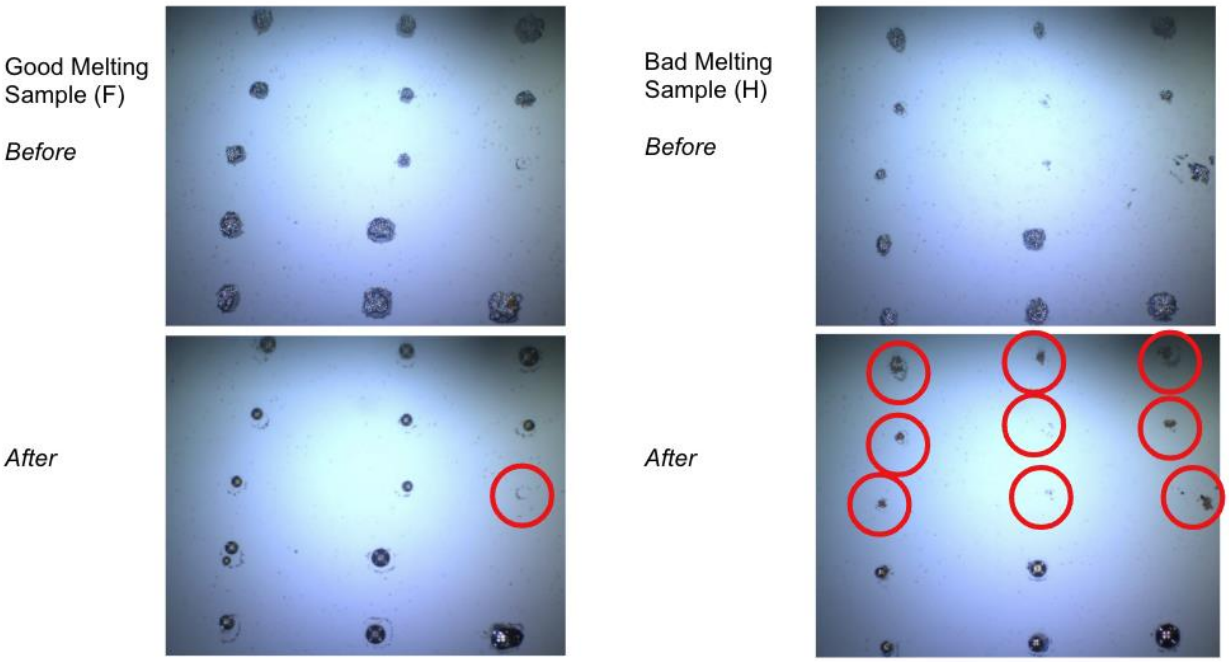
1. Keep stencil flush against surface. A standard stencil/pcb configuration should be used, the stencil area could match the substrate area for paste application
2. Keep stencil thin as possible. This a nice resource that could help (a re-examination shows we should have used 0.001"): http://www.qualiecocircuits.co.nz/stencil-technology-other-aspects.htm
3. Single die stencils are cheaper, and possible future add-on for finetech would be their jig for mounting and aligning small stencils.
4. Stencils should be designed to include viewing windows to help with alignment, and alignment features can be included. Stencils can be machined with engraved alignment marks for mechanical fixtures as well.
5. There are standard powder-size recommendations for solder paste with respect to aperture (See attached PDF)

Open Face Experiments

From the previously mentioned laser cutting experiments, there were many tape stencils available to choose from. To select the best stencil for a specific device, perform open face reflow experiments using blank pieces of the same substrate as your desired final device. The

stencil should at least include the smallest and largest apertures planned to be used in the final device stencil. The process is as follows:

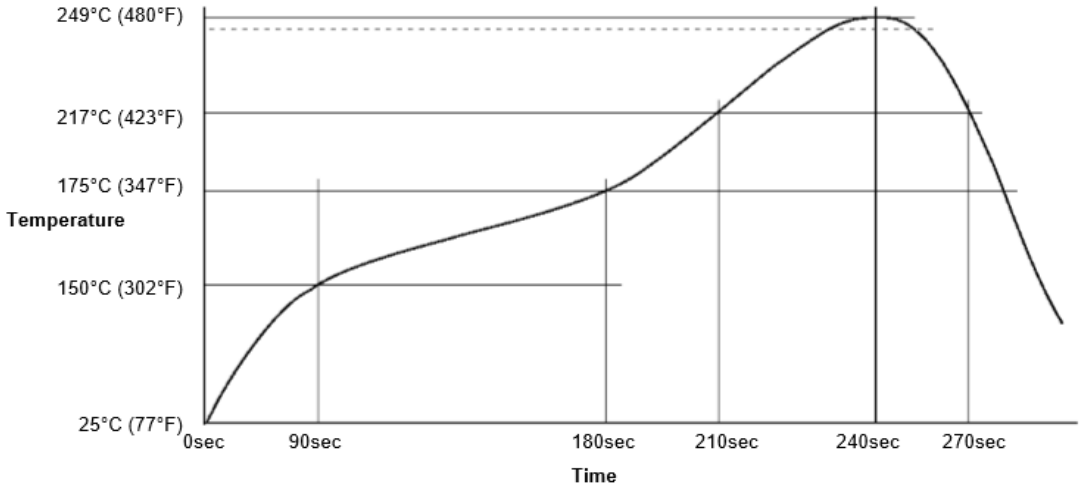
1. Apply tape stencil to blank die piece
2. Apply solder paste
3. Peel off stencil
4. Reflow solder, taking a note of the temperature at which the solder starts to melt and stops melting. These temperatures can serve as the basis of your final temperature profile
5. Determine which apertures deposited enough solder beads to produce a reflowed joint



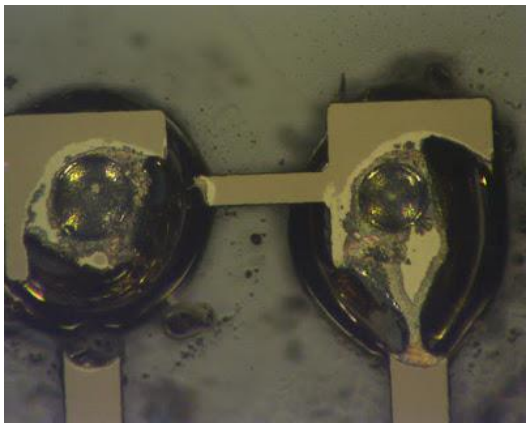
An example of a successful open face experiment is seen on the left. Compared to the sample on the right, the successful sample had more solder balls per joint, so all except the smallest aperture (circled in red) produced a reflowed joint. In the sample the right, the circled joints in the after picture either had no solder balls or only a few before reflow. It is not sufficient to have only a few solder balls to create a joint. Performing these open face experiments allows the selection of a stencil that permits consistent and repeatable reflow for all aperture sizes needed for the final device.

Temperature Profile Experiments

While the datasheet that comes with the selected solder paste gives important information about the appropriate temperature profile required to reflow the solder, that information should only be taken as a starting point for your specific device bonding. The addition of the device substrates and the experimental setup will change the required temperature the finetech heating plate must be at for reflow. As mentioned in the “Open Face Experiments” section, additional tests can be conducted to gain insight about the actual expected reflow temperature.



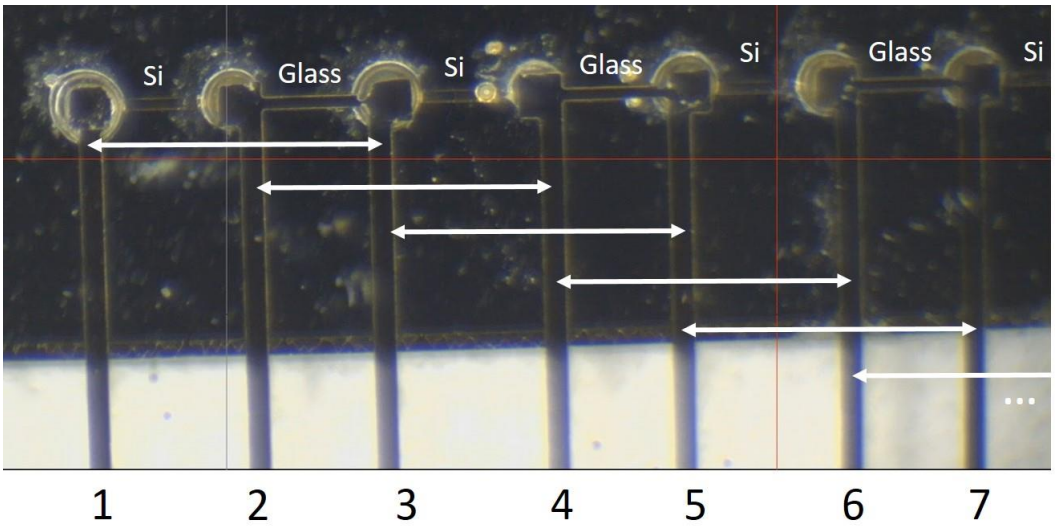
The standard reflow temperature curve has several main components. It is composed of an increasing ramp, a flux bath plateau, a second ramp, a high temperature solder reflow plateau, and a final ramp back down to room temperature. Industry standard holds the flux bath for ~60 seconds and ~30 second for solder reflow. While the plateau hold times can be optimized, the first experimental parameter to be optimized should be the value of the high temperature solder reflow. The reflow temperature should be sufficient to reflow the solder paste without extensively oxidizing the joints. For devices with thin metal traces, high temperatures and holding the reflow temperature for too long may also result in failures such as traces peeling off, as seen below.



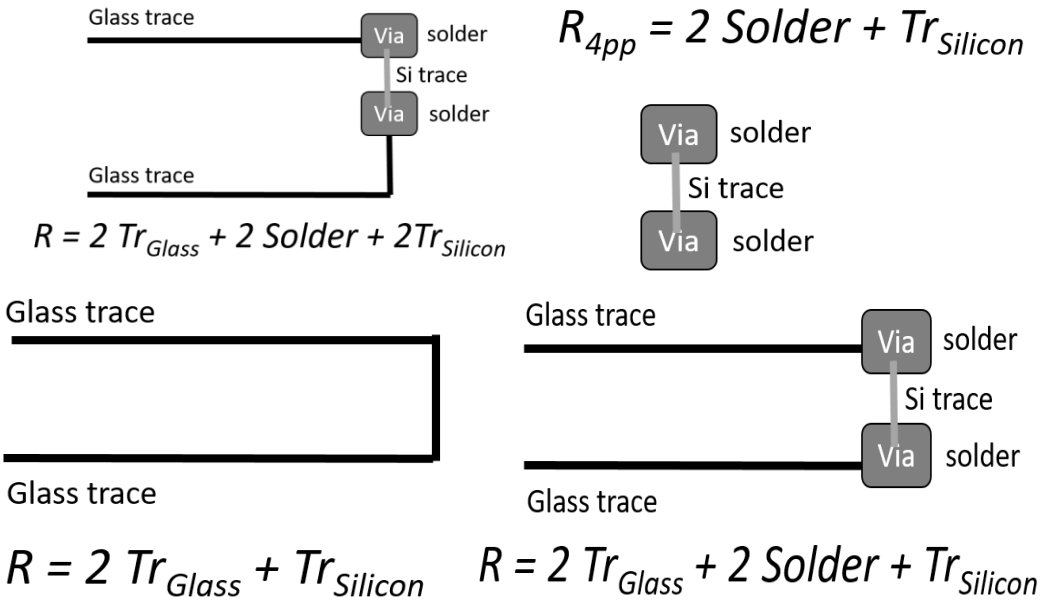
Electrical Characterization

There are several methods to quantify the quality of the solder joint, depending on the application. This project was specifically interested in evaluating the electrical characteristics of the joints. To do so, daisy chains and kelvin structures were used as test structures on the die. Both structures were designed so that the glass substrate hosted leads that connected to resistor traces alternating on the glass and silicon substrates. Hence, to complete a daisy chain and kelvin structure, a solder joint must complete the electrical connection between two adjacent daisy chain resistors. The fabricated devices include two sets of daisy chains and

kelvin structures with different dimension resistors. These devices will now be referred to as the long daisy chain, short kelvin structure, etc. in reference to the length of the connected resistors.

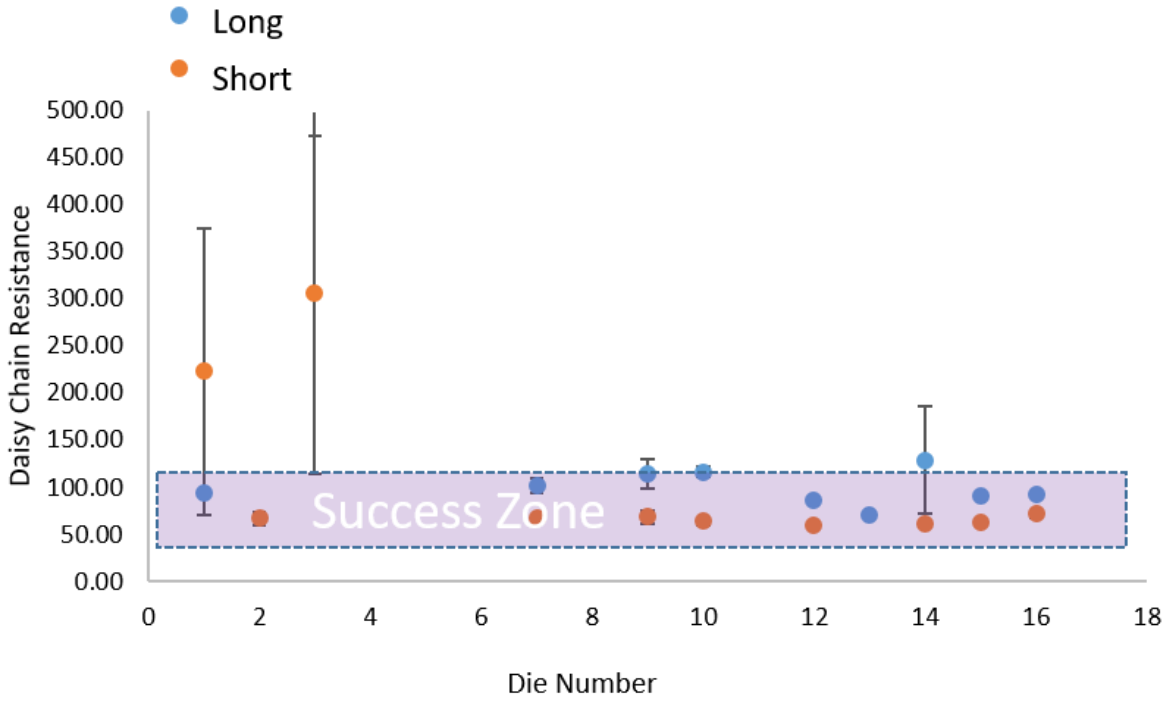


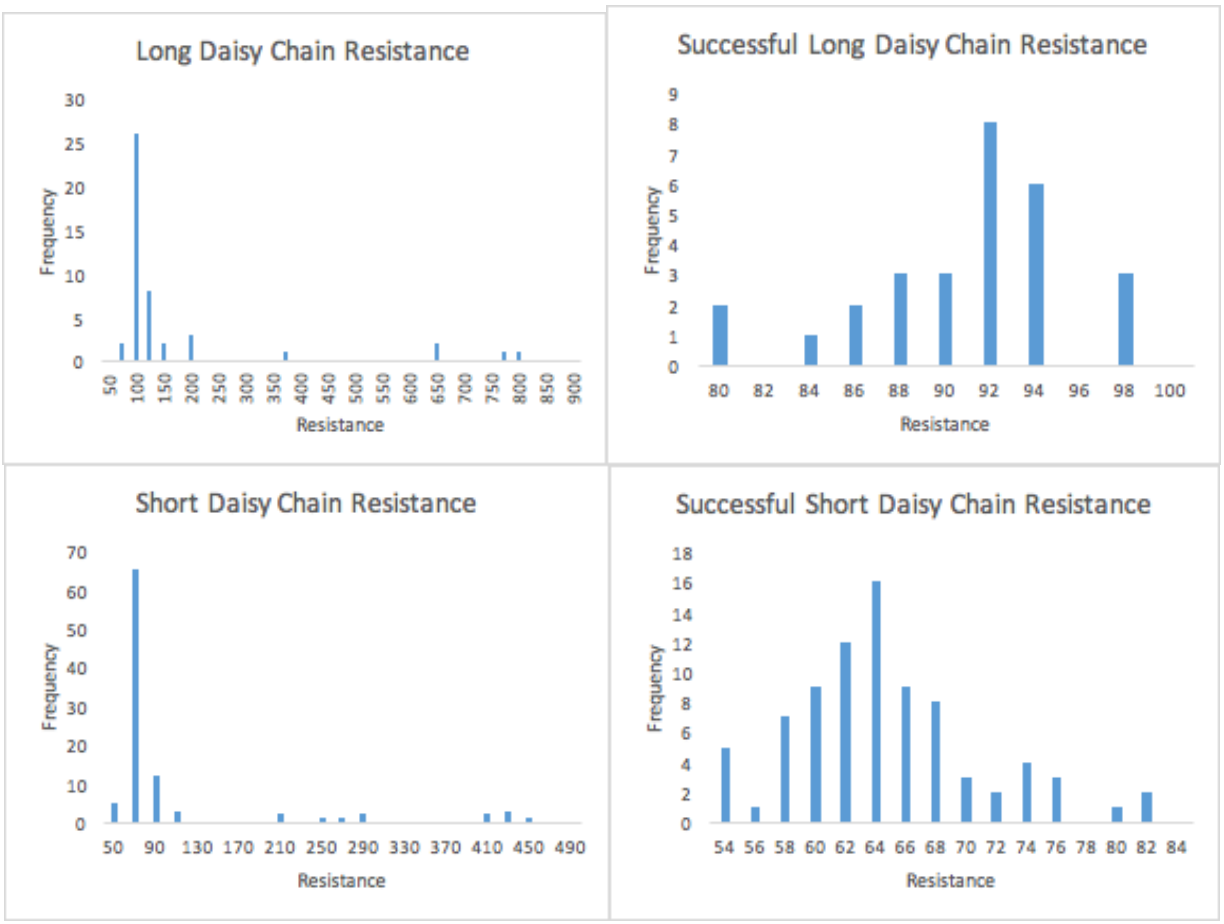
For example, in the above picture, the resistor between leads 1 and 2 lies on the silicon substrate while the resistor between leads 2 and 3 lies on the glass substrate. When measuring the resistance between probe pads 1 and 3, the resistance includes two glass substrate leads, a silicon substrate resistor, a glass substrate resistor, and two solder joints. In this design, the resistors on the glass and silicon substrates are of the same dimensions and hence resistance.



Depending on which probe pads are measured, the resistance measurement will include resistances from the glass leads, silicon or glass resistors, and solder joint resistances. From the 4 types of measurements shown above, the individual resistance contributions can be calculated.

From the electrical measurements of the devices fabricated for this project, it is clear what is the expected resistance of a daisy chain, given a good solder joint. Plotting the resistance values for all the daisy chains gives a gaussian distribution of low resistance, good joint values and sparse, high values for poor joints.

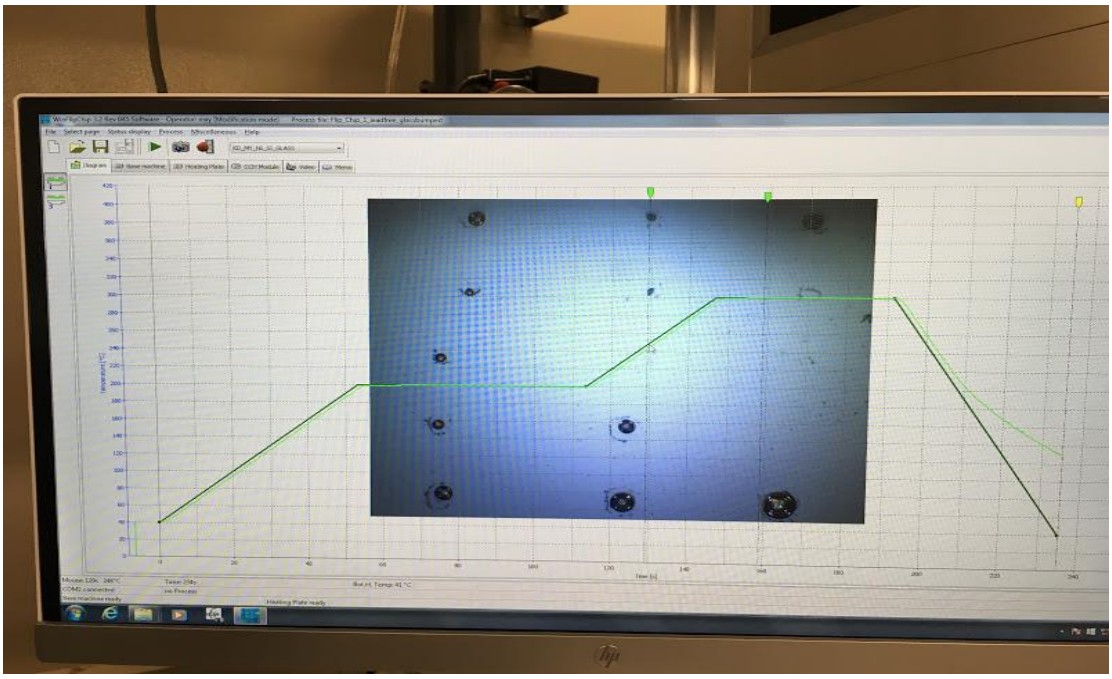




Given the distribution of the electrical resistances, we were able to determine that the average contact resistance of a good solder joint is 2-3 ohms for our fabricated devices. Due to the experimental nature of the project and variation in fabrication and measurement, the true joint resistance may be less than that calculated, but would require rigorous and repeated experimentation of select sets of experimental parameters.

Main Lessons Learned

Below is an image showing the temperature profile we used to heat our flip chip samples, and a table summarizing the key parameters that produced a successful bond for our samples.



Flux Temp and hold time	200 C, 60 seconds
Reflow Temp and hold time	250C, 15-30 seconds
temperature ramps	3 degC/sec
Force	0 N, alignment issues may happen
Bond Pad Sizes	all worked (100 to 300 um)
Heating side	Heat from bottom, Chip head too small

Other good practices include:

- Characterize solder paste temperature profile with open face reflow experiments
- Include space on edge of tape stencil for glass weights
- Design to include windows and large and easy alignment features
- Test flip chip alignment with clear substrate before permanent bonding
- Use thick metal pads (>500 nm) to prevent trace breakage
- Maintain oxide top layer to prevent excessive capillary movement during reflow
- Use base plate for heating instead of head
- Place alignment mark at center of finetech camera viewer
- (Develop melting process with chip holder in place, our results had limited success, to aid alignment issues)

<u>Recommended Future Projects</u>

- Solder voids with Xray Microscopy
- Bond strength via Instron pull tests
- Apply to real devices!
    - EE 410 transistors anyone?

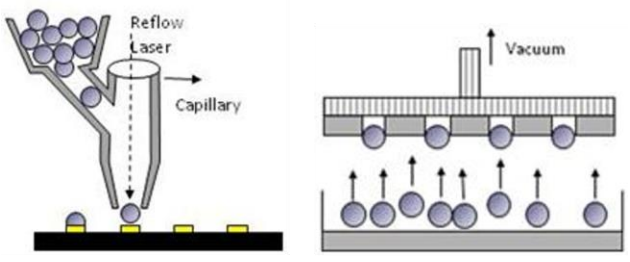


Image credit: Pactech.com

- Shorting - density of pads
- Alloys - High and Low Temp Solder
- Uniformity of Bump Arrays across die
- Use spheres directly
    - Pactech.com provide placement service in the Bay Area
  - Apply solder paste through inkjet printing

Youtube Videos

Applying solder paste via squeegie https://www.youtube.com/watch?v=xRbTOfbuWpw
Removing the tape stencil https://www.youtube.com/watch?v=_1BL19anPeY
Open Si Chip solder melting https://www.youtube.com/watch?v=gFavoGtj6Eg
Failure Mode 1: Misalginment to Alignment https://www.youtube.com/watch?v=JPHrdLWCwMQ
Failure Mode 2: Alignment to Mis-alignment https://www.youtube.com/watch?v=V5zHqwEs_oE
Failure Mode 3: Solder damages traces https://www.youtube.com/watch?v=R1uZxFGqBFU

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