# Au-Sn Eutectic Chip-Bonding for High Heat-Flux Vapor-Chamber Applications

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Introduction

Chip-level bonding between components has been a widely studied subject for decades in the electronics industry, where several bonding methods like high temperature hydrophilic/hydrophobic, fusion, anodic and intermediate metal layer bonding have been investigated.[1] Eutectic bonding, which leverages the diffusion between metal layers at relatively low temperature has gained popularity because of its superior strength, hermeticity and significantly relaxed restrictions on substrate type, roughness and flatness.[2]

Fig. 1: A typical vapor chamber

Bar-Cohen et al. (2015)
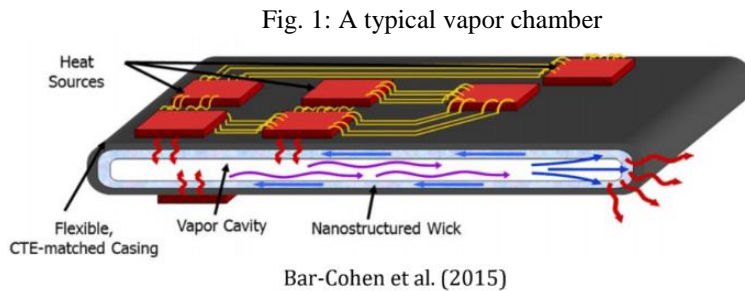
One of the major applications that require precisely controlled eutectic bonding, are vapor chambers for cooling chips and processors which act as localized hot spots in an IC device. Vapor chambers consist of a micro-structured bottom substrate, called the evaporator, which act as liquid reservoirs and provides the surface area required for phase change convective heat transfer to cool the chip kept below while a top condenser acts as a relatively colder site to condense the evaporated liquid. A few tall pillars on either side of the system serve as bonding sites for structural support of the device and simultaneously provides additional paths for liquid to be routed back to the evaporator, thus preventing potentially dangerous scenarios like dry-out and burnt chips. For high heat transfer performance of these cooling systems, it is necessary to optimize the bonds to have as low an area as possible without compromising the strength. Two major issues that plague fabrication yield and reliability are eutectic metal overflow from bonded region and non-uniformity within the bond. Most of the existing bonding studies aim to characterize the bond strength by performing shear tests and observing cross-section images of the bonded region, however hardly any of these studies delve into the details of bond uniformity and metal squeeze-out from the bonded area.

In this study, a detailed characterization of eutectic bonding between Gold and Tin is performed by varying bonding temperature, bonding time and total bond area, with emphasis on metal overflow and uniformity. The aim of this study is to further the understanding of eutectic bonding process as well as facilitate effective low temperature, high strength bonding between chips useful in large scale electronic packaging industry and microfluidic vapor chambers applications.

Sample Fabrication

- *Bottom Substrate*

  Silicon wafers are chosen as our bottom substrate. Vapor chambers are often made out of Silicon for its compatibility and easy integration with high heat generating chips in the semiconductor industry. For our study we have chosen 4 inches K-prime wafer (100 mm). The wafers are marked using diamond scriber and then thoroughly cleaned in Piranha (90% Sulfuric Acid, 10% Hydrogen Peroxide) for 20 minutes followed by SRD (spin, rinse, dry) clean.

- *Alignment Marks Patterning*

The wafers are ready for photoresist deposition after being HMDS primed in the YES Oven. The wafers are cooled down, and Shipley 3612 resist is spin coated on the wafers with 1 micron thickness (with additional vapor priming) and 2 mm edge bead removal in Track2 of the SVGCoat. Using Karlsuss the alignment marks and the dicing lines (Mask 1) are exposed on the wafers. Karlsuss is a contact aligner system which performs precision mask-to-wafer front-backside alignment and near UV photoresist exposure in hard contact. The wafers are exposed for $0.8 - 1$ seconds using hard contact and alignment gap of 30 microns using the mask for alignment marks and dicing lines and then are soft baked, developed and hard baked in SVGDev.
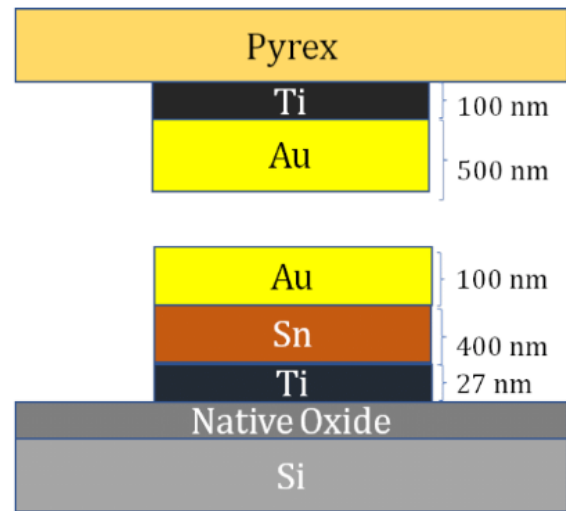

Fig. 2: Schematic of our top and bottom substrates

After developing, the Si wafers are etched in Drytek 2 which is a plasma etcher and uses chlorine-fluorine based chemistry to etch Si. The Si wafers are etched for 2 min 30 sec to 2 min 45 sec to get an etch depth of 300-400 nm and then characterized in the alphastep 500 profilometer. The photoresist is then stripped using Piranha for 30 minutes in a clean wet bench and SRD cleaned. It was observed that wafers when etched to depths of more than a few microns, broke during SRD clean.

- *Bonding Site Patterning*

The wafers are again subjected to the "Substrate Clean" and "Alignment Mark Patterning" process expect that now Mask 2 is used in Karlsuss to pattern the bonding sites instead of mask 1 and then developed in SVGDev. After developing, the wafers are descumed in Drytek 2 and are now ready for metal deposition.

- *Metal Deposition*

Innotec, an E-beam evaporator system that gives controlled film thickness of less than $1 \ \mu m$ is used for metal deposition. Since evaporation is a directional process using Innotec for metal deposition proves to be beneficial during lift-off patterning. In general, the adhesion of evaporated films to the substrate is worse than sputtering the same film/substrate combination. Adhesion depends on the film material, the substrate material, and the stress in the film.[3] A thin "adhesion layer" of Ti is first deposited to the native oxide which acts as an adhesion layer. It is followed by deposition of Sn and then Au without breaking vacuum to prevent oxidation of Sn.

Titanium thin films are largely employed in electronic and micro-electromechanical devices as adhesion layer between insulators and conductive metallic layers, e.g. Au used for electrical contacts and signal transmission lines. Here, we are not concerned about the thin film inter-diffusion between Ti/Au which promotes the formation of $TiAu$ intermetallics and/or, if Ti diffuses through Au up to the free surface – the formation of TiO_2, which in turn can cause an undesired ohmic resistance, since

substantial thickness of Au is deposited over a layer of Sn.[4] Also, the native oxide acts as a diffusion barrier to prevent Au and Sn from diffusing into the Si substrate.

- *Lift-Off*

Several studies have reported problems in performing lift-off when the deposited metal layer stack is thicker than the photoresist thickness, where the chemical used for lift-off is unable to penetrate the metal layer to the PR layer.[5] In our case, the thickness of the total metal layers deposited are of the order of 500 - 600 nm while the photoresist thickness is 1 micron, and we had no problems in lift-off, even without the use of Lift-Off Layer (LOL). For applications requiring a thicker metal layer, it is recommended to use a thicker photoresist, which will eventually change the subsequent exposure and development recipes. After metal deposition, the wafers are immersed in Remover PG overnight after which they are cleaned thoroughly with acetone in an ultrasonic bath. The fig. 3 shows wafers after proper and partial development.
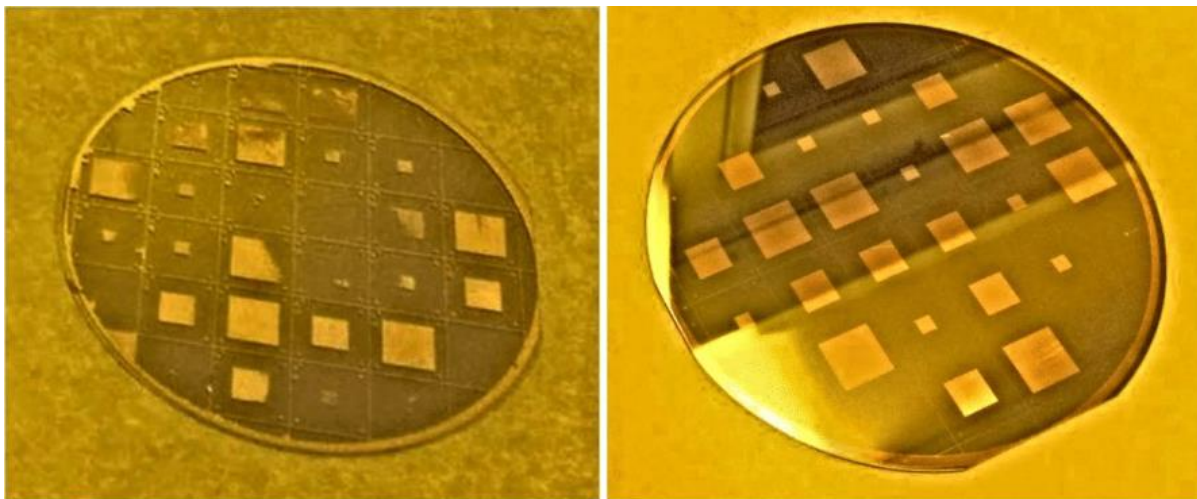
(a) Partial Development   (b) Complete Development

Fig. 3: Attempts at Lift-Off after complete and partial development (bad double exposure recipe)

- *Top Substrate*

To facilitate detailed observation of the Au-Sn eutectic alloy through a microscope, we have chosen Pyrex as our top substrate. Pyrex 7740 borosilicate is a good choice because its thermal expansion coefficient matches closely to that of Silicon (Pyrex: $32.7 \; x \; 10^{-7} \; {}^{o}C$ over a temperature range 0 to 300 ${}^{o}C$; Silicon: $30 \; to \; 38 \; x \; 10^{-7} \; {}^{o}C$ over a temperature range of -70 to 430 ${}^{o}C$)[6] thereby also making it suitable for wafer level bonding, but it suffers from the drawback of relatively low thermal conductivity (Pyrex: 1.15 W/mK; Silicon: 70 W/mK (0K) to 30 W/mK (500 ${}^{o}C$))

The wafers were thoroughly cleaned for more than 30 minutes in Piranha (90% Sulfuric Acid, 10% Hydrogen Peroxide) and then cleaned in the SRD cleaner. Following HMDS priming in the YES Oven, the wafers are ready for deposition of photoresist. After the wafers cool down, Shipley 3612 resist is spin coated on the wafers with 1 micron thickness (with additional vapor priming) and 2 mm edge bead removal in Track2 of the SVGCoat. The KarlSuss Contact Aligner was used to expose the wafers for 0.8 - 1 seconds using hard contact and alignment gap of 30 microns using the first mask for alignment marks and dicing lines, then they are developed in SVGDev.

- *Double Exposure*

Unlike Silicon, instead of etching the Pyrex wafers, we have chosen to lay metal on the alignment marks and dicing lines, thus getting rid of an extra set of lithography steps. This would require us to expose the Pyrex wafers immediately after the first development stage with our second mask (which opens up small windows of varying size for metal deposition for subsequent bonding). It should be noted that this type of multiple exposure is possible only when the developer use, in this case, MF-26A (2% TMAH) doesn't react with the unexposed photoresist. The KarlSuss was used again to align and expose the developed Pyrex wafers through the second mask. It was seen that the second exposure if done for 0.8 - 1 seconds, which is standard for 1 micron thick 3612 resist is not enough. A thin layer of Photoresist (as seen in fig. 4 in pink) remained on the windows which was not developed away. In later steps after metal deposition and lift-off, this Photoresist residue affects uniformity of deposited metal layers and also causes metal to be partially stripped away from these areas deeming these wafers unusable (Fig. 3)

This problem during multiple exposure is observed because of way the first development is done, which involves two baking steps, a post-exposure softbake and a post-development hardbake. These baking steps improve unexposed PR adhesion to the wafers, improves chemical stability and structural integrity of the PR layer still existing on the wafers. Because of this improved adhesion and stability of the PR layer, the second exposure has to be performed for a longer duration. It was seen that, typically around 1.6 - 2 seconds of exposure is sufficient for the next exposure step. An alternative could also be the multiple exposure option in the KarlSuss. Three exposures for 0.7 seconds each at an interval of 5 seconds works satisfactorily as well.
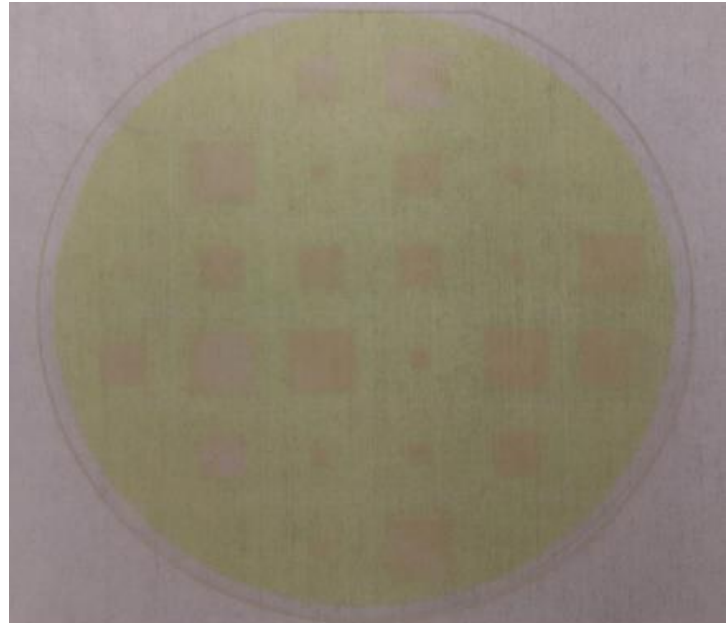

Fig. 4: Pink PR residue left on pyrex (result of bad double exposure)

In our case, to ensure that there is no photoresist left on the windows, the second mask was exposed first, and following spray development, the second mask was exposed with a larger UV dose. If multiple exposure-development cycles are done correctly one should observe no yellow/pink residue on the exposed parts of the wafer, instead they should appear transparent.

Dicing

The Si and pyrex wafers are now ready to be diced. Using the Disco Wafer-Saw, the wafers are diced along the dicing lines (using softer Resin blade) and the chips are cleaned using SRS-100 (SRS-100 consists of: N-Methyl-2 pyrrolidone (NMP) 60%, Tetramethylene sulfone 30%, Isopropanolamine 10%) at a temperature between 50-60 ^{o}C for 20 minutes and then manually rinsed and dried. It has been observed that SRS-100 is more effective in removing photoresist layer that has been developed and hard-baked. The Si and pyrex chips are then bonded using Finetech Lambda flipchip bonder.
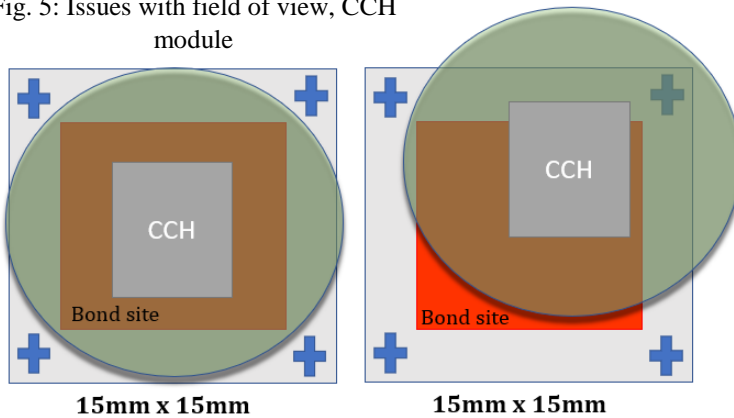
Bonding

Finetech Lambda flip-chip bonder is a versatile chip bonder that allows bonding of chips using pickup-tools: heating plate module and CCH (chip heating module) module. The maximum heating temperature that can be reached is 400 ^{o}C. The sample sizes range from 5mm x 5mm to 50 mm x 50 mm. The manual arm allows adjustment of bonding force between 0.1N to 100N. Despite its popularity it has several drawbacks that one needs to consider before using it for chip bonding.

The *Si* chip is placed on the substrate plate and the pyrex chip acts as a die which is picked up by the CCH module. The chips are then aligned by viewing through the camera and adjusting the x, y, z travels and the theta fine travel. The CCH module is lowered and the required force is applied using the manual bonding force module for the eutectic bonding to take place.

One of the major issues faced while using the flip-chip bonder was alignment with large chip sizes. The maximum field of view of the camera which is used to align the top and the bottom substrates is roughly a circle of 0.6 mm diameter at the lowest magnification. Thus, we need to make sure to design the alignment marks in the field of view of the camera, especially for our samples with bond areas 49 mm^2 and 100 mm^2.

Fig. 5: Issues with field of view, CCH module

15mm x 15mm   15mm x 15mm

Alternatively, it is possible to pick up the substrate at the location of the alignment marks, but this would decenter the bonding area from the CCH module causing non-uniform heating and non-uniform pressure application on the bond area. (Fig. 5) This ultimately leads to partial bonding. Application of uniform pressure and temperature being a key requirement in eutectic bonding, our samples were picked up from the center and this pushed the alignment marks out of the field of view. Alignment was performed using the four sides of the bond area, made possible because the camera can be translated and tilted to a small amount. Tilting the camera by more than a few degrees is not desirable since it causes parallax errors and makes the top bond site appear slightly bigger than the bottom site. To deal with these problems, one should design the alignment marks to be within the bond area and well within the field of view of the camera such that tilting can be avoided as much as possible.

Additionally, non-uniformity of bonding pressure applied is a drawback which is inherent to the working of the Finetech Lambda flip-chip bonder. The top arm of the bonder closes in radially and contacts the bottom plate. A side camera is used to view and align the two plates as parallel as possible. Absence of any kind of electronic or mechanical system
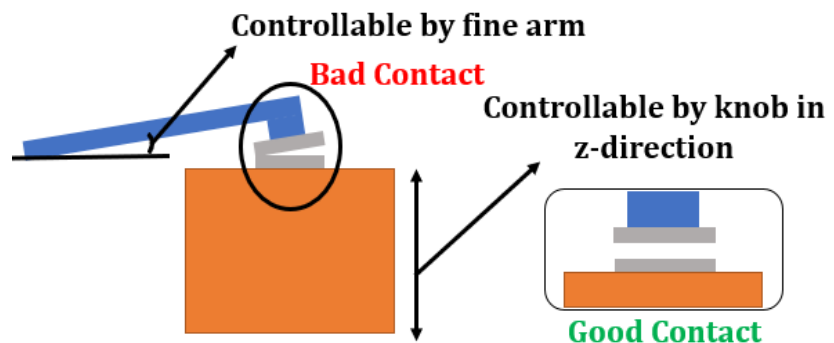

Fig. 6: Issues with flat contact between top and bottom substrate

that measures the flatness of the two substrates before the start of the bonding process is a major drawback of the current bonder system. Because of human error in judging flatness of each set of samples, repeatability of an experiment is lost and we never obtained any two sets of reproducible pressure distribution in our samples. This does not become a huge issue when the chip sizes are very small, of the order 5 mm or less, but for large samples like ours which are 1.5 cm in size, a slight tilt can amount to huge pressure difference between one side of the sample and the other, and this is a problem faced while bonding most of our samples. (Fig. 6, 7)
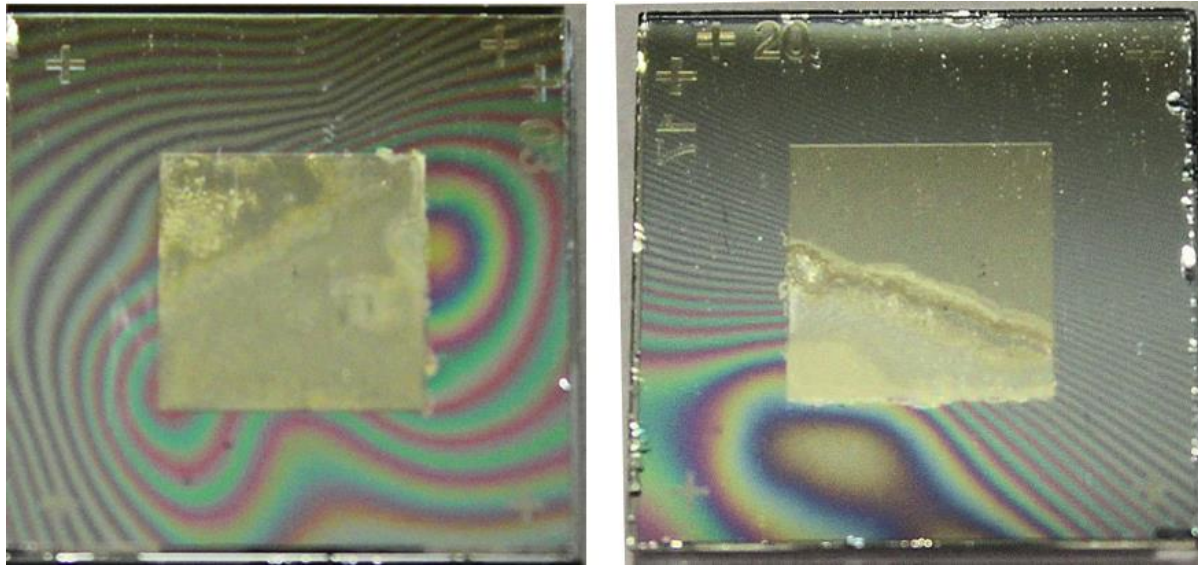

Fig. 7: Bonded substrates showing uniform (left) and non-uniform pressure application (right)

Results and Discussions

There are several options available when it comes to the choice of material for eutectic bonding. A few most commonly used and investigated are Au-In, Cu-Sn, Au-Sn, Au-Si, Au-Ge bonding techniques. Among these, Au-In has a very low eutectic reaction temperature of 156 $^o C$ and is very attractive for bonding chips and wafers which are sensitive to high temperature, but it has been observed that under several situations, formation of bulk amount of intermetallics like $AuIn_2$ can drastically decrease bond strength and quality[7]. Previous studies also observed that In tends to flow a lot and squeeze out of bond area if excess pressure is applied. Au-Si bonds have a eutectic temperature of 370 $^o C$ which is beyond the temperature limit of the Finetech Lambda Flip-Chip bonder. An attractive and low-cost alternative is Cu-Sn, which provides low bond temperature of 230 $^o C$ but is very susceptible to oxidation of the metals, especially in cases where forming gases are not used to keep the atmosphere O_2 free. Au-Sn bonds are a reasonable compromise with eutectic reaction temperature of 280 $^o C$ with the Au layer deposited above Sn preventing Sn oxidation. Moreover, Au-Sn bonds have shown superior mechanical properties like high strength and low Young's modulus. It is widely used in SLID bonding of chips and wafers, multilayer bonding, bonding of high area chips and microsensors.[8] Following the needs specific to vapor chamber applications, where the requirement for bond strength and hermetic seal is a much more important parameter than temperature, we have selected Au-Sn for our eutectic recipe.

- *Design of Experiment*

The bonding temperature has been studied to be one of the most important parameters in any kind of eutectic bonding process. It has also been observed that the cooling rate and temperature gradient in the eutectic zone affects growth rate and amount of the microstructure and also determines the grain size of the final alloy.[7] An important parameter in our DOE is, therefore, temperature of the two elements (base and the CCH module) of the flip-chip bonder.

Our choice of temperature of the CCH module and the base heating plate is determined by previous studies by Jung and Kwon[10] where they reported better bonding at the highest T_bond available, 379 ^oC. The bonding temperature profile used is a conventional and very widely used profile (as shown fig. 7). We have chosen their best results as reference for setting up our DOE for the base heating plate-

- o T_bond $= 350\,^oC$
- o T_bond $= 320\,^oC$
- o T_bond $= 379\,^oC$

Fig. 7: Temperature/Pressure profile of the flipchip bonder

The low conductivity of pyrex (1.15 W/mK) is a big barrier to heat transfer from the top CCH module to the metal bond layers and thus the top module is always kept at the highest temperature available, 379 ^oC to ensure that the metal layers on the top substrate reaches sufficiently high temperature.

Previous ENGR241 project by Jung and Kwon[10] observed that bonding force is another significant variable. Applications specific to vapor chambers require us to have good bond strength while having as low a bond area, as possible, so as to maximize the remaining area for heat transfer. Thus, two more variables that get automatically added to our DOE are bonding force and area.

We have selected 3 bond areas -

- o 1 cm x 1 cm
- o 0.7 cm x 0.7 cm
- o 0.3 cm x 0.3 cm

These have been chosen such that they are respectively 100%, 50% and 10% of the maximum bond area, 1 cm^2. Also, it should be noted that the sizes of our vapor chambers vary from 4 to 9 cm^2, and thus the maximum bond area in our DOE corresponds to only 25% to 10% of the chip area, which will provide us with reasonable heat transfer performance.

The work of Jung and Kwon[10] concluded that the eutectic bonding occurs by an initial thermocompression bonding between Au-Au and then Eutectic reaction between Au and Sn. The pressure required for achieving thermocompression bonding between Au-Au is reported to be of the order of 1 MPa or higher. Three forces chosen and their corresponding pressures were -

- o 50 N
- o 70 N
- o 100 N

Table 1 : Design of Experiment

Sample	Bond Parameters					
	$T_{uniform}$(°C)	$\Delta T_{uniform}$(min)	T_{bond}(°C)	ΔT_{bond}(sec)	Force(N)	Cooling(sec)
Small1	300	5	320	1500	50	1000
Small2	300	5	350	1500	50	1000
Small3	300	5	379	1500	50	1000
Small4	300	5	320	1500	70	1000
Small5	300	5	350	1500	70	1000
Small6	300	5	379	1500	70	1000
Small7	300	5	320	1500	100	1000
Small8	300	5	350	1500	100	1000
Small9	300	5	379	1500	100	1000
Medium1	300	5	320	1500	50	1000
Medium2	300	5	350	1500	50	1000
medium3	300	5	379	1500	50	1000
Medium4	300	5	320	1500	70	1000
Medium5	300	5	350	1500	70	1000
Medium6	300	5	379	1500	70	1000
Medium7	300	5	320	1500	100	1000
Medium8	300	5	350	1500	100	1000
Medium9	300	5	379	1500	100	1000

- *Multilayer Bonding*

  Multilayer bonding has been investigated for several applications where several Sn and Au layers are sandwiched between each other, which show better diffusion between Sn and Au and thus better bond quality.[10,11]

  But in our case, we have avoided multilayer bonding to decrease thermal resistance, which is a key parameter in applications involving heat transfer. Several nano-layers deposited on top of each other drastically increases the thermal boundary resistance of such stacks.[12] Experimental investigation of multilayer bonding vs bonding with less metal layers could be an interesting future study to investigate the trade-off between thermal resistance and bond strength and thus optimize multilayer bonding methods.

- *Bond Quality Assessment*

  Usually, shear tests and some other mechanical failure test is performed to characterize the bond strength of such experiments. Bond quality assessment is also performed by viewing bond cross-sections under an SEM or TEM[10] and components of bond site evaluated using X-Ray spectroscopy (EDS) and diffraction (XRD)[11]

The glass substrate used as top substrate enables us to view the bond from top, an information which is usually not available when the top and bottom chips are both Si. Because of imperfect pressure distribution while using the flip-chip bonder, it was observed that many of the sample showed partial bonding. Using larger samples, shows increase in the unbonded region because of increased pressure non-uniformity. Fig. 7 and fig. 8 shows samples with varying degree of bonding within the metalized
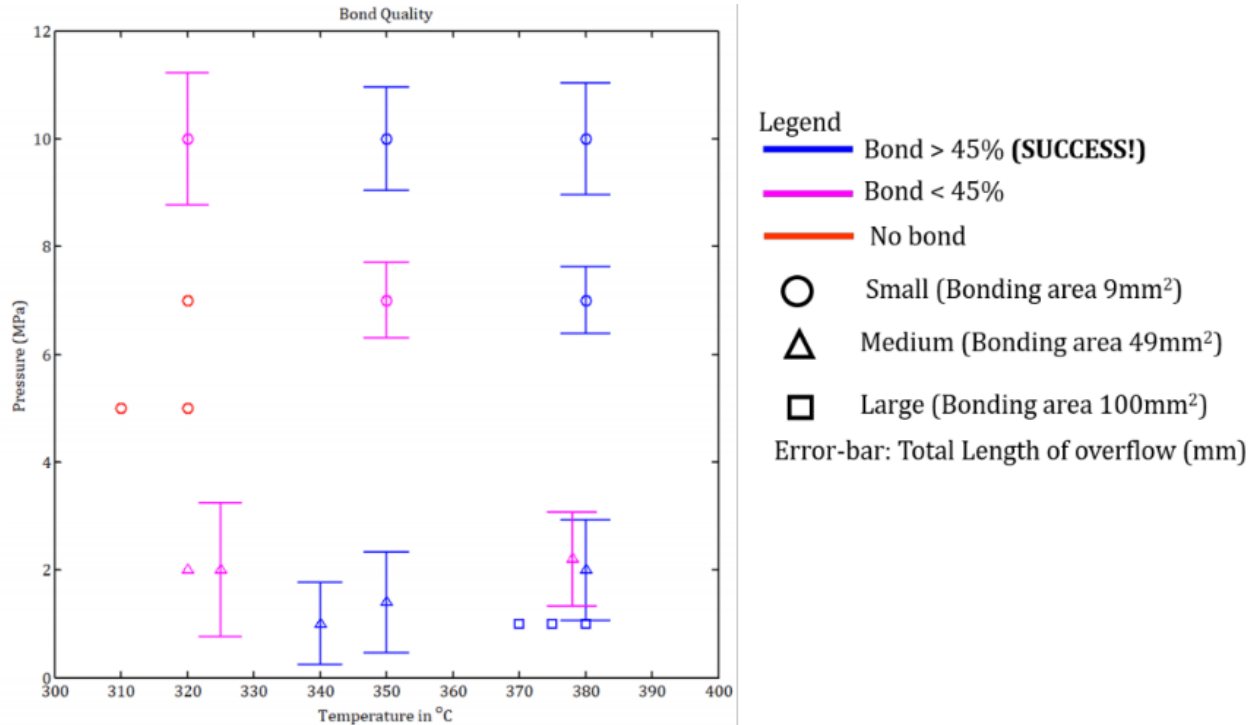
Plot. 1: Bond Quality Plot

region.

We have used the percentage of bonded area as a metric to assess bond quality. Samples with more than 40 - 45 % bonded region is categorized as good bonds while samples with low eutectic alloy area were classified as partial or bad bonds. Table 1 shows almost the entire matrix of our DOE and classifies the samples based on quality of bond, temperature and pressure. The vertical-bars on some of the samples denote the total length of bond perimeter from which overflow is observed. The samples which do not have these, show no or very little overflow.

The plot (plot. 1) shows that successful bonds are formed generally at a higher temperature. We observe a total of 6 samples being badly bonded or showing no bonding around a temperature of 320 ^oC, which indicates that 320 ^oC temperature of the base plate is not able to supply enough heat to the metal layers for eutectic bonding. We observed this after proceeding halfway through our DOE, and so we changed our DOE to perform experiments on samples at a relatively higher temperature of more than 340 ^oC.

It was observed that even though, small samples showed much higher bond area percentage, they were much weaker than larger samples which showed same percentage of bonded region. It was also concluded that for large sample sizes as ours (1.5 cm x 1.5 cm), bond area of only 10 mm² is too low for required bond strength.
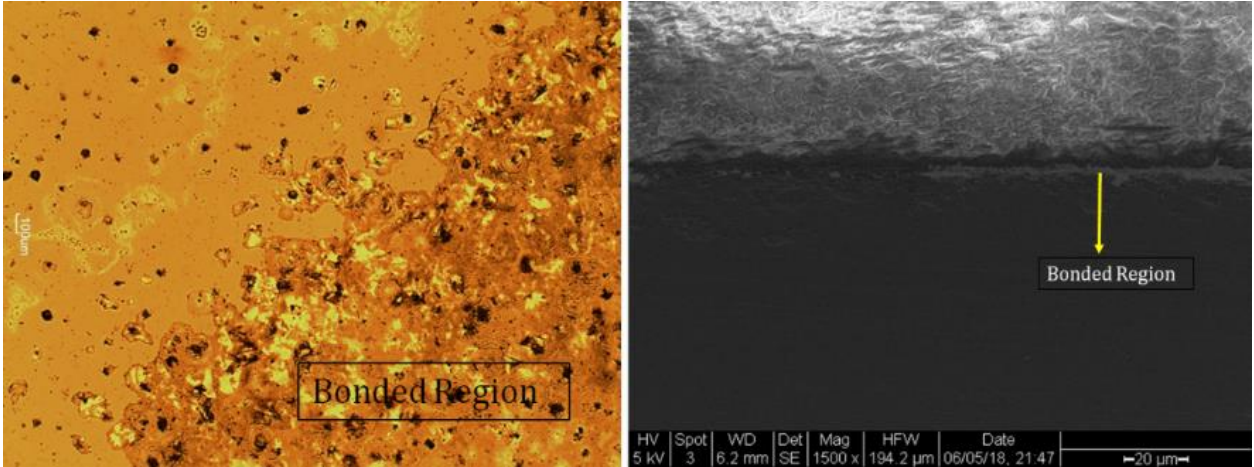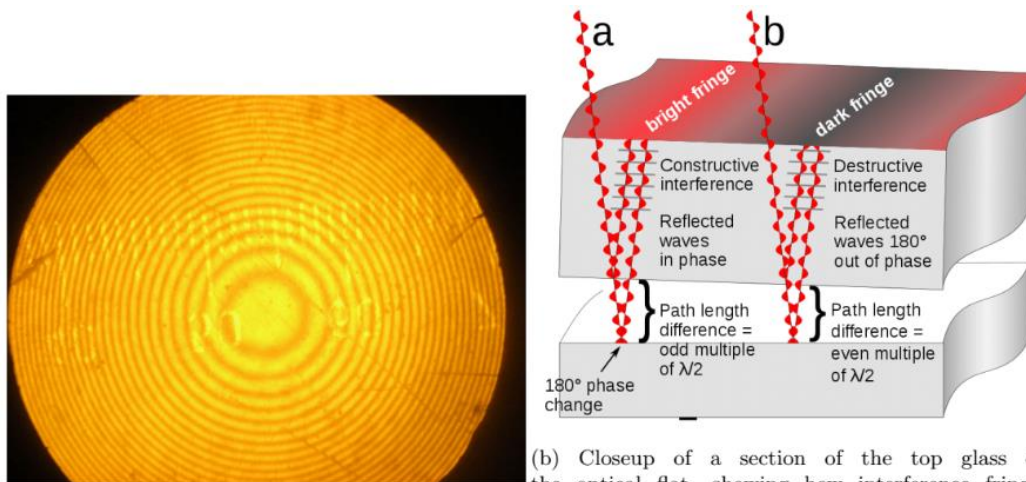

Fig. 8: Images showing bonded and non-bonded region in Optical microscope (left) and SEM (right)

Images taken using the optical microscope and later SEM sections reveals clearly the bonded and unbonded parts within the sample. (see fig. 8)

- *Effect of Pressure*

Another indirect result of use of a transparent top substrate is formation of interference fringes. The schematic in fig. 9 (ref. Wikipedia) shows how interference rings are formed when a thin layer of air is entrapped between a transparent substrate and another bottom substrate. The distance between the fringes correspond to change in air layer thickness between the two substrates and is proportional to the wavelength of visible light.
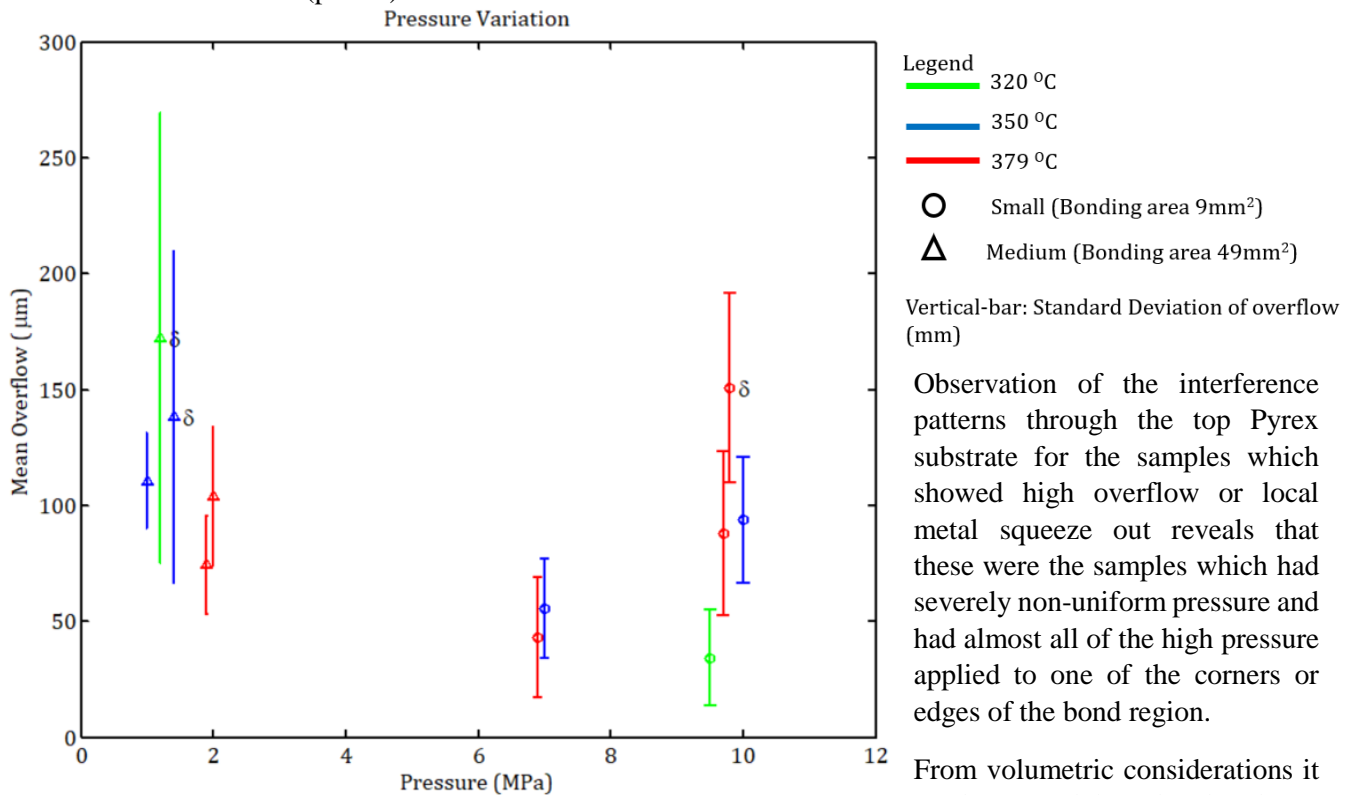

(a) Newton's rings observed through a microscope. The smallest increments on the superimposed scale are 100m. .

(b) Closeup of a section of the top glass on the optical flat, showing how interference fringes form.(a)The reflected waves reinforce, resulting in a bright spot(b)The reflected waves cancel, resulting in a dark spot.

Fig. 9: Schematic showing formation of interference fringes

From fig. 7, we can make some comments about the quality and flatness of contact achieved in the flip chip bonder. Closely spaced rings indicate that the change in air layer thickness occurs rapidly as we move across fringes, which means that the gap between top and the bottom substrates are not perfectly uniform, while chip areas where fringes are far apart from each other, show good contact between the top and the bottom plate. This is further confirmed by the fact that good bonding takes place where the fringes are far apart from each other and where uniform large pressure has been applied throughout the process. In other areas with closely spaced fringes, we observed inferior bond quality which also indicates insufficient and non-uniform pressure application in these areas.

Fig. 7 shows clearly the visible interference fringes and without having to do any complicated analysis we can gauge whether the contact quality and pressure distribution throughout the sample during the bonding process was uniform enough. Because of this non-uniformity, the study of effect of pressure on squeeze out is challenging.

The data points represent the mean overflow or spread width with the vertical bars corresponding to the standard deviation of the data. The delta signs next to some data points are the ones which show high localized overflow. (plot. 2)

Plot. 2: Overflow with Pressure variation

Legend
— 320 °C
— 350 °C
— 379 °C

○ Small (Bonding area 9mm^2)

△ Medium (Bonding area 49mm^2)

Vertical-bar: Standard Deviation of overflow (mm)

Observation of the interference patterns through the top Pyrex substrate for the samples which showed high overflow or local metal squeeze out reveals that these were the samples which had severely non-uniform pressure and had almost all of the high pressure applied to one of the corners or edges of the bond region.

From volumetric considerations it can be gauged that a low bond area will decrease the chances of overflow, which can also be observed from the plot where we see the average overflow of the smaller samples are much smaller than larger samples.

Among all the medium samples, the one that shows the best result based on overflow width and observing the interference fringes of the sample reveals that more or less uniform pressure had been applied during the bonding process. This further establishes that the magnitude of pressure is not a very critical parameter as long as it is of the order of 1 MPa (to establish good contact between substrates and facilitate Au-Au thermocompression), but what is more important during bonding of large sized samples is the uniformity of the pressure applied by the CCH holder.

(a) Overflow 1 of Au-Sn Eutectic bond

(b) Overflow 2 of Au-Sn Eutectic bond

(c) Localised Overflow 1

(d) Localised Overflow 2
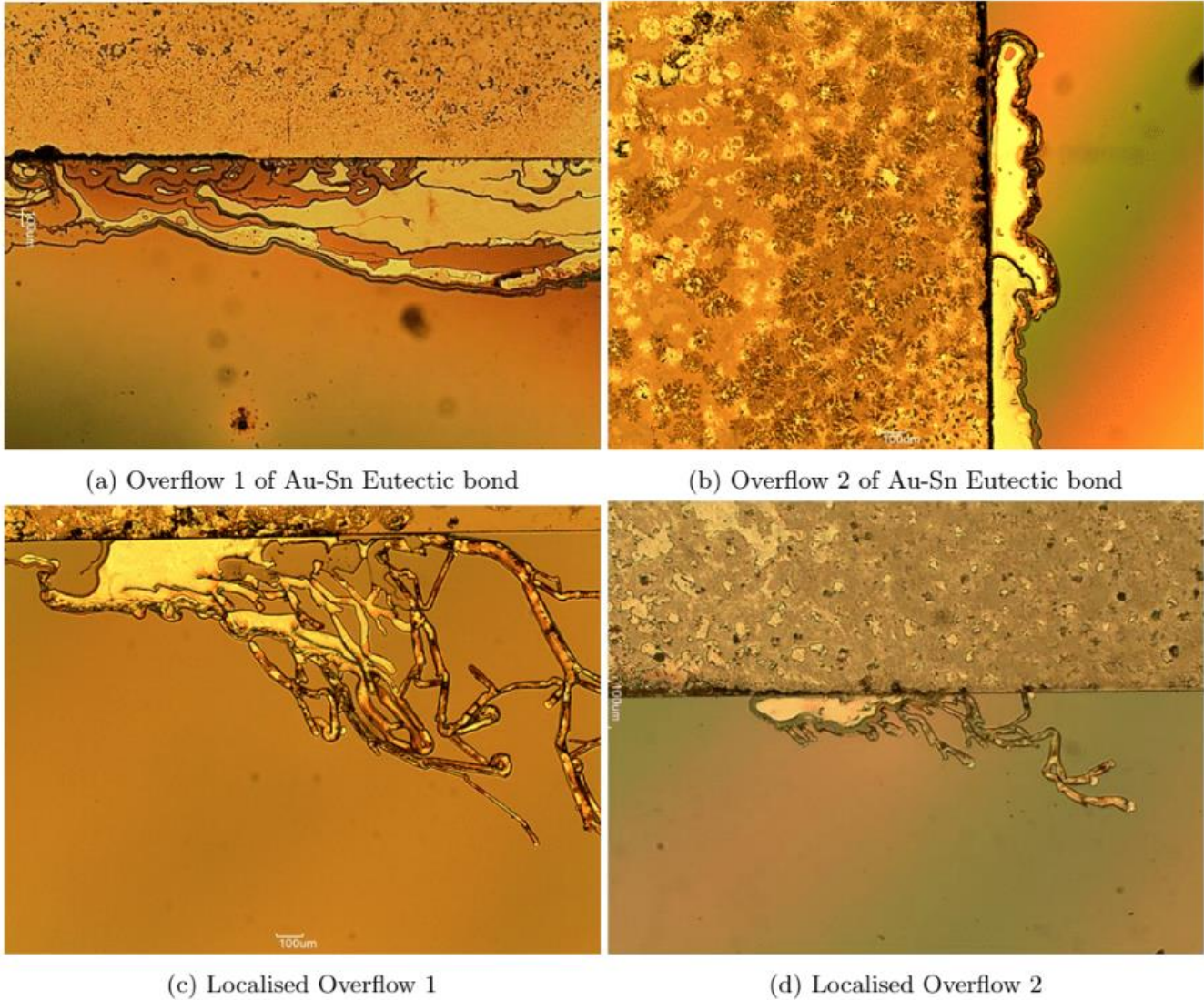
Fig. 10: Few examples of overflow observed while bonding

- *Possible fix for pressure non-uniformity*

   In the current system, a crude way to correct for application of non-uniform pressure is to perform a small experiment by changing the z-positions and recording the location which gives best contact (judged by observing interference fringes). The optimal z-location will be very sensitive to the thickness of the substrates and the metal layers and so cannot be generalized for all kinds of experiments.
   When the temperature is kept well above the Eutectic temperature, pressure uniformity has been established as the most critical parameter affecting bond quality, uniformity and strength, which makes
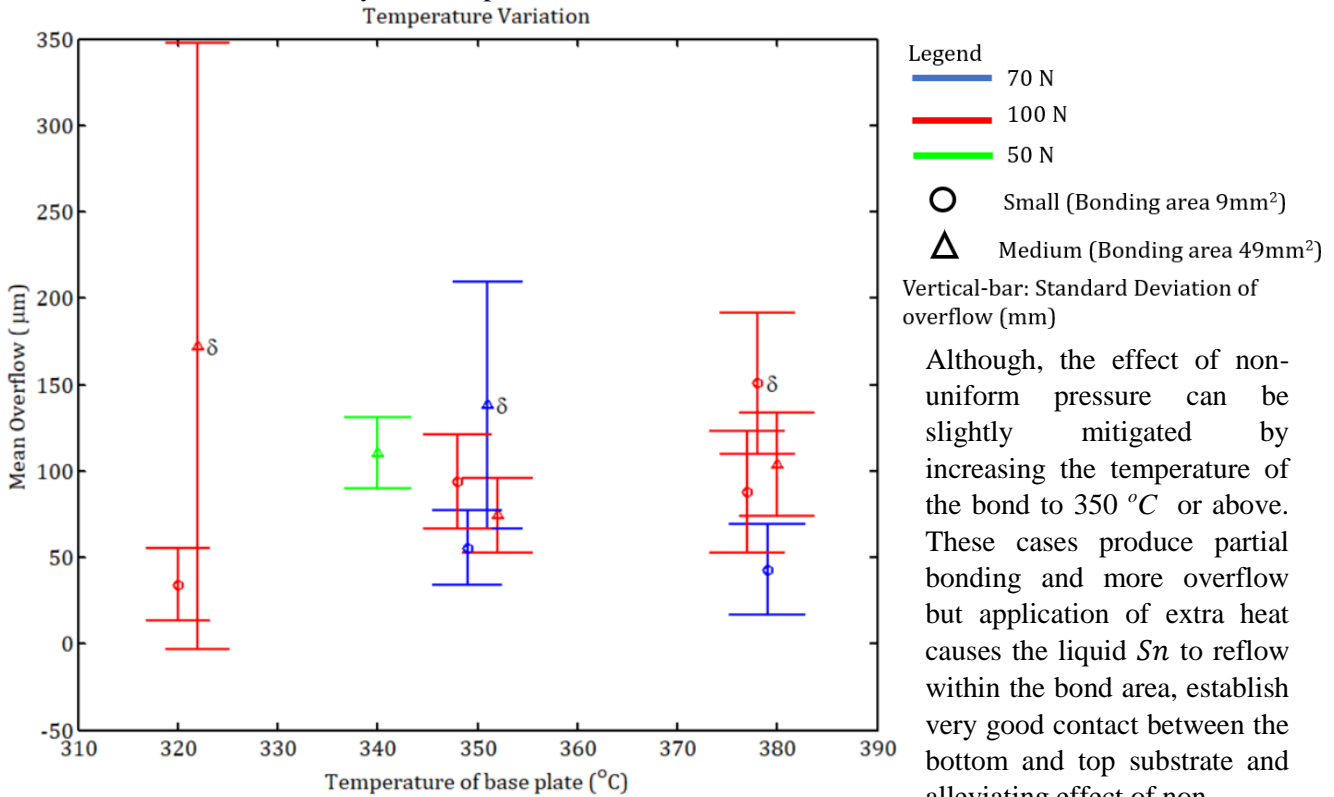
it worthwhile to do this small experiment with top substrate as pyrex and determine the z-location which provides best contact between the substrates.

- *Effect of Temperature*

Plot. 3 shows all the experiments that exhibit significant overflow with varying temperature of the base plate. The circular data points represent the small samples with size 10 mm^2 and the triangular data points represent medium samples with size 50 mm^2, the varying colors in the figure corresponds to the different forces used.

It is erroneous to set a general trend in the data without eliminating the samples with localized high metal squeeze out. Once we remove them, we observe a general increase in overflow with increasing temperature for the same type of samples with same forces. A clear trend can never be established using the flip-chip bonder because of the issue of non-uniform pressure application (if the samples are not flat during bonding) caused by radial descent of the CCH module as discussed earlier, which makes all our experiments unrepeatable.

Additionally, while performing bonding, it was observed that there was no bond formation for 3 samples which were bonded at 320 $^o C$. There were two samples which bonded at 320 $^o C$ but in these two cases extremely uniform pressure was applied throughout the bond area, therefore it was interfered that in absence of a very uniform pressure, 320 $^o C$ is too low for eutectic bond formation.

Legend
— 70 N
— 100 N
— 50 N
◯ Small (Bonding area 9mm^2)
△ Medium (Bonding area 49mm^2)
Vertical-bar: Standard Deviation of overflow (mm)

Although, the effect of non-uniform pressure can be slightly mitigated by increasing the temperature of the bond to 350 $^o C$ or above. These cases produce partial bonding and more overflow but application of extra heat causes the liquid Sn to reflow within the bond area, establish very good contact between the bottom and top substrate and alleviating effect of non-

Plot. 3: Overflow with Temperature variation

uniform pressure application. Although, if high pressure is severely concentrated on one edge and bonding time and temperature is increased many fold, it is possible to cause excessive overflow from one edge of the bond and tin oxidation at the edge. It is therefore, critical to find an optimal balance of temperature and pressure.

- *Misalignment and overflow restriction*

As described in earlier sections, the limited field of view of the flip-chip bonder is a major hindrance to the alignment of our 1 cm x 1 cm bond area samples, so almost always these samples were found misaligned after bonding. Despite misalignment, the bonds were strong and percentage of bond area were almost always much higher than 50% of the total area. Furthermore, bond area misalignment of orders of 100 microns, which was initially associated with increased overflow, showed very little or no overflow (see fig. 11)
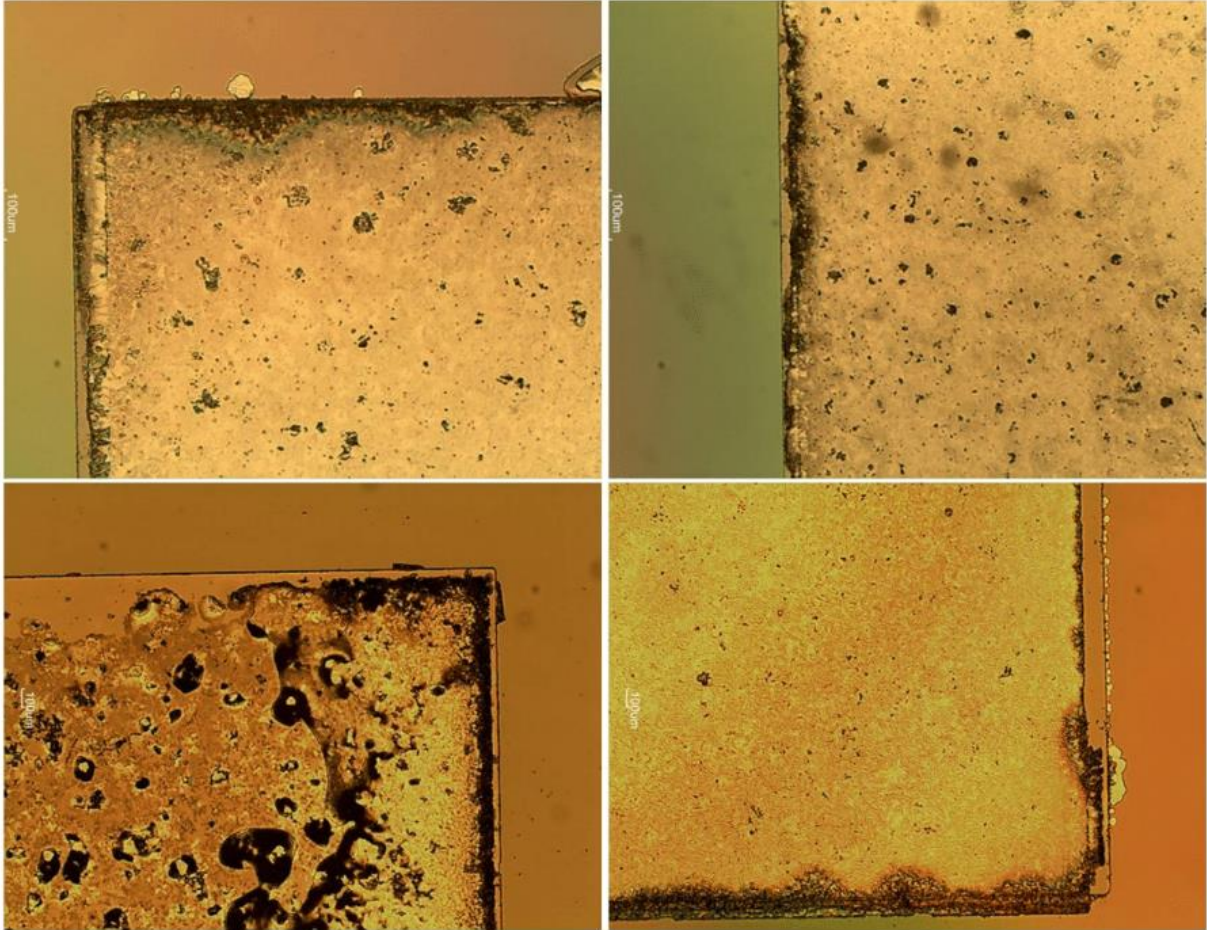
Fig. 11: Misalignment to restrict overflow

Careful observation of the bond edges showed that the misaligned part appeared dark reddish brown under the microscope, which is an indicator for Sn oxidation at the edge of the bonds. It was postulated that, the misaligned part being at the edge of the bond, has much less temperature than the center of the bond, because of which the Sn turns into soft semi-solid state instead of liquid as it does in the center, and acts as a stopping layer for the bond. Moreover, there is ample supply of air at the edge which oxidizes the Sn and turns it into SnO. This acts as a sealant for the eutectic alloy, restricting it and forcing it flow within the bond site, thus restricting overflow. Following this observation in the 1 cm^2 samples, two 0.5 cm^2 samples were intentionally misaligned, and no overflow was observed in them. Although, this requires further investigation, this could be a possibly cheap and fast way to restrict overflow by making one bond site slightly larger than the other. If this method is successful could deal

away with time consuming and expensive steps for fabrication of dams, trenches or stopping layers to restrict overflow. We achieved a success rate of 87.5% (7 of our 8 misaligned samples showed no overflow), which indicates that this is not the result of sheer luck.

Qualitative Results

An added advantage of having a transparent top layer is the ability to view the bond uniformity and macrostructure. The following sections will discuss, somewhat qualitatively, about some of the macrostructures observed within the bonded region. It should be noted that these comments are merely conjectures based on available knowledge and should not be taken for an absolute fact. To establish their validity, detailed studies must be performed on all of these individually.

- *Bond Macrostructure*

Fig. 12 shows the Au-Sn phase diagram. The eutectic reaction which forms the bond occurs when at a specific composition (20% wt. of Sn or 29 at. % of Sn), the binary phase is cooled from a temperature higher than the temperature at the eutectic point, forming a mixture of two different solid phases, zeta (Au_5Sn) and delta ($AuSn$).

The transformation of liquid phases into solid generally takes place by formation of dendrites. In a liquid melt (unary or having multiple components) undergoing supercooling at a temperature lower than its freezing point, there exist nucleation sites which are sites with locally higher cooling rate, voids, impurities, deformities or other interfaces, where spherical balls of solid originate and gradually start growing. Shortly after, owing to solid-liquid surface energy anisotropy and different crystallographic orientations, the spherical shape becomes perturbed and the growing solid front splits into several branches and forms dendrites.[9] (fig. 13, 14)

We can also infer information about the cooling rate of the metal and subsequently it's mechanical properties from the size and spacing between dendrites observed in the final structure. A lower undercooling rate leads to dendrites forming up to larger distance and often interfering with other growing dendrites forming grain boundaries and large sized grains.
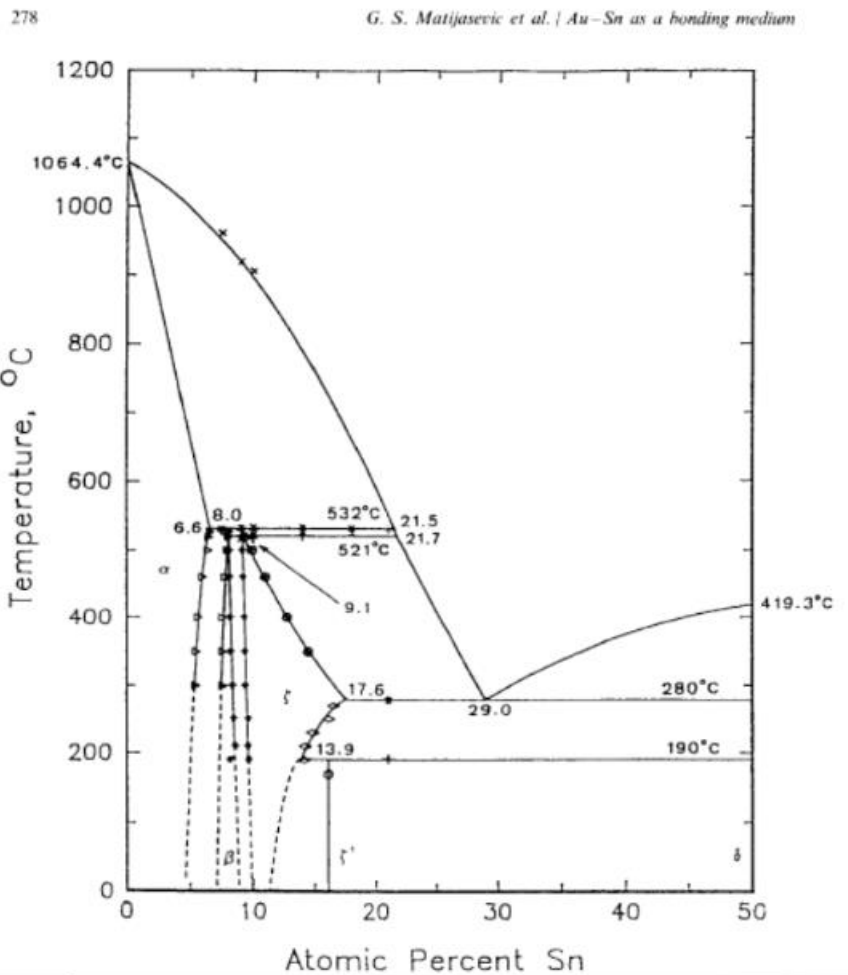
G. S. Matijasevic et al. / Au–Sn as a bonding medium

Fig. 12: Au-Sn phase diagram

However, a rapid undercooling rate is analogous to quenching a hot metal piece in cold water. In this case, the liquid phase is being forced to cool much faster and the dendrites do not have sufficient to grow, thus forming smaller grain sizes.[9] Larger grain-sized metals display much higher strength while smaller grain sizes are ductile.

Fig. 14 shows a very sparse distribution of dendrites within the eutectic matrix along with several sites of needle formation (early stages of dendrite formation), which suggests a high undercooling rate or insufficient temperature within the bond which restricts proper formation and growth of dendrites.

Additionally, other kinds of macrostructures are observed in some of the samples which are a little harder to understand and analyze. (see fig. 15, 16)
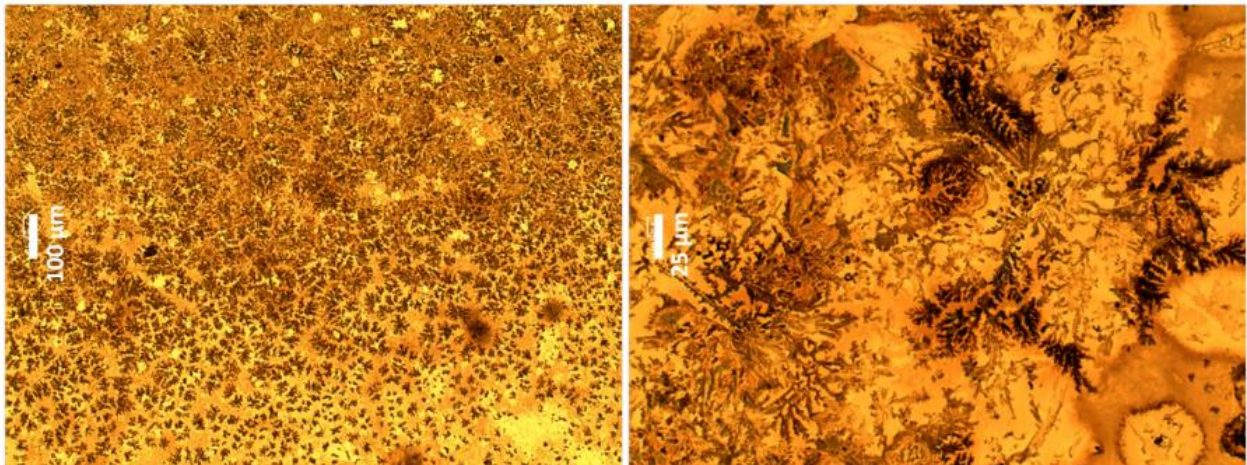
(a) Initial dendrite formation   (b) Merging of dendrites

Fig. 13: Bond macrostructure showing dendrites
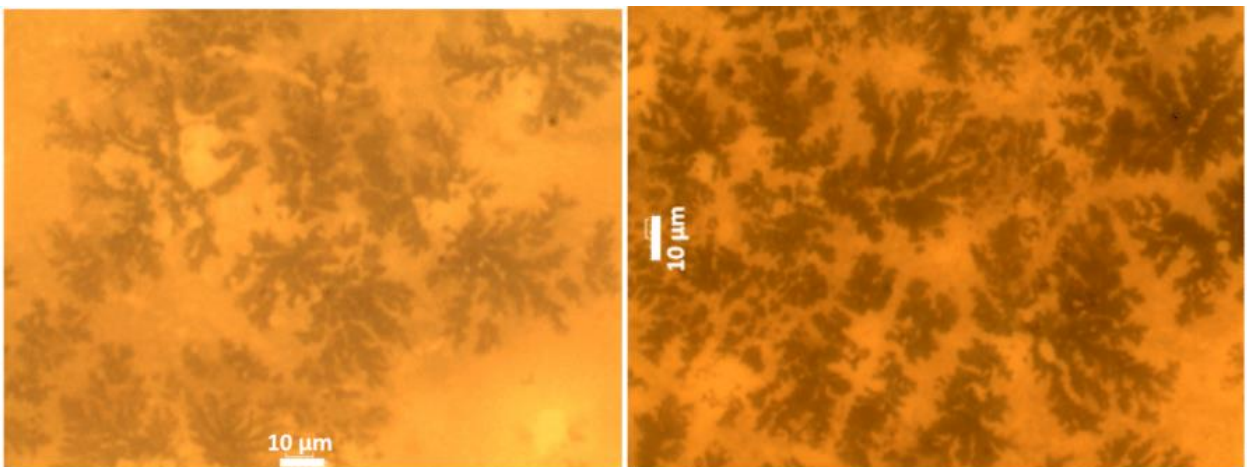
(a) Sparse Dendrites   (b) Closely spaced Dendrites

Fig. 14: Dendrite arm spacing as a result of different cooling rates

There might be two different explanations for these structures –

- o Temperature non-uniformity - Since our top substrate is pyrex, a very low conductivity material, the temperature gradient (non-uniformity) is pretty significant in this layer. The chip size used is 1.5 cm x 1.5 cm while the size of the CCH holder is slightly lesser than 1 cm^2. This gives rise to sudden drop in temperature in the chip area not in direct contact with the holder.

This problem might give rise to drastically different cooling rates in various parts of the bond area and thus form different stages of dendritic growth (early stage of needle formation to late stage of interfering dendrites)

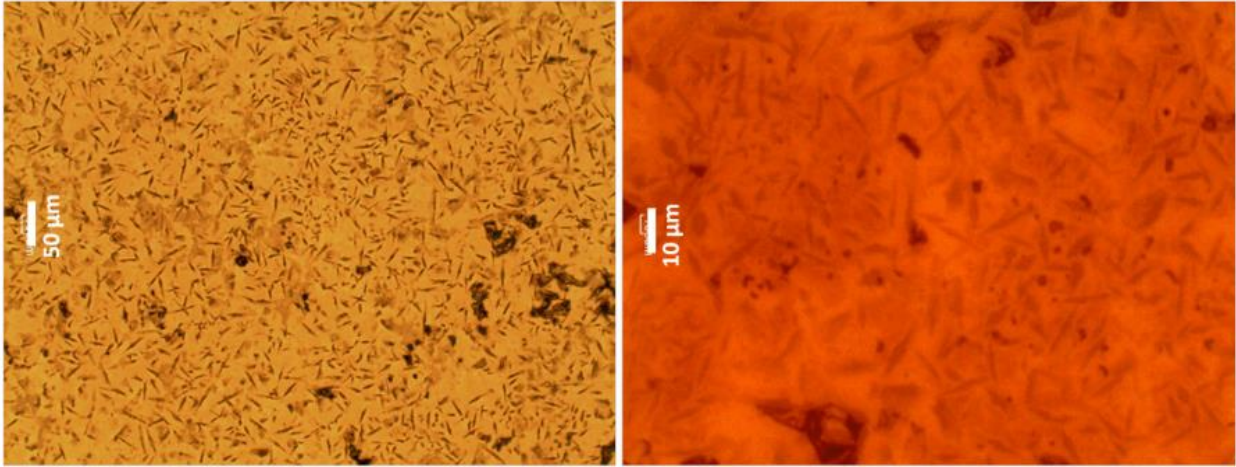This prediction matches several previous studies where an initial needle like protrusion has

Fig. 15: Bond macrostructure showing needles

been observed to develop branches and turn into a dendrite[13] (see fig. 15)

o Formation of chemically different compounds - The different macrostructure could also correspond to intermetallics formed during the eutectic reaction. Fig. 16 clearly indicates formation of yellow gold rich compound between areas of reddish brown Sn rich species. Interdiffusion studies have indicated that there are situations where pure $AuSn$ is formed at bond interfaces alongside the eutectic alloy, thus supporting this claim.[8]
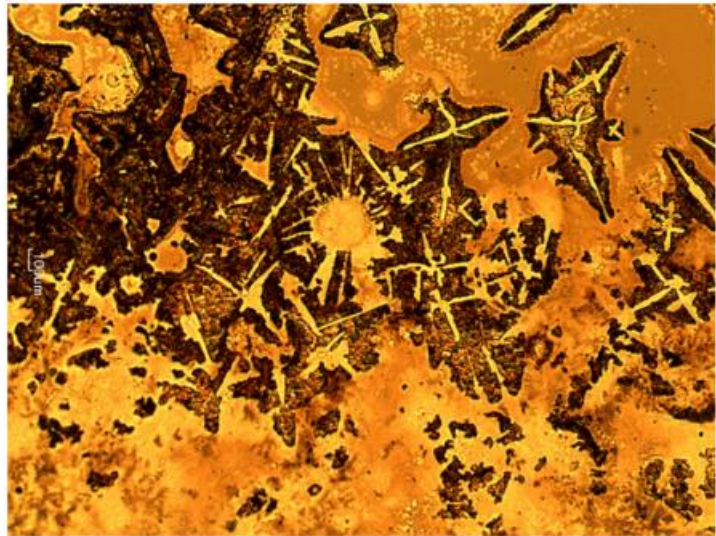
There could also be the chance of

Fig. 16: Bond macrostructure showing intermetallics

localized high concentration of one of the species coupled with localized temperature and pressure peaks, that could lead to formation of slightly Au rich or Sn rich phases which could have a different different structure and growth mechanism than that of the eutectic alloy. Matijasevic et al. [8] reported formation of other intermetallics like $AuSn_4$, $AuSn_2$ and Au_4Sn during the eutectic bonding between Au-Sn at later stages of interdiffusion, thus supporting this claim.

- *Kirkendall Voids*

Kirkendall effect is the result of movement of the interface between two metals during diffusion or such eutectic bonding situations because of drastically different diffusion rates of the metals into each other. Matijasevic et al. observed that the rate of Au diffusion in Sn is almost 4 times that of Sn in Au. In such situations, bulk motion of one type of atom predominantly from one side to the other leaves voids one side. At the bond metal interface this phenomenon produces microscopic holes. At the interface of a different substance (pyrex in our case), these voids accumulate and act as extra sinks for vacancies to migrate into. This causes proliferated void accumulation and stands out distinctly when viewed through
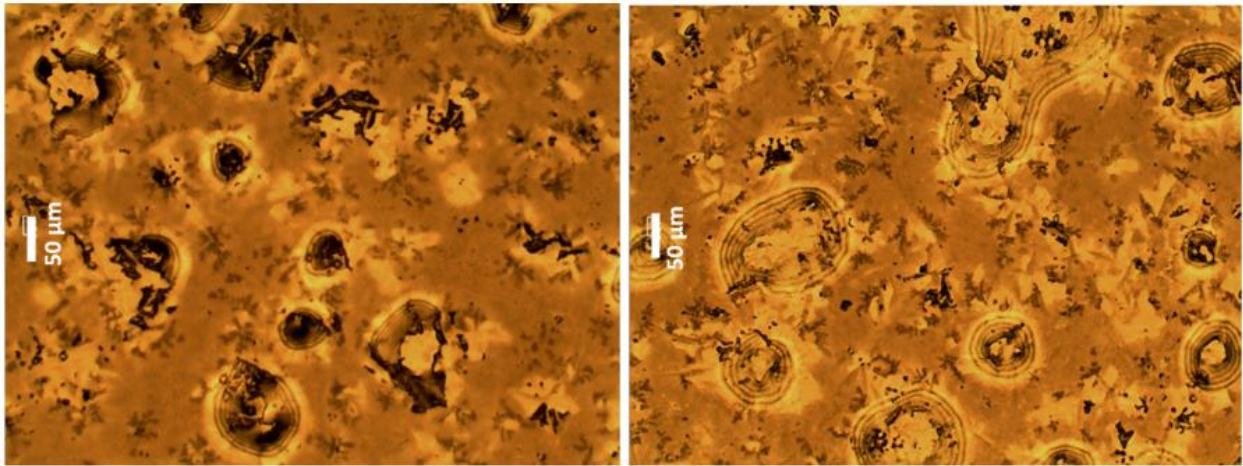

Fig. 17: Kirkendall voids and interference fringes around them

a microscope. Nakahara and McCoy[14] studied Kirkendall voids extensively while investigating several bonding recipes.

In one our samples, which had been bonded at a T_bond value of 320 ^oC with a force of slightly over 100 N, we observed the formation of voids within the macrostructure. The voids were clearly visible through an optical microscope at a magnification of 20x. Several interference fringes formed around the voids which can be used to quantify the depth of the voids and get an estimate for the volume of these voids. Capturing a wide area of the bond, we can also estimate the volume fraction and density of these voids. The sample subsequently was broken during handling, which proves that visible detection of Kirkendall voids through an optical microscope is a sign of weak bonding. Thus, additionally, observation of Kirkendall voids may be classified as an intermediary case between successful formation of eutectic bonding and no bond formation. Although formation of these voids is pretty common and inevitable in eutectic bonding, when we observe the bonding parameters under which these voids were formed, we can infer about the limiting scenario which marks the boundaries between good and weak bond qualities.

Another possible explanation for the formation of these voids may be the presence of intermetallic constituents within the bond. When temperature is comparatively lower (320 ^oC) and the cooling rate pretty high, then it might be possible that Au-Sn diffusion does not take place to a full extent. In such situations of incomplete diffusion, it is not uncommon to observe local high concentrations of Au or Sn. The eutectic alloy comprising of the zeta and the delta phase can undergo a congruent reaction around a temperature of 190 ^oC, where the zeta phase breaks down into $zeta'$ and $AuSn$ phase. This

reaction which is accompanied by a volume contraction can be attributed to as one of the reasons for formation of such voids.

- *Tin Oxidation at the edges*

Another issue plaguing bonding process in the flip chip bonder is the lack of inert atmosphere. The edges of the bond which are under significant pressure due to uneven CCH holder module are also the areas which gets supplied with the most amount of heat during the bonding process because of good thermal contact due to high pressure. These areas, being close to the edge of the chip has access to air and Sn can get easily oxidized at high temperature to form SnO which appears brownish black in all the images and are noticed only at portions of edges of some samples (fig. 18) SnO causes the bond to become brittle and ineffective and thus should ideally be avoided during the bond formation process.
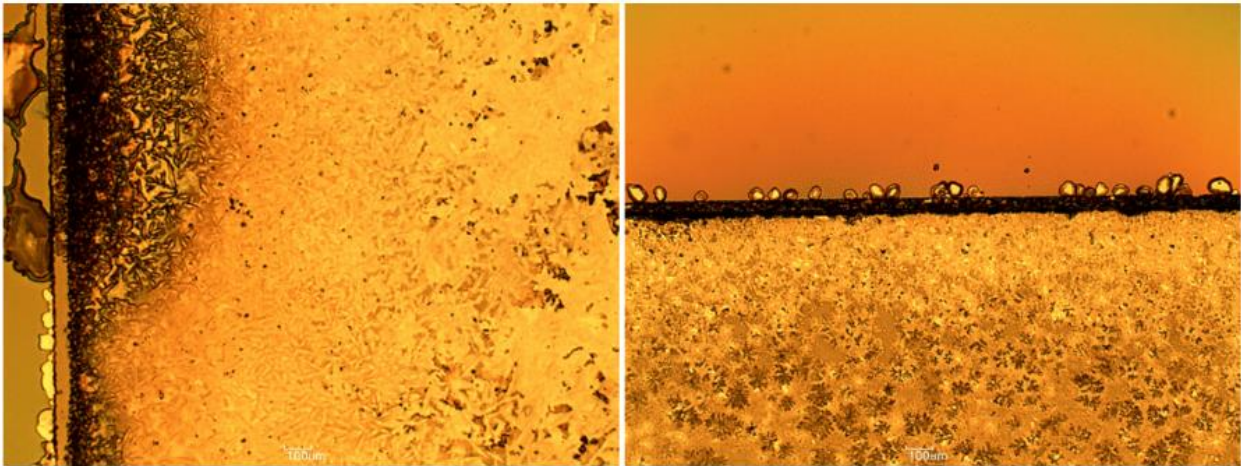

Fig. 18: Oxidized Sn at the edges of the bond

Conclusion and Suggestions

The optimized results to achieve the best bond quality for least bond area and minimize the overflow of Au-Sn eutectic bonding are as follows –

- o The temperature of Au-Sn eutectic bonding should be greater than 330 ^oC
- o Pressure uniformity is extremely crucial. Though we could not deduce any discernable success trends for pressure variation for this project, what we did observe that is as long as the pressure applied is uniform and is above 0.5MPa, a good quality bond is formed.
- o The Finetech Lambda Flip-Chip Bonder is not the best option to bond samples with bonding area more than 6 mm x 6 mm. This is because of the fact that the maximum field of view of the camera the lowest magnification is 6 mm x 6 mm. To mitigate this issue, one can pattern alignment marks within the bond site.

We provide a few more suggestions to mitigate the non-uniformity issue of the flip-chip bonder machine. This is a way of fixing the tilting issue and ensuring that the two samples are perfectly flat when they contact each other. This can be done by performing a set of trial experiments by taking one pyrex and one silicon wafer while varying the z-position of the bottom substrate plate. The interference

rings formed would give us information about the uniformity. We can then record the z-position of the substrate plate for which best uniformity is observed and use it for the subsequent bonding experiments.

Future Scope

We have garnered ample qualitative information by observing the macrostructure of the Au-Sn eutectic bonding through an optical microscope. Quantifying these results by performing metallographic tests and doing EDS or XRD spectroscopic analysis would be a great next step. We observed sparse and closely spaced dendrites in the macrostructures. The dendrite length and the spacing have a direct correlation with the cooling rate. Following this, the effect of cooling rate on bond uniformity and strength could be studied.

Kirdenkall voids were another very interesting qualitative observation of our study. We can use interferometry to detect voids formed at the interface of the pyrex chips without breaking it open. Several interference fringes formed around the voids can be used to quantify the depth of the voids and get an estimate for the volume of these voids. Capturing a wide area of the bond, we can also estimate the volume fraction and density of these voids. The samples that show these voids mark the boundary between successful and unsuccessful bonding trials.

A serendipitous finding of our study was that misalignment could be used to restrict the bond overflow. Surprisingly we achieved a success rate of 87.5% (7/8 samples). This is an extremely interesting area of future studies as it could prevent time consuming, complicated and expensive lithographic steps that would be involved in making stoppers, trenches or grooves to restrict bond overflow.

Fig. 19: Nanofoil
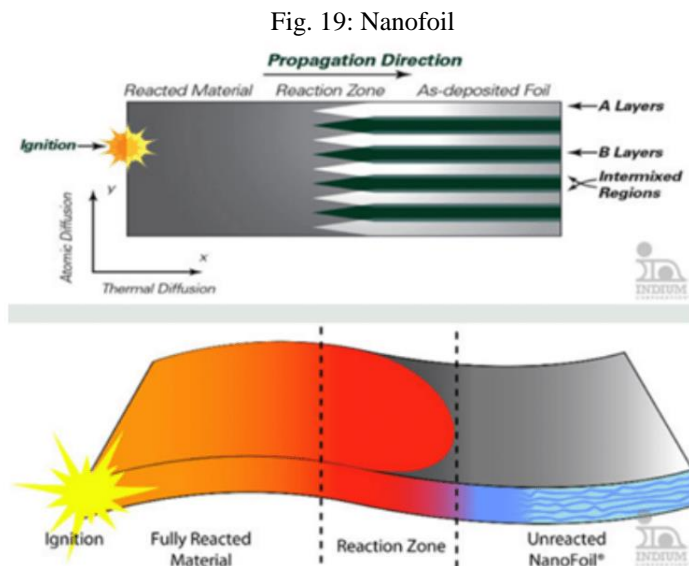
The electronic industry is averse to the idea of heating up individual chips to facilitate bonding because of presence on sensitive components within the chips. An area of interest for future is use of localized heating using electrical source and patterned lines for eutectic bonding instead of heating the substrate plate and the CCH Module (top holder plate) in the flip-chip bonder. One potential method is by using Nanofoil[15] which is a reactive multi-layer that provides instantaneous heat for a variety of applications. Nanofoil is a predictable, controllable and affordable material that is industry accepted and proven to lower manufacturing costs while providing repeatable and reliable bonds and reaction. This reactive multi-layer foil is fabricated by vapor-depositing thousands of alternating nanoscale layers of Aluminum (Al) and Nickel (Ni). When activated by a small pulse of local energy from electrical, optical or thermal sources, the foil reacts exothermically to precisely deliver localized heat up to temperatures of 1500 ^oC in fractions (thousandths) of a second. Travelling approximately eight meters per second, the reaction's rapid delivery coupled with its localized and versatile nature makes it ideal for many types of bonding and reaction initiation (energetics) applications.

Acknowledgements

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