Superconducting Parallel Plate Capacitors with High Kinetic Inductance

E241 Fall-Quarter Report

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Introduction

Project Motivation

Parallel plate capacitors can potentially achieve high capacitance values, while shouldn't introduce unwanted parasitic self-resonances. In addition, introducing kinetic inductance allows nonlinear processes to occur. Combining these three virtues, on-chip parallel plate capacitors open a way to fabricate high-efficiency nonlinear devices for frequency conversion and signal amplification in microwave and millimeter-wave regime. Two applications are especially tempting - microwave to mm-wave transduction for establishing quantum networks and Josephson parametric amplification of microwave signals.

Building of Quantum Networks can be a milestone in the development of quantum computers as it would allow to distribute entanglement between quantum machines and run computing tasks on scattered devices. We proposed[1] a kinetic-inductance-based converter of qubit microwave signals to mm-waves, which could be transmitted between two dilution refrigerators with almost no loss. Moreover, this transducer could facilitate conversion to even higher, optical frequencies when integrated with non-centro symmetric crystal platforms like lithium niobate[2]. We already achieved coupling of mm-waves to a superconducting device[3] and for the next stage of the project, we need to introduce a 5 GHz resonance that requires a large capacitance, that can be achieved with parallel-plate capacitors.

Josephson parametric amplifiers (JPAs) have become a crucial component of superconducting qubit measurement circuitry, enabling recent studies of quantum jumps, generation, and detection of the squeezed microwave field, quantum feedback, real-time tracking of qubit state evolution and quantum error detection[4]. We plan to make an on-chip JPA and for our circuit parameters, it requires non-planar superconducting capacitors to avoid parasitic resonances in the circuit.

Benefits to the SNF Community

We propose the fabrication of a parallel-plate capacitor analogous to the process in the study of K. Cicak et al.[4] for aluminum structures. In our case we want to fabricate devices of niobium on Sapphire, Nb has a higher transition temperature and kinetic inductance than Al. Sapphire substrate potentially allows to integrate superconducting circuits with optical platforms, like lithium niobate and work in the infrared regime with low loss. First, we plan to develop a process to fabricate a capacitor with a dielectric layer (SiO_2), then we would like to work out a way to remove the dielectric (or another sacrificial layer) and fabricate vacuum-gap capacitors to achieve lower loss resonators.

Deliverables:

Done in the Fall Quarter:

- ✓ Characterization of selective Nb etching in CF_4 plasma – 3 parameters DOE
- ✓ Characterization of selective SiO_2 etching in CF_4:CHF_3 plasma – 3 parameters DOE
- ✓ Characterization of lesker-sputterer in the context of Nb Deposition
- ✓ Evaporation of good-quality Niobium films

Planned for the Winter Quarter:

- Process flow for vapor HF etching of SiO_2 and releasing Nb structures:
  - Air Bridges for Spiral Inductors
  - Parallel Plate Capacitors
- Process for creating vias to galvanically connect two planes
- Comparison of the new Lesker Sputter system with the old one

All of the process components that we develop during the class will allow other SNF users fabricate complex niobium/oxide structures like, for instance, non-planar resonators[4], electro-optic modulators[2], microwave to millimeter-wave frequency transducers[1] or MEMS devices.

Superconductivity

Superconductivity is an attribute of materials where the resistance vanishes and magnetic fields are repelled. Any material that shows these electrical properties is called a superconductor. Conventional superconductivity can be understood by Bardeen-Cooper-Schrieffer theory or BCS theory[6]. The theory describes superconductivity as a microscopic phenomenon caused by the formation of an electron-electron bound state called a Cooper-pair.

To see how the formation of Cooper-pairs is related to superconductivity, we will follow a classically-motivated approach[7,8]. For normal conductors, the resistance to electrical currents can be seen microscopically as the scattering of the electrons off of the conductor's crystal-lattice. In other words, the lattice-vibrations have a direct influence on the resistance. As we cool down the conductor, we find that the low-thermal-energy-environment causes the lattice vibrations become dampened and decreases the probability of electrons to scatter off of the lattice. Hence, the resistance decreases.

For superconducting materials when the temperatures are low enough, the electrons that are moving will attract positive charges within the lattice. This deformation of the lattice causes another electron, with opposite spin, to move into the region of higher positive charge density. The two electrons now become correlated i.e. form a Cooper-pair with total spin either 0 or 1. Since there are many such pairs in superconductors and have bosonic spin properties, they can collect and form a condensate. In this condensed state, the energy required to break a single Cooper-pair bond is related to the energy to break the bonds of all the Cooper-pairs. Thus,

when the condensate is travelling through the superconductor it remains undisturbed by the lattice because the vibrations do not have enough energy to impact the state of a single Cooper-pair and so all of the electrons flow without any resistance.

Superconducting Parallel Plate Capacitors

Superconducting devices are electronic devices that utilize the zero-resistance properties of superconductors. In general, these devices are used for highly sensitive, low-loss electrical systems. We are interested in on-chip low-loss microwave electronics wherein quantum systems are developed. In addition to low-loss components, we also care about microwave components that can be treated as lumped-elements.

Often, coplanar waveguides (CPWs) are used as transmission lines or resonators when paired with interdigitated capacitors (IDCs)[9]. However, for our purposes fabricating resonators with CPWs and IDCs require footprints spanning millimeters. With large footprints these components suffer from non ideal, distributed characteristics such as parasitic inductances and capacitances resulting in unwanted resonant modes[10]. With parallel-plate capacitors, we are provided access to large capacitances while suppressing the nonidealities we observe with IDCs.

In addition to fabricating lumped-element resonators, we are concerned with intrinsic loss-mechanisms within the materials. The main loss mechanisms for quantum systems that we are interested in are due to unsaturated two-level system (TLS) defects found in amorphous dielectric materials[10,11]. For LC resonators with dielectric-filled parallel-plate capacitors, it has been shown that energy is lost to a TLS-bath[10]. Therefore, we would like to develop vacuum-gap capacitors (see Figure 1 below), releasing the dielectric from between the capacitors on a Niobium-Sapphire platform, instead of a Aluminum-Sapphire platform shown in previous work[5].

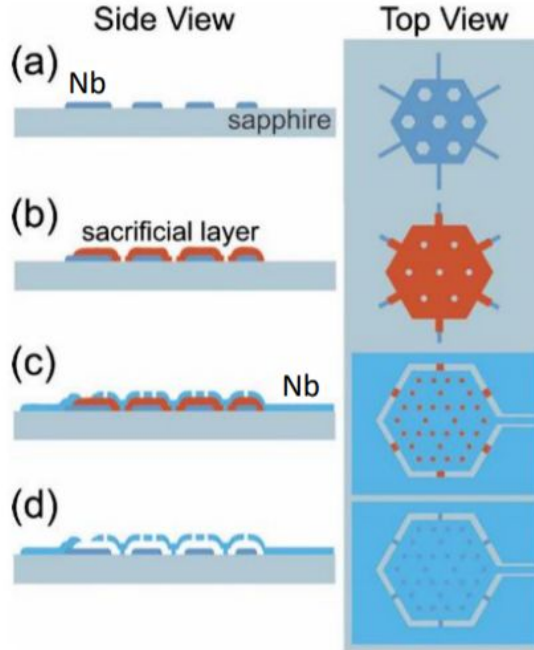


Figure 1: This figure shows the proposed parallel plate capacitor processing flow. Modified from Kicak et al.[5]

Kinetic Inductance

Our decision to use Niobium as our metal-film for this project comes from the fact that it has a high kinetic inductance. Kinetic inductance is naturally described by the Drude model of electrical conduction[13]. The Drude model is an application of kinetic theory and assumes that the microscopic behaviour of electrons in a solid may be treated classically (as we did when discussing superconductivity). The model considers DC conductivity and the time-to-collision, τ, of mobile charge carriers:

$$\sigma(\omega) = \frac{ne^2\tau}{m^*(1+\omega^2\tau^2)} - i\,\frac{ne^2\omega\tau^2}{m^*(1+\omega^2\tau^2)} = \sigma_1 - i\,\sigma_2$$

Here m^* is the effective mass of the charge carrier. In our case, the charge carriers are electrons. The imaginary component of the complex conductance, $-\sigma_2$ represents the kinetic inductance. For superconductors, the time-to-collision $\tau \to \infty$ and we find that in the limit the term that represents kinetic inductance remains. This model also shows that even though dc resistance vanishes for superconductors, there is still a non-zero ac-impedance observed[14].

Intuitively, kinetic inductance comes from the inertial mass of the electrons in alternating electric fields. Since electrons (or other charge carriers) have finite mass, they tend to travel at a constant velocity, once accelerated. Therefore, it takes a finite amount of time for the electrons to gain speed, when acted upon by the changing electric field. Thus, resulting in a phase lag with respect to the varying electric fields (voltage). This is identical to the phase lag experienced

by geometrical inductors when they are exposed to a change in voltage which is opposed by a change in magnetic flux. In one case the energy is stored in the kinetic energy of the electrons (where the name comes from) and in the other case the energy is stored in the magnetic field. Since they have the same phase lag characteristics, both of these energy storage mechanisms are seen as inductances $L = L_0 + L_K$.

Fabrication Process Development

Niobium Deposition

This section will focus on the portion of the project related to Niobium deposition. We will discuss the requirements of the Niobium films, deposition capabilities of SNF, results and operating procedure of the Kurt J. Lesker Magnetron Sputtering system in the exFab, and the characterization of the deposited films.

Tool Selection for Deposition in SNF

There are a variety of deposition systems in SNF that are capable of depositing Niobium films. Through discussions with SNF mentors, we decided on using the Kurt J. Lesker Magnetron Sputtering system. There were two main reasons in selecting sputtering as our deposition tool:

1. Literature review showed desirable electrical properties for sputtered films (next section).
2. Compared to ALD (Fiji-1) , and e-beam evaporation (AJA evaporator), the KJL sputtering system provides access to many more process parameters - increasing the probability of a successful deposition (see Table below).

KJL Sputtering System	**Fiji1 ALD**	**AJA Evaporator**
RF/DC Power (W)	Chamber Temperature (C)	Final Thickness (nm)
Pressure (mTorr)	Pressure (mTorr)	Beam Current (mA)
Gas Flow rate (sccm)	Precursor Temperature (C)	
Substrate Temperature (C)	Deposition Time (s)	
Substrate Bias (V)		
Deposition Time (s)		

Table shows the process parameters that can be controlled by the user for the KJL sputtering system, Fiji1 ALD system, and the AJA evaporator. Because of the volume of the parameter space we can explore with the sputtering system, it makes it an enticing tool to use.

The final consideration was that we believed that this was an opportunity to provide SNF with a comparison of sputtering capability as a function of usage. The KJL sputtering system is one of the most heavily used tools in SNF/exFab. The popularity of this tool makes it so that it needs to be vented and pumped down every weekday. There is good reason to be concerned about this as the system's rated base pressure is rarely reached. Another point of concern is the variety of materials that are allowed in the exFab KJL. Because of the system's versatility in material deposition and there is a suspected tradeoff with film quality. Because of this usage, another KJL sputtering system was purchased, to be placed in the clean room within the category of Semi-Clean-B. The plan was to use the exFab KJL and attempt to obtain some results, and then compare the same process with the new KJL in the cleanroom in order to compare how much the daily-venting impacts film quality.

In this report, we discuss the results of the exFab KJL Sputtering system. Looking forward we hope to characterize the new sputtering system so that we can provide some compelling evidence for the suspected versatility-quality trade-off.

Literature Review and Figures of Merit

To help us understand which process parameters will be important for producing acceptable quality films, we searched the literature. Since we would like to make superconducting devices with the Niobium metallization our primary goal is to produce films that have the superconducting transition temperature near the bulk value of 9.3 K. Jin et. al.[15], Bose et. al.[16], show that grain size of the Nb films strongly correlates with T_c suppression. The larger the grain size, the closer T_c is to bulk, even for thick films (500 nm) as shown by Bose et. al.[16]. Thus, the deposition rate becomes important. Furthermore, other studies[17,18] show that substrate bias and substrate temperature may also play a role in engineering T_c.

From this review, and discussions with mentors we decided on using RF sputtering and focusing on four process parameters: pressure, flow rate, substrate temperature, and substrate bias. Additionally, to characterize the films, we have identified four figures of merit: grain size, room temperature (RT) resistivity (or residual resistivity ratio), film stress, and T_c.

Niobium Sputtering Standard Operating Procedure

While the standard operating procedure of the KJL sputtering system is well-documented for wafers, it is worth discussing the case for working with pieces. Furthermore, we also include chamber conditioning steps so that the deposition environment is approximately the same across all of the depositions. This SOP is summarized as a runsheet in the "Runsheets" section below.

1. At a solvent bench, clean your pieces with an acetone rinse, followed by an ipa rinse - 30 seconds each, then N2 blow dry. Necessary to keep substrate surface clean for deposition.

2. At the KJL, turn on the two fans and wait until blue light turns on to work with your sample in the area. These fans create an environment with a low amount of air particulates.

3. While waiting for the fan, enable the tool in badger (lesker-sputter, found under nSiL tab).

4. Run a Ti deposition: 200 W DC, 50 sccm Ar, 3 mTorr, 15 minutes. Note: during the “burn-in” step you need to slowly increase the pressure manually until the plasma strikes. If plasma does not strike you can “Pause” the recipe and “Resume” when the plasma is lit.

5. Run a Nb deposition: 100 W RF, 50 sccm Ar, 3 mTorr, 15 minutes. Note: Nb is tricky to strike. Best way is to increase pressure to ~25 mTorr, and quickly open and close the shutter. Once the Nb plasma is lit, reduce back to 3 mTorr.

6. Select a suitable platten/carrier chuck so that you can mount your chip. Before you begin mounting Run LL Vent from the touch screen of the KJL’s computer. Venting should take around 5 minutes (the process screen will show a green-bar to indicate the recipe is finished).

7. Begin mounting your sample. The mounting procedure varies whether you want to do a low-temperature deposition or a high temperature deposition (see High Temperature Mounting section). Make sure the piece is secure (do a shake test) because it will be loaded upside-down.

8. Use the N2 gun to blow away any particulates.

9. Load the platten in the LL and **align the notch on the wafer carrier to the notch in the LL**.

10. Pump the LL using the “LL Pump” recipe on the touchscreen. Wait for recipe-end confirmation.

11. Run “Sample Load” recipe and wait for recipe-end confirmation. This recipe transfers your sample from the LL to the process chamber.

12. Log the chamber pressure.

13. Run the desired deposition recipe. Make sure to use the “No DC Bias downstream control” recipe for your particular gun.
    a. **If you want substrate bias:** Apply substrate bias before recipe start, using the touch screen. Note: if the power setpoint and ramp are not zero, the power supply will not turn on - make sure to zero those before turning on.
    b. **If you want to do a high temperature deposition**: Turn on substrate heater before recipe start. If the measured temperature values do not change and you have followed the instructions in the “Heating” tab, make sure the PID controller has a setting file loaded. Use **PC MFC Default 2**.

14. Once the recipe ends, the heater and the substrate bias power **will automatically turn off**.

15. Run “Sample Unload” recipe and wait for recipe-end. If you have done a high temperature deposition, the sample needs to sit in the LL for ~ 20 minutes to cool down. The chamber takes longer to cool down. **You cannot disable the tool until the chamber has reached room temperature**.

16. Run “LL Vent” recipe and wait for recipe end. If you have done a high-temperature deposition, **be careful as the platten/carrier chuck may still be hot**.

17. Once the platten/carrier chuck is cool enough to handle you can remove it and place on an aluminum block so that it cools off quicker.

18. Run “LL Pump” recipe and wait for recipe-end.

19. Take a picture, and unmount your sample.

20. Clean up the working area, turn off the fans, and put the platten/carrier chuck back.

21. Disable the tool.

22. Take your sample to Prometrix and use the standard single-point measurement. Make sure you choose the correct probe tip for Nb. Note: alignment here is tricky because the Prometrix expects wafers. Additionally, the tool does a test measurement and moves ~ 0.5 mm down the chip. If the alignment is wrong, the probe tip will miss the metal and you will get an error. Log the results.

23. Measure the step-height using a profilometer. Either AlphaStep or Dektak will work. Make sure the expected thickness is greater than 30 nm - this is generally the limit for these tools.

High Temperature Deposition Mounting

When doing a low temperature deposition, using Kapton tape is sufficient to obtain a step height. However, at high temperatures (400-600 C), Kapton tape will melt. Instead we use a another piece of (cleaned) sapphire and place the polished side down. We mount on top of this extra piece. The picture below depicts the proper mounting procedure. Note, it is best to align the mounting clip in the direction of the masking-sapphire piece. This is to reduce the non-ideal shadowing caused by the clip.

Figure 2. Shows mounting procedure for high temperature depositions

Experimental Results

For the first quarter, we focused on determining the deposition rate of the KJL sputtering tool and the resistivity of the Niobium film. We decided on focusing on only the resistivity because of two main reasons: (1) resistivity correlates well with T_c [19,20] (2) it is easy to measure with the Prometrix OmniMap Model RS35e. Both the deposition rate and the resistivity require the film thickness, which is given by a step height measurement. The step height measurement was conducted using the Dektak Stylus profilometer in the SNC (see Figure 3).

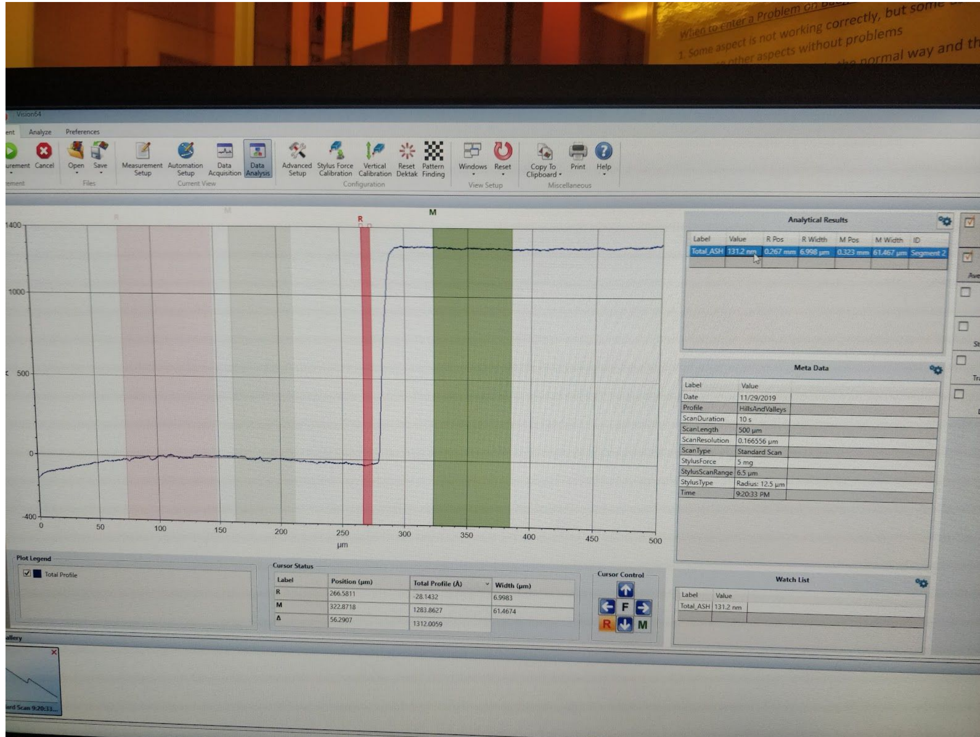


Figure 3: Example of Dektak measurement

One huge experimental limitation that we determined before doing any deposition was that our Niobium target is a bonded target. Bonded targets have the bulk material bonded by Indium to a Copper adaptor. The issue with bonded targets for our purposes is that it limits the RF power. The RF power is directly correlated with the deposition rate[17,20], a process parameter we care about. Therefore, the RF power for us was a fixed parameter at the maximum allowed by the bonded target.

We conducted three separate sets of experimentation, each one was motivated by the previous. The first round served as an exploratory deposition to see where in the process-space we are at and how we should adjust. The second round looked at substrate temperature and substrate bias, keeping Argon flow and pressure constant. Lastly, the third set was Niobium deposition via a Plassys Evaporator owned by the Safavi-Naeini group. The reason that a DOE was not developed for this portion because we would first like to determine the proper location in the parameter-space to design the DOE at. As shown by the results below, it is unlikely that the KJL sputtering system in the exFab can produce films that are acceptable for the next portion of our project.

The target resistivity range is 15.2(bulk)-20 uOhm-cm[19,20]. This range was determined by a combination of literature and measurement. We measured a vendor-supplied Niobium films using the prometrix and the resistivity 17 uOhm-cm.

Set 1: November 2, 2019

The RF power was set to 100 W, deposition time was 4706 s (80 minutes) and there was no heating of the substrate. The chamber pressure was at P = 5.7e-7 Torr when we started these depositions.

Chip name	Substrate Bias (V)	Argon Flow (sccm)	Argon Pressure (mTorr)	Measured thickness (nm)	Rate (nm/min)	Sheet Resistance (Ohm/sq)	Resistivity (uOhm-cm)
NbSa01	0	100	25	72.37	0.92	583	4219
NbSa02	**90**	**100**	**3**	**65.18**	**0.83**	**25.36**	**165**
NbSa03	90	50	25	44.95	0.5	53.9	242

We see a drastic change in resistivity by introducing a substrate bias. NbSa01 is also a different colour than the other two samples (see Figure 4). The second row is bolded because it is the optimal sample of this set. The SEM (Figure 5) of NbSa01 shows that the grains are exposed without any additional processing, with grain sizes being small[15,16]. We tried to SEM NbSa02, but the grains were not exposed without additional processing. From this set of experiments, we determined to keep the Argon flow and pressure constant and vary the substrate temperature and pressure, since we are a factor of 10 away from the desired resistivity.

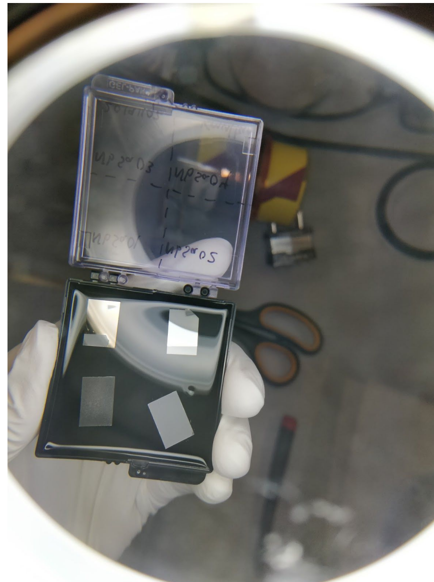


Figure 4: The top two samples are NbSa01, and NbSa02. Bottom two are non-metallized in this photo.

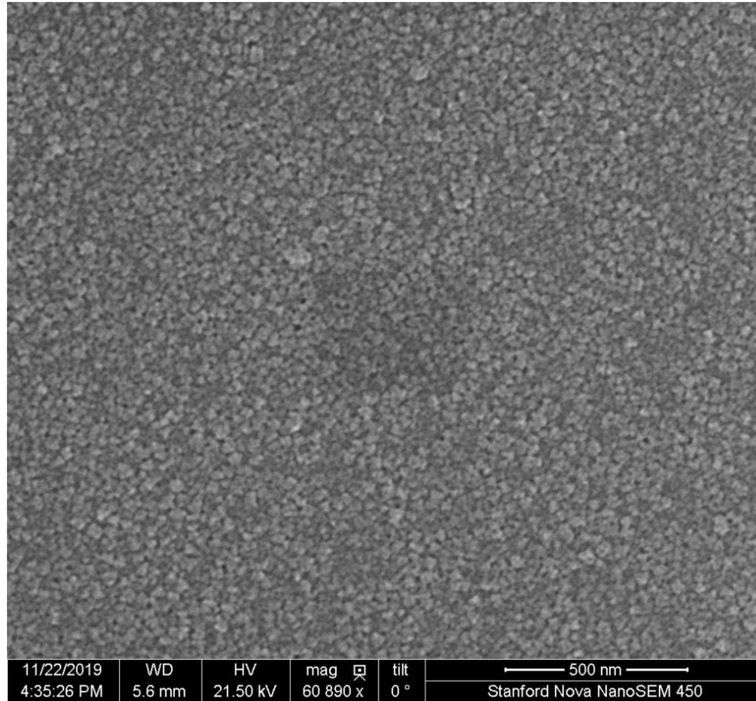


Figure 5: SEM of NbSa01 without any additional processing.

Set 2: November 17, 2019 & November 23-24, 2019

On November 17, we deposited Niobium on NbSa10, NbSa11, and NbSa12. On November 23-24 we conducted a repeat experiment of our best sample in order to test two things (1) does baking out the chamber help with the chamber pressure (2) the impact of low deposition rates.

The RF power was set to 100 W, Argon flow was set to 100 sccm, and the pressure was set to 3 mTorr.

Chip name	Substrate Temperature (C)	Substrate Bias (V)	Measured thickness (nm)	Dep. Time (s)	Rate (nm/min)	Sheet Resistance (Ohm/sq)	Resistivity (uOhm-cm)
NbSa10	**395**	**90**	**40.37**	**7200**	**0.34**	**14.7**	**59.3439**
NbSa11	395	0	44.21	7200	0.37	33.54	148.28034
NbSa12	20	175	49.7	4706	0.63	38.56	191.6432
NbSa10R	395	90	213.23	18000	0.71	7.5	159.9225

The chamber pressure before heating up the substrates for NbSa10-12 was around 5e-7 Torr, but the pressure spiked to 5e-5 Torr when the substrate reached 395 C, where the deposition occurred. NbSa10 is bolded because it is our best deposition from the lesker, which is a factor of 4 away from the target value. While this is an optimistic result, the deposition rate is too slow. We want a nominal thickness of 150 nm and at a rate of 0.34 nm/min we would require a ~7.3

hour deposition. The longer the sample stays in the chamber, the more impurities will form within the film[20]. For context, at P = 1e-6 Torr it takes ~ 2 seconds for a monolayer of impurity to form[21].

We repeated NbSa10 (shown in the row labelled NbSa10R), but we did a 60 minute bake of the chamber followed by an overnight pump. Also, we left the sample in the load lock during this time - the load lock had a pressure of 1e-7 mTorr. When we started NbSa10R's deposition, the chamber pressure was a factor of two better at 395 C, P = 5e-6 Torr. The deposition time was increased because we were expecting a deposition rate of 0.34 nm/min, but we found that the deposition rate increased by a factor of two as well. In the end, the sample was left in the chamber for too long and we observe a degradation of the resistivity compared to NbSa10.

Furthermore, it is important to note that increasing substrate bias doesn't necessarily improve the resistivity. Comparing NbSa12 and NbSa02, the process parameters were the same except NbSa12 had a higher substrate bias, but NbSa02 has a lower resistivity. This is important because it means our limiting factors are now chamber pressure and deposition time.

Set 3: November 29, 2019

In this set we used a Plassys E-beam evaporator, which is owned by the Safavi-Naeini lab. We used a standard Niobium deposition recipe. The chamber pressure while deposition was P = 2.4e-8 Torr, more than an order of magnitude better than the KJL sputtering system.

Chip name	Deposition Rate (nm/min)	Measured Thickness	Sheet Resistance (Ohm/sq)	Resistivity (uOhm-cm)
NbSaE01	**42**	**131.2**	**1.502**	**19.70624**
NbSaE02	42	131.56	1.564	20.575984

From the e-beam evaporation we observe that the resistivities lie within our target range. We suspect this is due to the factor of 60-140 increase in deposition rate and the factor of 10 reduction in chamber pressure.

Results Summary:

We summarize our results in this section. The constant KJL parameters are: Ar flow = 100 sccm, Pressure = 3 mTorr, RF Power = 100 W. In the table below, P_{ch} denotes the chamber pressure before deposition. Figure 6 shows the corresponding resistivities.

LESKER-DEP	A	B	C	D
Temp (C)	20	395	395	395
Bias (V)	90	0	90	90
P_{ch} (Torr)	5e-7	1.1e-5	2e-5	5.3e-6

Rate (nm/min)	0.83	0.36	0.33	0.71

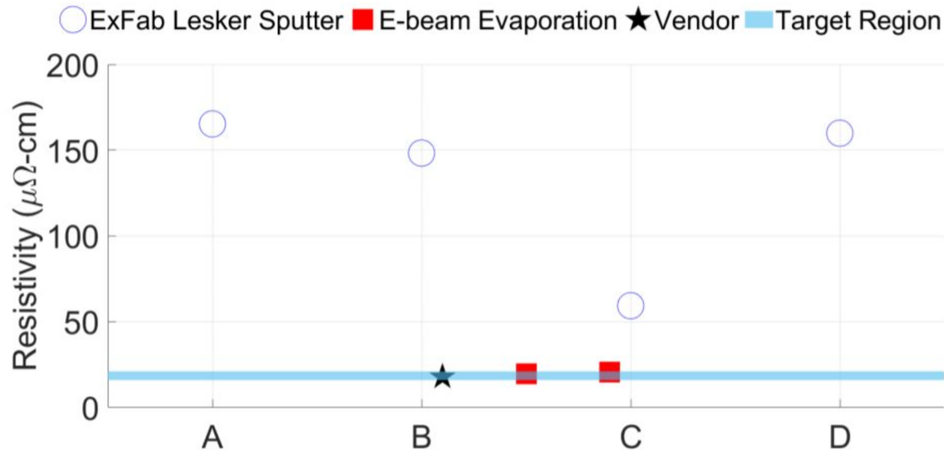


Figure 6: Resistivities summary plot. The x-axis corresponds to the experiment labels defined in the table above.

Silicon dioxide deposition and patterning

This section will focus on operating the PlasmaTherm Oxide Etcher, the entire procedure for selective etching of the silicon dioxide can be found in the attached runsheet, in “Runsheets” section.

Literature review

While reactive ion etching and deposition of the silicon oxide itself is well-understood and described in the literature, an analysis of etching selectivity with respect to niobium has not been studied so far. To gain intuitions about this it is possible to compare experimental etching results of the silicon dioxide[22] and niobium[23,24] that were conducted separately. This approach is not perfect, due to different etching systems and techniques applied but should be enough to choose good chemistry. Based on the work of Chen[23] and Sasserath[24], we can expect CF4/O2 plasma mixture to etch niobium, but the rate can be highly controlled by other process parameters. At the same time this mixture is known to etch the silicon dioxide with high rate[1]. All of the abovementioned processes utilize reactive ion etching with capacitively coupled plasma, hence, we cannot directly use the parameters like power or pressure but we can estimate the parameter space that is worth to probe.

In our case we decided to use the Inductively Coupled Plasma Etching tool - Plasma Therm Versaline LL ICP Dielectric Etcher. Based on the literature review and mentors expertise we decided on using CF_4/CHF_3 gas mixture and determined other parameters based on standard

oxide etching recipes. We decided to investigate the CHF_3 content between 0.2 and 0.8, while keeping the total flow constant at 50 sccm, in addition we varied the RF power between 100 and 150 W , and chamber pressure between 10 and 20 mTorr. Based on these values we prepared a full-factorial design of experiment using JMP software, details and results are described in the DOE section.

PECVD oxide deposition

For the silicon dioxide deposition we use one of the standard procedures available in PlasmaTherm Shuttlecock PECVD System (ccp-dep) at SNF. We use SIO350-0 recipe, that results in a layer with the stoichiometry close to SiO_2. For the purpose of the etching DOE we deposit dielectric layer on silicon wafers but, for the final devices we will work with chips. While the standard operating procedures for wafers is well-known it is worth to mention the SOP for pieces. This part has to be consistent from run to run since the deposition rate is non-uniform and cleanliness standards may impact the results.

Silicon Dioxide Deposition Standard Operating Procedure for 5x10 mm^2 chips:

1. Clean device chip and calibration Si piece with acetone and 2-propanol. Spray acetone for 30 seconds, then repeat with 2-propanol, blow dry with nitrogen gun.

2. Enable ccp-dep on badger, load the empty wafer holder into the process chamber if it's in the load lock.

3. To avoid changing the process conditions it is recommended to clean the chamber before each deposition. For this purpose, load the standard cleaning recipe at the same temperature as your deposition (in this case 350C). Go to Process->Chamber->Load… and choose recipe CLN350.

4. Go to Ready state by clicking the READY button on the main panel and check the temperature readout.

5. Click RUN and set the process time to 20 min.

6. When the process is done go back to the Standby mode by clicking STANDBY button.

7. Go to Service->Maintenance->Wafer Handling, in the new window click Unload to transfer the stage to the load lock.

8. When the transfer is done exit the Wafer Handling and click Utilities->Vent to vent the load lock.

9. Be careful when lifting the load lock lid - it is heavy and can slam your hand.

10. When the venting is done load four carrier wafers on the stage. Be careful - the stage is currently at around 350C, do not touch it with your hand or plastic tweezers as it will cause burns and will melt tweezers and vinyl gloves. Be sure to align the flat of the wafer to the tweezer trench.

11. Close the lid and pump the chamber down: Utilities->Pump.

12. When the chamber is at vacuum go to Wafer Handling (see p. 7) and click Load to transfer material to the process chamber. Close Wafer Handling window.

13. Load the recipe: Process->Chamber->Open and choose SIO350-0 recipe to load it.

14. Go to ready state (see p. 4) and click RUN, set the time to 5 minutes to condition the chamber and wafers.

15. When the process is done transfer carrier wafers back to the load lock (p. 6-9).

16. Load the chip for processing on the top right section of the bottom-left wafer, close to the center of the stage, about 1 cm from the wafer edge. Load the calibration Si piece on the top-left carrier wafer, in the bottom right section of the wafer.

17. Pump the load lock and load the material (see p. 11-12).

18. Go to ready state (see p. 4) and click RUN, set the time to deposit the target thickness. Measured deposition rate: 62.82 nm/min.

19. When the process is done go to the Standby Mode and transfer the material back to the load lock (p. 6-9).

20. Unload the chip and wafers. Chip is small and cools down quickly so it can be transferred directly to the sample box. While unloading wafers, place them on a clean piece of aluminum foil and let it cool down when pumping down the load lock (see p. 11).

21. Transfer the stage to the process chamber and repeat the cleaning procedure for the next user (p. 3-5).
22. Put carrier wafers back to the cassette.

23. You can disable the tool on Badger when running the final celan.

24. Measure the thickness of the deposited film on the calibration Si piece using Woollam Ellipsometer or NanoSpec.

ICP RIE Standard Operating Procedure

For the oxide etching we use Plasma Therm Versaline LL ICP Dielectric Etcher (PT-Ox), for the process development we used two chips per each run - one with niobium layer on sapphire and one with PECVD-deposited silicon dioxide on silicon. With this strategy we were able to compare the etching rates for SiO_2 and Nb. Here we describe a general SOP for processing a single chip, we will describe the process in which members of the SNF community can etch the Niobium structures selectively to the sapphire substrate and silicon dioxide. Moreover, this SOP will also allow for etching silicon dioxide selectively with respect to Niobium.

Mounting a chip on the carrier wafer using Diffusion Pump Oil

Having a good thermal contact between the stage and the sample is a crucial aspect of the reactive ion etching process, since it can affect the etching rate and lead to overheating small chips if done improperly. For the purpose of this project we investigated two methods of mounting the chip on a carrier wafer - using 5% PMMA and Diffusion Pump Oil. The former turned out to be faulty and led to chemical reaction of the PMMA with the etching gas mixture and redeposition - see Figure 7.

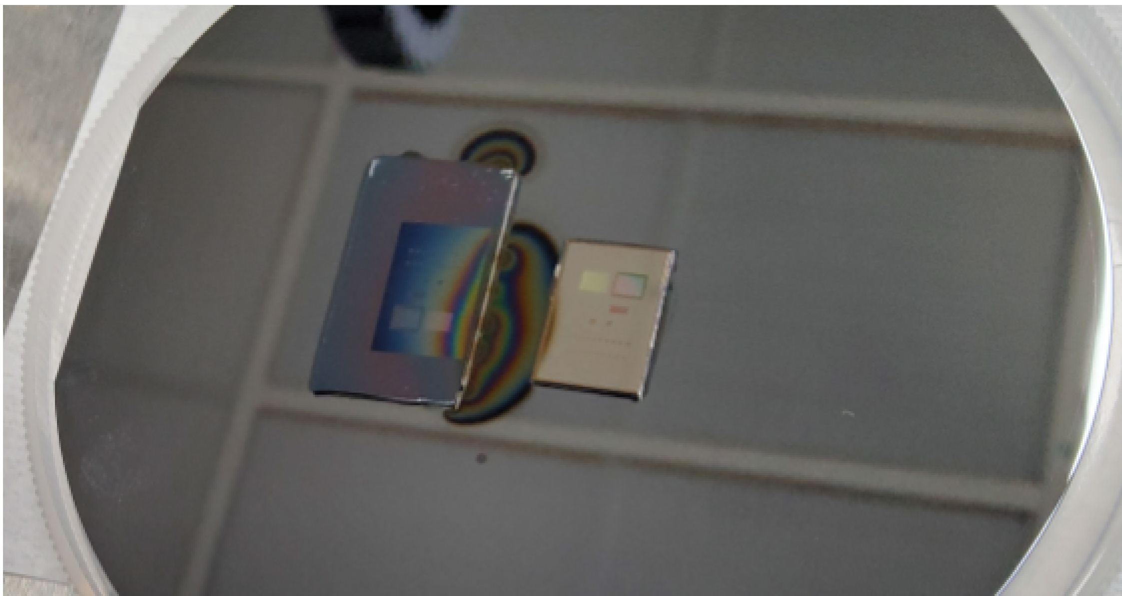


Fig. 7 Thin film interference pattern on the layer re-deposited after using 5% PMMA for mounting chips on PT-Ox carrier wafer.

To avoid PMMA redeposition we switch to the Diffusion Pump Oil, it doesn't hold the chip tight but we mostly care about the thermal contact. Application of the oil requires some practice and has to be precise because we don't want to have exposed oil during the etch. The general procedure for oil application on small chips is:

1. Take your chip in tweezers and ensure that the backside is clear, especially that there is on resist residue.
2. Take the oil bottle and immerse the tip of the pipette. For 5x10 mm^2 chips use the small plastic resist pipette, for larger chips use directly the pipette from the oil bottle.
3. Gently touch the backside of the chip with the pipette to make a small drop stay on the chip.
4. Put the chip in the center of the carrier wafer and spread the oil under the chip making several movements in x and y, you should feel oil drag when the oil is spread properly.

SOP

Standard operating procedure is the same for PT-Ox and PT-MET, the only difference is the recommended cleaning procedure, hence we compile the general SOP here for both tools and will point out differences. Figure 8 shows the user interface of the PlasmaTherm Versaline Software, section A allows for the recipe selection, section B shows the state of the system and wafer localization, C displays current job, D - current and set chamber parameters, E - allows to vent and pump the load lock, F - starts/stops the job.

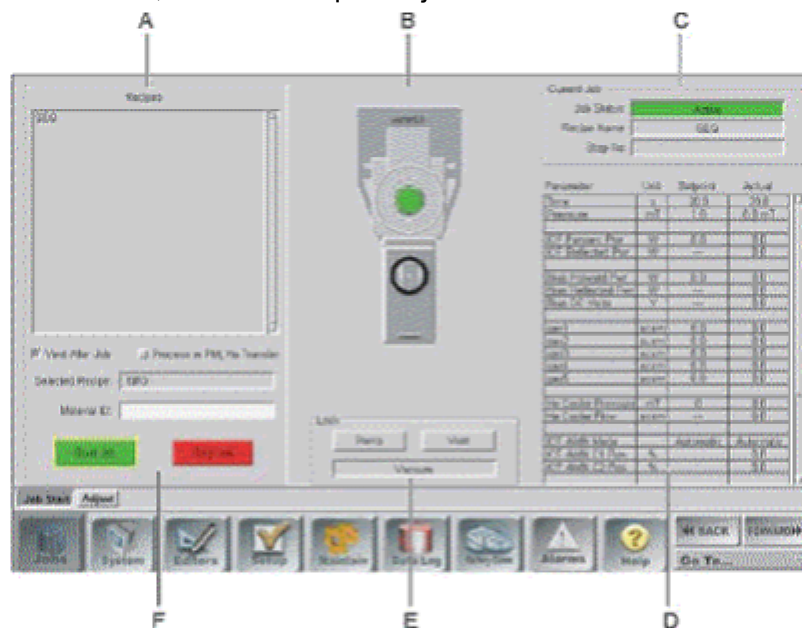


Fig. 8. PlasmaTherm Versaline Software GUI.

1. Arrive at the tool with prepared carrier wafer and chip with patterned and hard-baked photoresist.

2. The alarm “Facilities service has failed” indicates that the equipment is disabled in Badger. This alarm will disappear when the equipment is enabled.

3. Check if the transfer arm screws are set to the correct wafer size.

4. Enable the tool on Badger.

5. Make sure that there are no active alarms on the system and the chamber is empty.

6. Vent the loadlock using “Vent” button in section E of the GUI.

7. Open the load lock and load the wafer, align the flat to the screws and straight line on the stage.

8. Close and pump the load lock using “Pump” button in section E of the GUI.

9. Click “Maintain” button in the bottom menu and switch all chambers into Maintenance Mode, go to material transfer tab and transfer the material to the process chamber.

10. When done switch all chambers back to Production Mode.

11. Go back to the main screen and choose recipe *O2 Clean1*, check the “Process in PM No Transfer” box to keep the wafer in the process chamber after the cleaning procedure.

12. Default time of the procedure is 10 minutes, run it twice or go to Editor -> Sequence Editor and open the recipe. Then click on the third step (actual etch) and edit it, change the time to 20 minutes and save the step. Caution: saving the step will modify any recipe that uses it, a good practice is to have your own steps for your recipes to make sure that you don’t modify other users’ processes.

13. Run the cleaning procedure by clicking “Start Job”.

14. When the cleaning process is running prepare your recipe, for this purpose go to the Editor and create new or open existing one. To edit process parameters follow instructions in p. 12. For example, a selective etch of SiO2 vs Nb can be achieved using 40 sccm of CF_4 , 10 sccm of CHF_3, 20 mT chamber pressure, 150 W bias power; Recipe HSS_OX-CF4CHF3. Measured selectivity is 8.42, oxide etch rate: 171.35 nm/min, Nb etch rate: 20.34 nm/min.

15. When the cleaning process is done run your desired recipe for 5 minutes to condition the chamber and carrier wafer. Before starting the job, make sure that the temperature of the stage is at the target value, if not - click “Go To Recipe Temperature”.

16. When conditioning done go to Maintenance Mode and transfer the wafer back to the loadlock, vent it.

17. Take the wafer out and load the chip following the procedure described in the previous section “Mounting a chip on the carrier wafer using Diffusion Pump Oil”. When done, load back the wafer following p. 6-10.

18. Change the time of the etch to achieve the desired etch depth and run the procedure.

19. Unload the material following p. 16, take the wafer out and pump the load lock down. Remove the chip and gently clean the oil residue from the back, clean the carrier wafer using acetone and 2-propanol, spray each for 30 seconds and blow-dry with nitrogen gun.

20. Disable the tool on Badger.

ICP Etching Design of Experiment

For the purpose of achieving high selectivity etch of the we run a Full Factorial Design of experiment. We probe the following parameters space:

- CF_4/CHF_3 10:40 - 40:10
- Bias power: 100-150 W
- Process pressure: 10-20 mTorr

In addition, we ran a single point with only 50 sccm of CHF_3 in the chamber to verify if that gives even better results. The complete DOE was generated using JMP software, table summarizing the entire effort is presented below, including measured etch rates and selectivities. Selectivities and etch rates were calculated based on the profilometer measurements before etch, after etch and after stripping the resist. For high selectivity measurements we cleaved samples along etched test lines and analyzed them under the SEM.

#	CF_4/CHF_3	Bias (W)	Pressure (mT)	Time (min)	SiO2 rate (nm/min)	Nb rate (nm/min)	Photoresist consumed (nm)	Selectivity vs PR	SiO2/Nb selectivity	Sidewall angle (°)
1	25:25:00	125	15	1	223.2	58.74	234.59	0.95	3.8	
2	40:10:00	100	20	1	174.46	75.64	258.97	0.67	2.31	
3	40:10:00	100	10	1	264.2	107.87	360.61	0.73	2.45	
4	40:10:00	150	20	1	208.07	80.9	302.31	0.69	2.57	
5	40:10:00	150	10	1	312.59	118.73	416.88	0.75	2.63	
6	10:40	100	20	1	134.97	16.21	123.95	1.09	8.33	23.35
7	10:40	100	10	1	234.28	33.42	168.64	1.39	7.01	22.90
8	**10:40**	**150**	**20**	**1**	**171.35**	**20.34**	**87.58**	**1.96**	**8.42**	**21.65**
9	10:40	150	10	1	292.06	39.83	204.54	1.43	7.33	21.15
10	0:50	150	10	1	288.53	30.12	120.46	2.4	9.58	**19.25**

Run number 8 was bolded - this is the one that we determine to be the best for our process. Even though run 10 has higher selectivity, it also has a slightly smaller sidewall angle, as determined under the SEM. For our purpose we want this angle to be high, so that we can deposit niobium layer that can cover it. Figure 9 presents a false-color SEM picture of the sample 9 cross-section, sidewall angles are measured using built-in tools of the SEM.

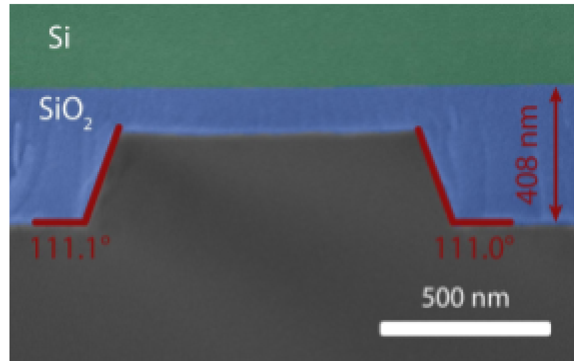


Fig. 9. False-color SEM of the sample 9 cross-section. Blue represents the silicon dioxide layer, green is the silicon substrate.

Generated data was analyzed using JMP software, we determine that the CHF_3 content is the main factor in the described process and it is quadratic, other important factors are CHF_3 content and chamber pressure interaction and the pressure itself. It turns out that the RF bias power is negligible when it comes to selectivity, as it increases Nb and SiO_2 etch rate in a very similar manner. Figure 10 (A) summarizes the selectivity as a function of pressure for all of the process parameters, Figure 10 (B) shows the etch rates of silicon dioxide, and (C) for the niobium.

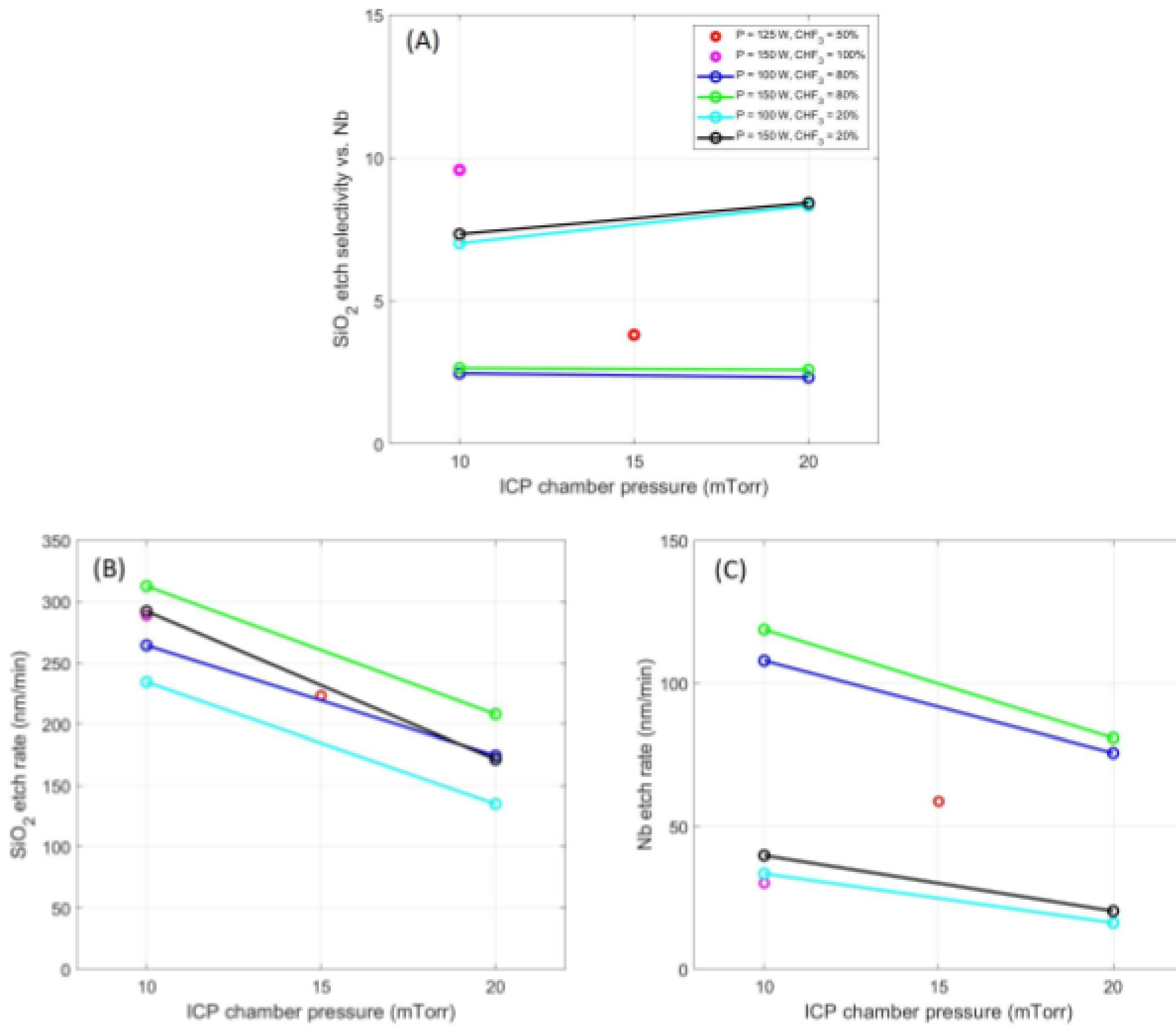


Fig. 10 Summary of the silicon dioxide etching DOE: (A) Selectivity to Nb, (B) Etch rates for SiO_2, (C) Etch rates for niobium.

Niobium patterning with high selectivity with respect to SiO_2

The motivation for this section is to explore the parameter regime for a highly selective niobium etch with respect to SiO_2 using dry etching technique.

Literature review

Studies have shown that dry etching of Nb as opposed to wet etching with respect to designing superconducting resonators/Josephson junctions has plenty of advantages like no dangerous chemicals and good process control without sacrificing etch rates[25]. Moreover, our decision of

using fluorine chemistry for etching rests on the fact that chlorine chemistry etches Sapphire, which is the substrate we are going to use for our process. This allowed us to take the decision of exploring Inductively Coupled Plasma- Reactive Ion Etching (ICP-RIE) technology for etching Nb in Versaline's PlasmaTherm Metal Etcher tool at SNF. Now we needed to find a proper parameter space constrained by the limits of this tool. Studies have been done in the past using SF_6/Ar[26] and CF_4/O_2[23-24,27] gases for selective dry etching of Nb but the parameter regime these studies explored was too outside the scope of the PT-MTL tool we have at SNF.

These reviews gave us a seed parameter space that we could probe to infer more information within the available space in PT-MTL. The extensivity of studies done using CF_4/O_2 gases for selective Nb etch made us confident to design a DOE with CF_4 flow rate at a fixed 50 sccm, ICP power at 600W and substrate temperature at 20C, while varying the RF bias power, chamber pressure and O_2 flow rates between 50-150W, 10-50mTorr and 2-10sccm respectively. Half way through the DOE, we realized that the best selectivity of Nb to oxide achieved is 0.726. Seeing trends like the decrease in RF bias power and increase in chamber pressure pushed towards a better selectivity or increased O_2 rate doesn't really affect selectivity to oxide, we designed a new DOE using JMP software with a revised set of parameters. We also wanted to explore the effect of substrate temperature on selectivity since there has been no studies for this parameter in the context of dry etching of Nb. The revised DOE is discussed in detail in the next section.

ICP Etching Design of Experiment

For the purpose of achieving high selectivity etch of Nb, we run a Full Factorial DOE with ICP Power at 1000W, chamber pressure at 50mTorr and CF_4 flow rate at 70 sccm, probing the following parameters space:

- O_2 flow rate: 0-2 sccm
- Bias power: 10-50 W
- Substrate Temperature: 20-60 C

The table showing the complete DOE is presented below, including measured etch rates and selectivities. Selectivities and etch rates were calculated based on the Alphastep 500 profilometer at SNF and Dektak profilometer in SNC, using the following set of formula:

Assuming pre-etch step height = x, post-etch step height = y, post-clean Nb step height = z, post-clean SiO_2 step height = z' and etch time in seconds = t

$$PR\ etch\ rate/min = 60\left(\frac{x-y+z}{t}\right)$$

$$Nb\ etch\ rate/min = \frac{60z}{t}$$

$$SiO2\ etch\ rate/min = \frac{60z'}{t}$$

$$Nb : SiO2\ selectivity = \frac{z}{z'}$$

$$Nb : PR\ selectivity = \frac{z}{x - y + z}$$

#	RF Bias Power(W)	O2 Flow(sccm)	Subs. Temp(C)	Nb etch rate (nm/min)	SiO2 etch rate (nm/min)	PR etch rate (nm/min)	Nb:SiO2	Nb:PR
1	50	2	20	283.2	114.5	251.0	2.473	1.128
2	50	2	60	562.8	140.1	413.4	4.011	1.361
3	30	1	40	329.7	85.2	236.7	3.846	1.392
4	10	2	20	383.0	50.76	37.4	7.569	10.229
5	**10**	**2**	**60**	**563.6**	**63.6**	**380.2**	**8.862**	**1.482**
6	10	0	20	107.4	43.3	335.4	2.477	0.320
7	50	0	20	182.4	145.2	428.4	1.257	0.425
8	10	0	60	380.4	79.2	380.4	4.799	1.000
9	50	0	60	402.0	130.2	537.6	3.087	0.747

The fifth run in this table is highlighted, since it gives us a very high selectivity for etching Nb. Although the etch rate of Nb is also very high, which is not completely desirable, but this can be treated as an optimal point for our process.

Analysis and Conclusions

This obtained data was analyzed using the JMP software. From all the runs in both seed and recentered DOE, we conclude that chamber pressure and RF bias powers are the two most important factors in the selective etching of Nb. Although O_2 flow rate doesn't have a great impact on the selectivity to oxide, its absence tends to decrease selectivity. The substrate temperature seems to have an impact on selectivity, presumably due to the increased volatility of reaction by-products at higher temperatures. Figure 11 (A),(B),(C) summarizes the univariate impact on selectivity as a function of O_2 flow rate, substrate temperature, and RF bias power respectively, while Figure 11 (D) shows a 4D hyper-plot demonstrating the impact as a combination of all the parameters.

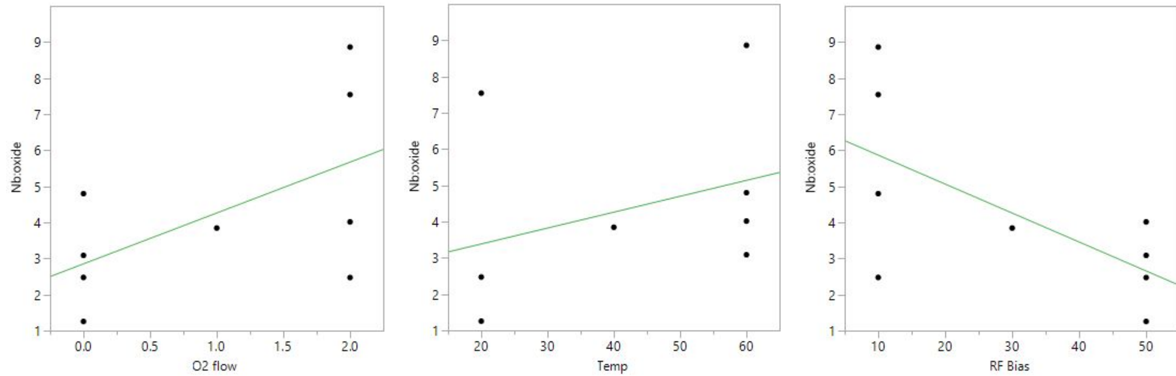
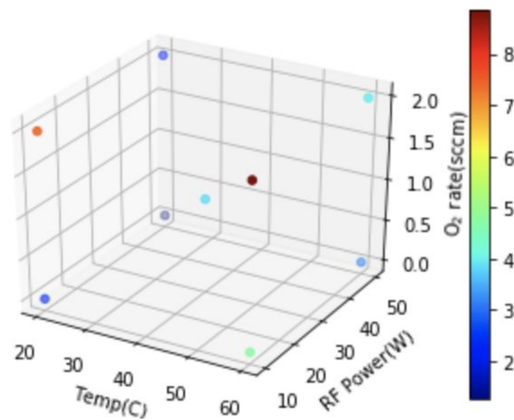


Fig 11. (A) Nb selectivity vs O_2 (B) Nb selectivity vs temp (C) Nb selectivity vs RF bias power



(D) Holistic Nb selectivity

Device design

Test pattern characterization

During the etching experiments we used a pattern that we designed specially for this purpose, it consisted of calibration etched lines and ridges with thickness between 0.5 and 4 μm, calibration circles with diameters of 0.5-20 μm, squares for the step height measurement and test patterns for the bottom electrode and the dielectric layer. When the Nb etching process was developed we also patterned meander inductors as a test before making resonators.

Test patterns were analyzed using scanning electron microscopy on the sample with the highest selectivity - run no. 10 from the silicon dioxide etching DOE table. Based on this study we can estimate the minimum feature size achievable in our process. On the Figure 12 (A) we can see an etched line of around 950 nm, (B) shows the smales resolved circle with diameter around 875 nm. As a result, we can assume that 1 μm feature size, which is enough for our project, is

achievable with no further optimization. In the future we might run a dose-defocus study on the Heidelberg and optimize the development time to improve the accuracy.

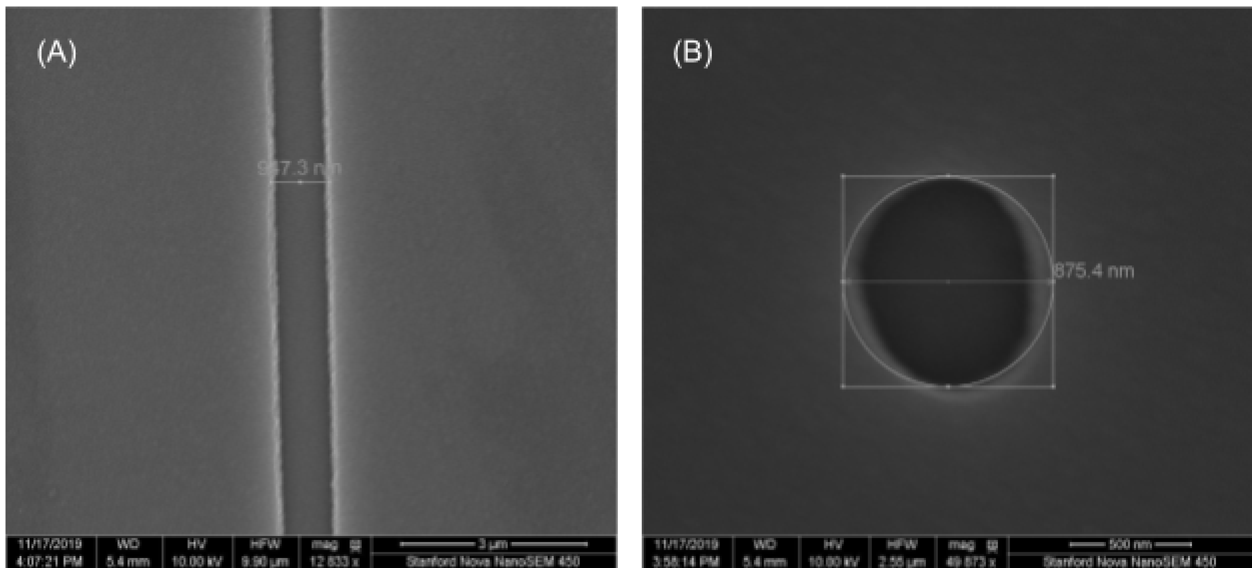


Fig. 12 SEM micrograph of lines (A) and circles (B), that are resolvable in our silicon dioxide etching process.

Another part of the test pattern, critical for the dielectric layer process was the actual pattern, which can be seen in Figure 13 (A). Hexagonal symmetry of the pattern is supposed to ease the releasing process, we plan to etch the circles in the pattern so that we can deposit niobium inside, when forming the top plate of the capacitor. In this way we will form posts to support the top layer of Nb. Figure 13 (B) shows a zoom into the etched circle, we can see that the effective diameter is about 5.3 µm, comparable to the desired 5 µm.

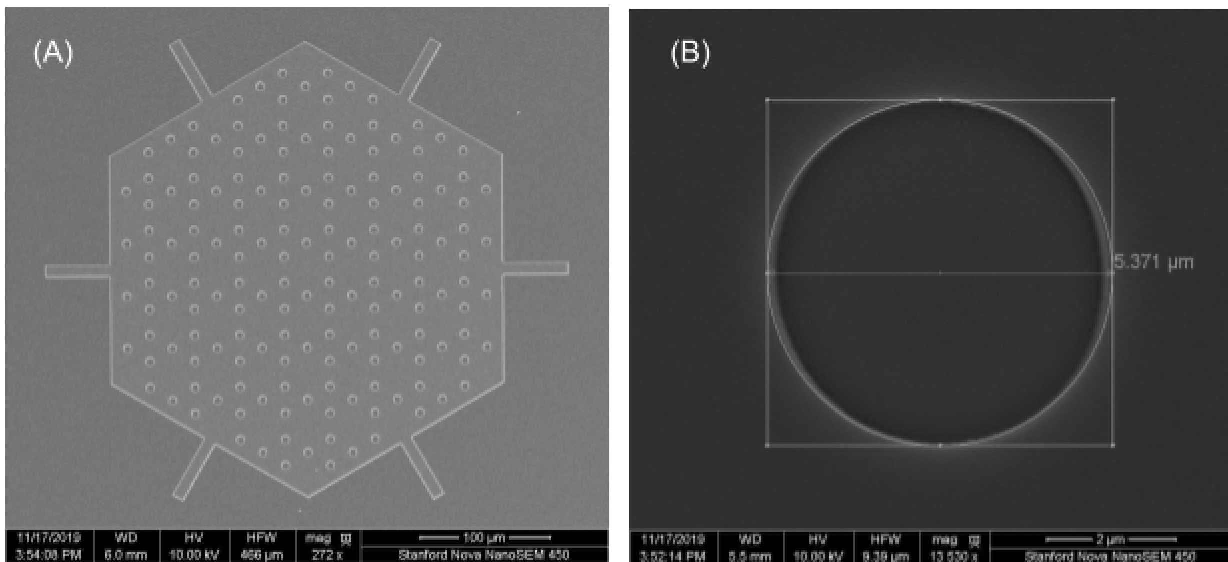


Fig. 13 (A) SEM micrograph of envisioned dielectric layer for the parallel plate capacitor, (B) Zoom into one of the circles etched in the pattern in (A).

In the next step we will stack layers like this, made of Nb, SIO_2 and Nb to build an actual device, Figure 14 (A) presents a false-color SEM of the bottom plate of the capacitor on sapphire substrate. We also already fabricated meander inductors as a presentation of the process potential, example microscope image is visible in Figure 14 (B).

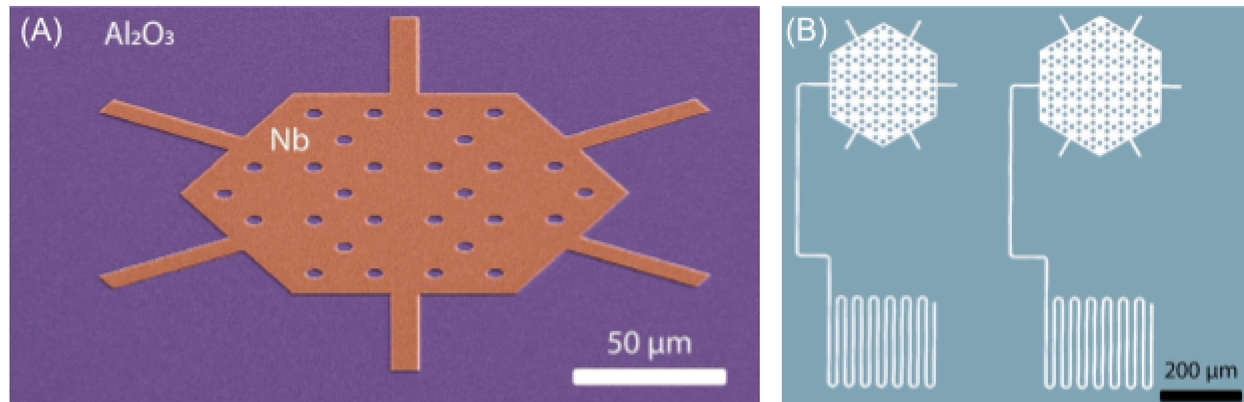


Fig. 14 (A) False-color SEM micrograph of the capacitor bottom-plate made of Nb on sapphire substrate, (B) microscope image of an example of the bottom plate connected to a meander inductor (light blue background is sapphire substrate).

Summary

In summary, we developed all of the steps that we promised to deliver during the Autumn quarter for the purpose of ENGR 241: Advanced Micro and Nano Fabrication Laboratory. We tested the Lesker Sputtering tool in the context of superconducting niobium deposition and proved that the tool currently doesn't allow to deposit high quality films. We suppose that it is mainly because of the chamber contamination, since a wide variety of materials is allowed, and targets changing cycle. Venting the chamber every day to switch targets prohibits it from reaching very low pressures, necessary to deposit good-quality films with low impurities content. We also developed two etching procedures - one for niobium and one for the dielectric layer, both are very selective with respect to the other material (selectivities around 8-10) and uniform. We also demonstrated that the fabrication process is capable of making desired structures, like capacitor elements and inductors. Combining all of these parts not only will allow us to fabricate and test useful devices in the next quarter, but also is very tempting from the perspective of other SNF community members for making a variety of niobium-based superconducting devices, including multi-layer stacks with silicon dioxide.

Future work

Characterization of a new Lesker deposition system

To provide something valuable to the entire SNF community we would like to compare the performance of the new and old KJL Sputtering system. We plan to run identical Niobium depositions on both of these tools, except we will let the new KJL sputtering system reach its base pressure. The comparison will aim to highlight that a difference in vacuum-cycling may impact the electrical, mechanical, and structural properties of Niobium films.

Additionally, we will have new characterization capabilities in the next quarter, when the new KJL is scheduled to come online. A Lakeshore 8404 Hall measurement system has been installed in SNF that has the capability to do resistance measurements as a function of temperature. The system can go down to temperatures as low as 7 K with a cycle time of 6 hours, which gives us access to measuring T_c directly. Since we can measure T_c directly, it would become our main characterization metric.

Capacitance and Resonator Measurements

Next quarter, we plan on merging the results from every portion of this project and fabricate parallel-plate capacitors. In order to characterize these capacitors we have two options (1) use the Micromanipulator in SNF to conduct C-V measurements and (2) use a Vector Network Analyzer owned by the Safavi-Naeini group and measure the impedance as a function of frequency. Fitting this spectrum will provide us with the lumped-element capacitance value. However, a C-V measurement with the micromanipulator can only be done at room temperature.

We have access to a Montana Cryostat fitted with microwave input-output lines. Therefore, we can characterize these Niobium parallel plate capacitors as a function of temperature and frequency. This setup will also help us characterize resonators we plan to fabricate. These resonators will be designed to have resonant frequencies around 5 GHz (X-Band). Eventually, our figure of merit for fabrication process will be the quality factor of these resonators because this is what matters to us in the end.

Structures releasing

When arriving with the non-planar capacitor geometry we will have to develop a way to release the structure by etching the sacrificial layer of silicon dioxide out and not collapsing the niobium. For this purpose we need an isotropic etching technique that is selective with respect to niobium. Ideally, we would like to use dry etching to avoid issues with capillary forces while

drying chemical compounds. For this reason, we will start with vapor HF etching using SPTS μetch. Hydrofluoric acid is well known etchant for PECVD-grown silicon dioxide and shouldn't impact niobium[28]. The other way that we might use, in case the first method doesn't work is wet chemical etching using buffered HF solution. In this case, however, we would also need to possibly exchange the HF to another liquid in the released structure and develop a method for supercritical point drying in SNF.

The abovementioned method would be also helpful for releasing other structures, like spiral inductors - we propose to fabricate them and build a non-planar resonator by combining them with parallel plate capacitors. Release step is necessary for the spiral inductors to avoid shorting its wires - planar waveguide has to spiral down to a point and then be connected to the region outside of the inductor. For this purpose it has to go either below or above the wires forming the spiral.

Runsheets

Niobium Deposition and Characterization

Metal Deposition	chip prep	chip clean	rinse with flowing ACT + IPA, 30s + 30s. N2 dry	wbsolv
	pre-dep	chamber conditioning	coat chamber with Ti (20 mins), then Nb (15 mins)	lesker-sputter
		sample load	load sample	
	dep-sputter	Nb sputtering	run dep recipe (Master Recipe Src 1 Downstream Control)	
	recovery	unload sample	unload and clean up area	

Characterization	resistivity	-	measure resistivity (center 1 point measurement)	prometrix
	step height	-	measure step height	dektak

Silicon Dioxide Deposition and Etching

SiO2 deposition		Chip clean	Rinse with flowing Acetone + IPA, 30 s + 30 s. N2 blow dry.	Solvent bench
	Oxide deposition	Chamber cleaning	Unload dummy wafers, procedure CLN350, 30 min (should be as long as the last deposition step)	ccp-dep
		Chamber conditioning	Load 4 carrier wafers, run the target recipe (SiO350_0)	
		Sample loading	Place the chip on the top of the bottom-left wafer, close to the center of the stage	
		SiOx deposition	SiO350_0, deposition rate 62.82 nm/min	
		Chamber cleaning	Unload dummy wafers, procedure CLN350, 30 min (should be as long as the last deposition step)	
		Thickness measurement	[65,70,75] deg, 40 rev/meas, high-accuracy	Woollam or Nanospec

SiO2 patterining	Photolitho	HMDS prime/Bake	Standard HMDS for wafers/Dehydrate bake 5 mins at 180C for chips	YES oven
		Spin coat	SPR3612 1.0 um; 40 s at 5500 rpm	Headway2
		Pre bake	Bake 1 min at 90C	Hotplate
		Exposure	Dose 100, defoc 0	Heidelberg 2

		Development	50s MF26A, 20s DI water rinse for chips/spray for wafers. Develop wafers upside-down to avoid redeposition of the resist residue.	wbmiscres
		Pattern verification	Observe the developed pattern under the optical microscope	Optical microscope
		Hardbake	3 min at 115C	Hotplate
		Cleaving	Cleave Siwafer into pieces if applicable	
	Etching SiO2	Chamber cleaning	Load dummy wafer, run oxygen plasma sequence ~20 min; Recipe *O2 Clean1*	PT-Ox
		Chamber conditioning	Run the target recipe for 5 minutes with the carrier wafer inside	
		Mounting on carrier	Small drop of the diffusion pump oil on the back of the chip, place on the wafer and spread the oil, gently moving the chip in x, y.	
		Etching	CF4 40 sccm, CHF3 10 sccm mix, total 50 sccm, 20 mT, 150 W bias; Recipe *HSS_OX-CF4CHF3*	
	Sample clean	Step measurement	Range: 6.5 micrometers, length: 800, duration: 10s, stylus force: 2 mg	Dektak
		Oxygen plasma clean	Indirect (bottom plate) ashing with 100W, 10 sccm O2 flow, 120 s	Asher
		Stripping resist	Spray acetone + IPA, 30 s each N2 blow dry; fill a short beaker with fresh acetone and put chips in, ultrasonic bath for 5 minutes, level ~1.5; N2 blowdry	Solvent bench
		Step meas.	Range: 6.5, l: 800, duration: 10s, stylus force: 5 mg	Dektak

Niobium Etching

Nb patterning	Photolitho	Dehydration baking	Dehydrate bake 5 mins at 180C	Hotplate
		Spin coat	SPR3612 1.0 um; 40 s at 5500 rpm	Headway2
		Pre bake	Bake 1 min at 90C	Hotplate
		Exposure	Dose 100, defoc 0	Heidelberg 2
		Development	50s MF26A, 40s DI water rinse, N2 blowdry	wbmiscres
		Pattern verification	Observe the developed pattern under the optical microscope	Optical microscope
		Hardbake	3 min at 115C	Hotplate
	Etching Nb	Chamber cleaning	Load carrier wafer, run clean sequence *Cham_Cln_Def_Cl2_SF6_O2*	Solvent bench
		Chamber conditioning	Run the target recipe for 5 minutes with the dummy wafer inside	PT-MTL
		Mounting on carrier	Small drop of the diffusion pump oil on the back of the chip, place on the wafer and spread the oil, gently moving the chip in x, y.	
		Etching	CF4/O2; Recipe: *DDas_Nb_Etch-2019a*	
	Sample	Step	Range: 6.5 micrometers, length: 800, duration: 10s,	Dektak

	clean	measurement	stylus force: 2 mg	
		Oxygen plasma clean	Indirect (bottom plate) ashing with 100W, 10 sccm O2 flow, 120 s	Asher
		Stripping resist	Spray acetone + IPA, 30 s each N2 blow dry; fill a short beaker with fresh acetone and put chips in, ultrasonic bath for 5 minutes, level ~1.5; N2 blowdry	Solvent bench
		Step measurement	Range: 6.5 micrometers, length: 800, duration: 10s, stylus force: 5 mg	Dektak

Financial Report

	Budget – Fall Quarter 2019				
TOOL TIME	**Tool**	**Training Cost ($)**	**Time (h)**	**Rate ($/h)**	**Subtotal ($)**
	wbexfab_solv	0	2.95	10	29.50
	Heidelberg	480	6.60	35	711.00
	woolam	160	0.42	50	180.83
	ccp-dep	0	0.75	50	37.50
	PT-MTL & PT-Ox	0	22.33	50	1116.67
	uetch	0	0.00	50	0.00
	lesker-sputter	80	51.90	35	1896.50
	disco-wafersaw	0	2.70	35	94.50
	prometrix	0	2.42	50	120.35
	Headway2	0	0.17	50	8.33
	Headway3	0	0.83	10	8.33
	YES Oven	0	2.05	50	102.50
	SNF Safety Tour	120	-	-	120.00
	All-litho	160	-	-	160.00
SUPPLIES	**Name**	**Count**	**Price ($)**		**Subtotal ($)**
	Silicon 4" wafers	12	17		204.00
	Sapphire 4" wafers	1	55		38.00
	Containers and covers	116			116.00
	Nb target	2	320		640.00
	Tweezers	48			48.00
			Grand Total:		**5632.02**

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Authors Contributions

H.S. ran and analyzed the results of the DOE for the selective etching of SiO_2 with respect to Nb and assisted with the Nb selective etching DOE, prepared CAD files for the test etch patterns and devices and analyzed results under SEM, developed the cleaning procedure, optimized post-exposure photoresist development scheme and prepared oxide layers for DOE procedures.

K.K.S.M. performed the Nb depositions for the KJL sputtering system and the Plassys E-beam evaporation system, analyzed the performance of deposition systems and Nb films via 4-point probe measurements and profilometry, developed mounting procedure for low and high temperature sputtering depositions for Nb pieces, developed deposition recipe for the KJL sputtering system, and designed the LC resonators to be fabricated next quarter.

D.D. performed the DOE and analyzed the experimental data to etch Nb selectively with respect to SiO_2 using JMP. Figured out a method to spin-coat small chips on larger chucks using a blue tape. Also found an appropriate program on Alphastep to measure step heights in small chips. Helped H.S. in developing the cleaning procedures. Also plan to help K.K.S.M. with resonator design CAD for the next quarter.

H.S., K.K.S.M, and D.D. did literature review and developed a detailed plan for the project.

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