Standard Process for Prototyping Flexible Devices

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Executive Summary

The field of flexible electronic devices has been expanded for decades. In this project, we focused on developing a standard processes for prototyping flexible structures in simple and cost efficient way. The previous process, developed in the Structures and Composites Laboratory, used polyimide (PI) as a flexible substrate and patterned a design with ASML lithography, O_2 plasma etch. However the photolithography and etching processes were time and cost consuming, which motivated this project to develop more efficient and simple prototyping process. We explored four major scopes: release method, wafer preparation, polyimide patterning, and photolithography.

Choosing a release method of flexible structures from standard silicon wafers are critical in reducing process time. We studied dry etch and wet etch methods. Given SNF tool setup (Xactix), we found that Ge layer etching with XeF_2 gas was desirable for its high etch rate and stiction-free process which was a crucial problem of wet etch.

To get the Ge layer on the silicon wafer, there are options to purchase from vendors at high cost and/or long lead times. Instead, we built Si-SiO_2-Ge layers from CVD and E-beam deposition.

Polyimide can be patterned with three different methods: O_2 plasma etching, photopatternable PI, and photodefinable PI. The conventional O_2 plasma etching requires multiple steps to etch, making the process too complicated and long (i.e. metal mask and liftoff). On the other hand, photopatternable PI can be simply patterned by exposure - development process which saves a lot of process time. However, there will be an undercut of the PI layer when it develops; thus, the user should carefully select the appropriate dose and development time. Photodefinable PI makes the process much simpler by exposing on PI layer and develop exposed patterns. However, a particular developer and manual developing process are needed because SNF is not equipped with them.

For photolithography exposure processes, we explored using Heidelberg tool for its fast prototyping without any costs or lead time for masks. We studied a resolution limit and right dose/defoc values for photopatternable PI by using “series exposure”. With the tested exposure and development settings, we built a testing structure for studying dry etch rate of Ge-XeF_2. The etch rate was approximately the same as the datasheet of Xactix, however potential decelerations of process due to the flexible substrates were discussed.

From the studies of the overall process, we built a decision flow chart for future users. This, combined with a set of process parameters, should make it easier for new users to create flexible devices.

Process Summary

Wafer Preparation

1. Purchase SiO_2 wafer
   > 1.5 um SiO_2

2. Deposit Ge
   Innotec E-beam Evaporator
   100 A Cr @ 0.5 A/sec
   3000 A Ge @ 2.2 A/sec

Pattern Photopatternable Polyimide

1. Spin-coat photopatternable PI
   Adhesion Promoter (VM-652):
   5000RPM, 20 sec
   PI2545 : T9039 = 1:2
   2000 RPM, 60 sec
   Spin-coat photoresist (SPR 3612)
   Program 7
   1 um, w/o vapor prime, 2 mm EBR

2. Hotplate bake
   140 ˚C, 10 min

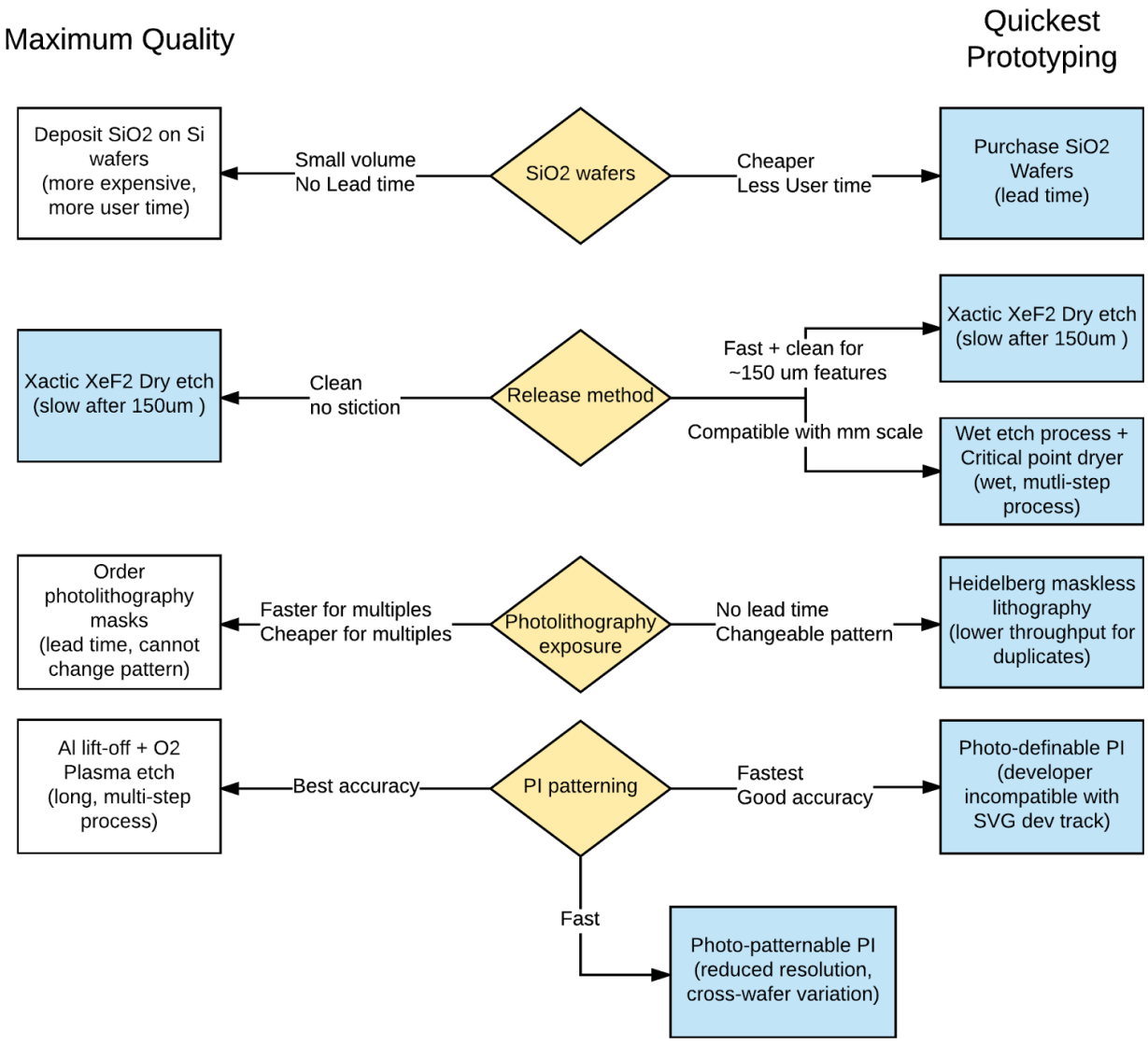
3. Convert FEA layout to GDS
   ACE 3000 Translator

4. Expose Photoresist
   Heidelberg
   85 mJ/cm^2

5. Develop wafer
   SVG
   2 x 7 sec

Release Devices

1. Dry etch Ge
   Xactix etch
   30 sec/cycle 3 mTorr
   (30 cycles to release 100 um features)


Maximum Quality
Quickest Prototyping
Deposit SiO2 on Si wafers (more expensive, more user time)
Small volume
No Lead time
SiO2 wafers
Cheaper
Less User time
Purchase SiO2 Wafers (lead time)
Xactic XeF2 Dry etch (slow after 150um)
Clean
no stiction
Release method
Fast + clean for ~150 um features
Compatible with mm scale
Xactic XeF2 Dry etch (slow after 150um)
Wet etch process + Critical point dryer (wet, mutli-step process)
Order photolithography masks (lead time, cannot change pattern)
Faster for multiples
Cheaper for multiples
Photolithography exposure
No lead time
Changeable pattern
Heidelberg maskless lithography (lower throughput for duplicates)
Al lift-off + O2 Plasma etch (long, multi-step process)
Best accuracy
PI patterning
Fastest
Good accuracy
Photo-definable PI (developer incompatible with SVG dev track)
Fast
Photo-patternable PI (reduced resolution, cross-wafer variation)

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Introduction

Motivation

Moore's law has been leading the direction of traditional electronics industry for over a century, however, with the limitation of materials physics and process cost, the current speed of further miniaturizing the transistors and enhancing the computing power is slowing down, indicating that the traditional electronics industry has reached a bottleneck. At this crossroad, flexible electronics appear on the stage and become an important development direction of future electronic technologies. Examples of flexible electronics must have features such as bendable, resilient, and unbreakable, etc.

As we are stepping into the era of artificial intelligence and big data, sensors are becoming more and more important in our daily life. Without sensors, artificial intelligence and big data are sheer moonshine. To enable the aforementioned two concepts, a myriad of sensors with high value and low cost are essential for providing tons of useful data continuously in real-time. Materials with self-sensing capabilities are the most import class of intelligent materials. Bio-inspired multifunctional structures that can carry mechanical loads as well as sensing the environments and diagnosing their health condition on a real-time basis are considered the next generation materials of the future. Unlike man-made structures, biological structures can sense and respond to the change of environments to avoid unexpected failure. This is because the biological structures are equipped with massively distributed sensors in a network to sense and monitor the conditions of the structures. Without such a network, intelligence that includes sensing and diagnosis would not be possible. Therefore, to add any intelligent functionality to structures, a highly distributed sensor network is considered to be the first step. Although sensors can now be made in nano and micro scales in a large volume through CMOS/MEMS process [1], unfortunately there are still limited techniques available to integrate those sensors into materials [2]. In most of the studies, sensors were installed individually into materials but not in a networked fashion [3].

Stretchable sensor networks have been considered as an alternative approach to deploy sensors to cover large structures. The ability to manufacture a sensor network that can be stretched and adapted to much larger areas (by orders of magnitude, e.g. more than 10,000%) and embedded into materials could be of great interest for many applications ranging from aircraft, automobiles, to buildings and appliances, etc [4-7]. Hence, as a team, our interests lie in the junction of the flexible electronics and stretchable devices, our goal of this project is to develop a general process for SNF lab users to low-costly and rapidly prototype flexible electronics with stretchable interconnections.

Current Process

The current process for fabricating stretchable sensor network was developed in Structures and Composites Laboratory (SACL) at Stanford University [8]. The existing process includes four main steps: wafer preparation, photolithography, polyimide patterning and network release. As illustrated in Figure 1, start from a carrier wafer with etch stop layer and sacrificial layer, spin coat liquid polyimide to form the network substrate, and then integrate sensors, electrodes, dielectrics and switches through direct deposition or transfer process. After that, etch through the substrate to form a stretchable network pattern. Finally the network is released from the carrier wafer, hence finishes the fabrication process. This process is based on spin coated on polyimide substrate, which is well bonded on carrier wafer. Hence in each of the fabrication step, it provides a very flat substrate. This enables the utilization of ASML 5:1 stepper as lithography tool to pattern each of the layers, and hence a key feature size and alignment accuracy of up to sub micron is achieved to fabricate the network on polyimide substrate.

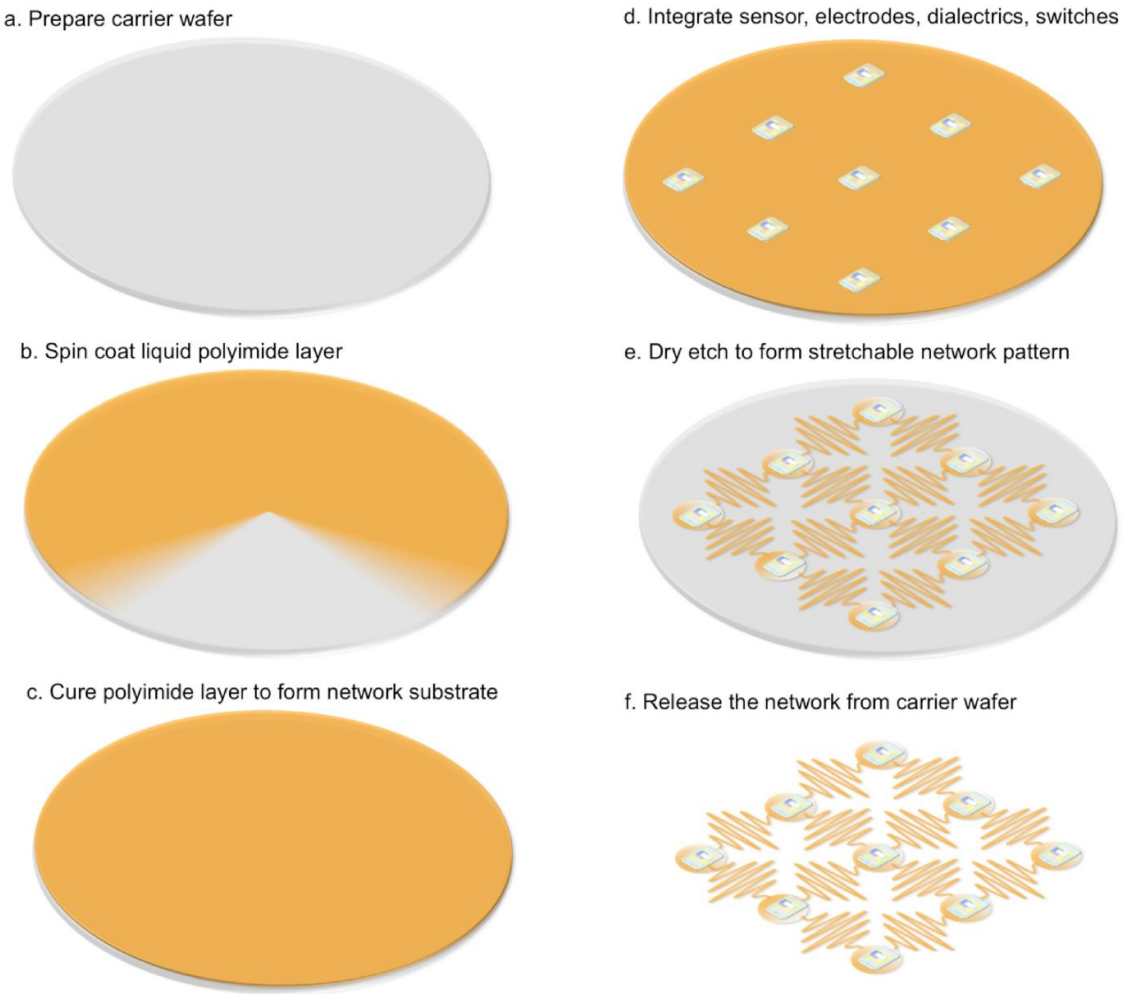


Figure 1. A process flow to fabricate highly stretchable sensor networks based on spin-coated polyimide

According to materials and structure properties, appropriate methods could be used to integrate devices, electrodes, dielectrics, and switching devices into the network. Thin film metal layers, such as electrodes, resistance temperature detectors (RTDs), and organic thin film devices (organic thin film diodes), can be directly evaporated onto the network substrate. While dielectric layers in this stretchable sensor network are made from liquid polyimide layers, hence they can be spin coated on the substrate.

However, the current progress has two main drawbacks. Firstly, it is time-consuming. For example, the polyimide patterning using aluminum mask involves the deposition, photolithography and liftoff of aluminum as well as oxygen plasma etching of polyimide. The former three processes usually take at least 4 hours while the latter one takes 6 hours. Secondly, it is high-cost, especially with the traditional stepper or contact aligner based photolithographic tool that requires at least one mask per layer. These two drawbacks seriously influenced the expandability and adaptability of the process to be used by other SNF lab members or users. Hence, the target here is to develop a general process by starting from the existing process and improving it in terms of time and cost.

Process Development

Release Method

For the flexible devices, it is critical to release the flexible materials from a conventional rigid wafer. To explore the faster and simpler release method, we tested two methods for etching the sacrificial layer, dry etching and wet etching.

For dry etching, we investigated the Ge-XeF_2 etching for the following reasons. First, in SNF, we have Xactix, XeF_2 dry etching tool which is known to have an etch rate of Ge of approximately 5 - 10 um/min. Second, XeF_2 has excellent etch selectivity for Ge under standard conditions. It is also known to etch Si, but Si elements are often avoided in for their rigidity or can be protected by other materials.

For wet etching, we have explored three different etchants: Ge-H_2O (aqueous), Al-HF, water soluble adhesives. Ge is known to be etched by H_2O_2 with etch rate of 460 nm/min. To obtain similar effect, we tried to put the wafers with Ge layer and placed it in the DI water at 60˚C (Figure 2, left). As the known etch rate, its etch rate was not slower than Ge-XeF_2 dry and after it released, the structure experienced stiction to the wafer. To avoid the stiction, the wafer can be dried in a critical point dryer (CPD) following the etc. However, the combination of these two processing times is longer than the Xactix etch process for most structures (exceptions for large areas). For the other ethant, we tested Al (sacrificial layer) - HF etching. The test wafer (Figure 2, right) was a wafer with Si - Al - Polyimide (~3 um thickness). To expose the Al with HF solution, we made a square scratch on polyimide layer. As a known etch rate of 250 nm/min, it was not as fast as Ge-Xactix dry etch. Moreover, the bubbles from the Al-HF reaction was lifting up the adjacent polyimide and tore the layer. To avoid those effects, one may use HF vapor “SPTS uetch vapor etch system”, however we could not try them due to the time limit of this course.

Figure 2. Wet etch, Ge-H2O (left) and Al-HF (right); stiction and bubble were the issues of wet etch.

Water soluble layers were tested for a proof of concept. The two water soluble materials were water soluble glue (Pure Methyl Cellulose : water = 1 : 25) and water soluble solder mask (*wonderMask* - W washable Solder Mask 2205). It was advantageous to use them because the layer can be built by spin-coating. Water soluble glue was easily spin coated at 4500 RPM. However, it was difficult to degas after mix, so there was undesired bubbles as shown in Figure 3 left. And the water soluble glue was attacked by acetone; this made the water soluble incompatible with conventional photolithography. Water soluble solder mask is a more appropriate candidate for the release layer in that it remains intact in IPA and acetone. The viscosity of the product seems to be high for the spin-coating as shown in Figure 3 right, but it can be thinned by DI water. The etch rate and the compatibility with other litho process was not fully studied in this project due to the time limit. Even if it survives other process, the wet etching has an intrinsic issue of stiction. Thus, if the user's process is sensitive to stiction, then the dry etching method would still be the best option.

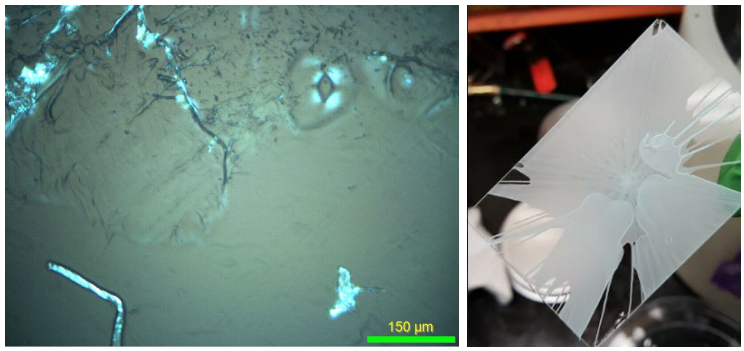
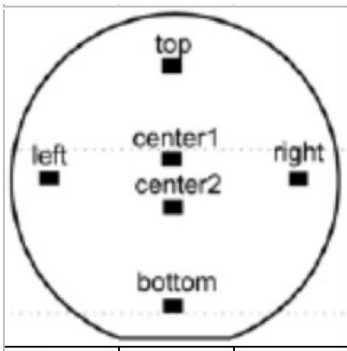


Figure 3. Water soluble glue (left) has degas problem; solder mask (right) need to be thinned for spin-coating.

Wafer Preparation for Dry Release

After deciding the Ge release method and XeF_2 dry etching process, the first step is to prepare the wafer with Ge sacrificial layer and SiO_2 etch-stop layer. The SiO_2 underneath the Ge is used to protect the Si wafer from attacking by XeF_2 when the Ge sacrificial layer is etched through. To make sure the Si wafer will not be etched by the dry etching gas, the SiO_2 must be thick enough. Thus a 1.5 um oxide layer was thermally grown directly on top of the Si wafer by LPCVD with tylanBPSG in SNF. The deposition program is LTO400PC and we ran 10 wafers for a set to measure the uniformity of the SiO_2 layers as a result of the CVD growth. The results are shown in the table below. Firstly, we selected the first, the fifth, the sixth, the tenth wafers and used nanospec to measure the SiO_2 layer on top of the Si by checking the reflection light. For each wafer, six points, including top, bottom, left, right, center1 and center2, are measured. The averaged uniformity per wafer is 2.27% and it is interesting to see that the edge SiO_2 is thicker than the center, likely due to different boundary conditions. The difference between the 10 wafers is 14.69% with the front end thicker and the back end thinner.



			Front First	Center 1	17727	Middle Fifth	Center 1	16558
				Center 2	17725		Center 2	16566
				Top	17445		Top	16349
				Bottom	18559		Bottom	16996
				Left	18402		Left	16985
				Right	18688		Right	17472
					Unit: Angstrom			Unit: Angstrom
			Standard Deviation	520.7536846	Uniformity	Standard Deviation	409.463063	Uniformity
			Average Value	18091	2.87852349	Average Value	16821	2.434237341
			Middle Sixth	Center 1	16206	End Tenth	Center 1	15189
				Center 2	16220		Center 2	15199
Average Uniformity Per Wafer	2.2737428	%		Top	16115		Top	15208
				Bottom	16619		Bottom	15502
				Left	16588		Left	15510
				Right	16839		Right	15988
Difference between 10 Wafers	14.694231	%			Unit: Angstrom			Unit: Angstrom
			Standard Deviation	290.3304439	Uniformity	Standard Deviation	311.0084672	Uniformity
			Average Value	16431.16667	1.766949662	Average Value	15432.66667	2.015260706

Table 1. Thickness results of the SiO_2 deposition.

Ge was then deposited by e-beam evaporation with innotec at 5e-7 torr pressure. 100 A chromium was firstly grown as the adhesion layer with a deposition rate of 0.5 A/sec followed by a 3000 A germanium grown at 2.2 A/sec.

Polyimide Patterning

Many flexible devices use the polyimide as their substrate because of its flexibility and compatibility with photolithography processes. The conventional polyimide (PI) patterning process uses O_2 plasma etching which can build in a fine resolution. However, it requires multiple steps to pattern, i.e. photoresist -> exposure -> development -> metal mask deposition -> liftoff -> O_2 plasma -> and metal stripping. Here, we suggest two fast prototyping methods for PI patterning: photopatternable PI and photodefinable PI.

Photopatternable PI (PI 2545) is patterned as the overlying photoresist is etched by developer (Figure 4). Because it etches as development process, it is simple and fast compared to the conventional approach. However, because the developer etches PI isotropically, it has undercut and consequently its resolution is worse than O_2 plasma etching. The undercut raised the need of well tuned dose of exposure and time duration of development. These two factors will be discussed in the following section. The photopatternable PI layer preparation is as follows: 1. spin coat adhesive promoter (VM-652) at 5000 RPM for 20 sec. 2. thin the PI 2545 by T9039 (PI 2545 : T9039 = 1:2) and spin coat at 2000 RPM for 60 sec. 3. heat the wafer at 140 ˚C on a hot plate for 10 min.

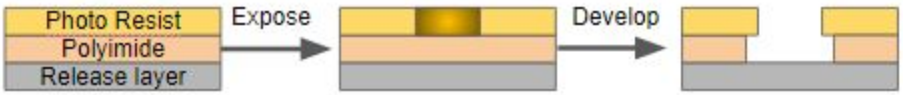


Figure 4. Process diagram for photopatternable polyimide

Photodefinable PI (HD-4110) is patterned by exposing on the PI layer and develop (Figure 5). Because the process does not need a photoresist, it is much simpler than other PI processes. And there is less undercut than photopatternable PI because the developer etches only the exposed PI patterns; thus photodefinable PI has finer resolution than photopatternable PI. HD 4110 can be spin coated conforming thicker layer (5 - 10 um), increasing the mechanical strength of the PI; this may prevent the aforementioned tearing from bubbles of wet etching. However, the use of HD 4110 in SNF was limited by its developer, PA401-D. We tested the SVG-Dev track developers (MF-26A (2%TMAH, base)) with HD-4110 but it made bubbles on the film (Figure 6). The future user of the photodefinable PI would need to develop manually with PA401-D. More detailed recipe can be found in [9].

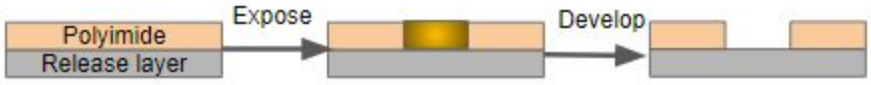


Figure 5. Process diagram for photodefinable polyimide

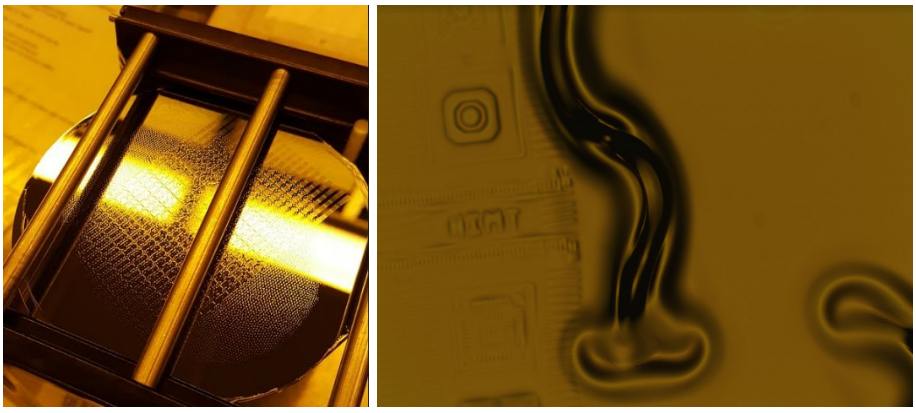


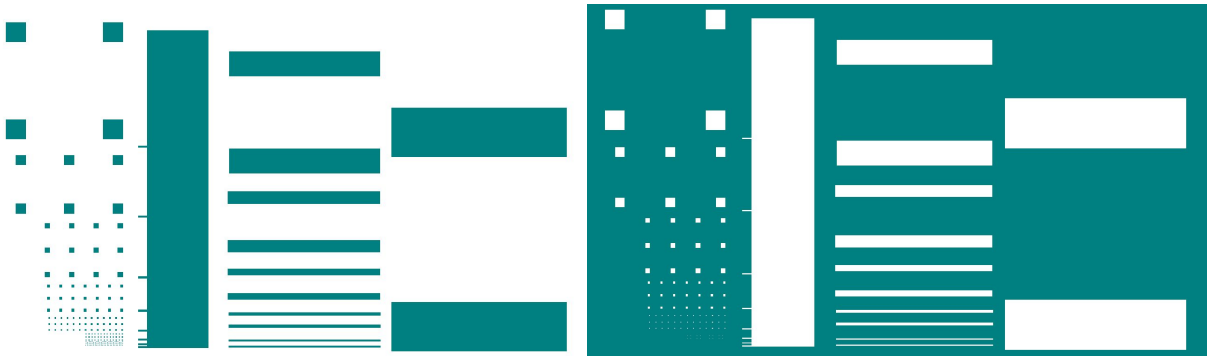
Figure 6. Photodefinable polyimide developed with SVG-DEV. MF-26A damaged the polyimide.

Photolithography

For the fast prototyping of different designs of flexible devices, we exposed the layers with Heidelberg, maskless exposure tool. The advantage of using Heidelberg is that users can change their design without the cost and time of ordering new photo masks. Moreover, the heidelberg has a software to expose with different dose and defoc values on a same wafer, so the users can easily figure out the appropriate setting of exposure from only one wafer.

It is also useful when researching different mechanical characteristics of flexible designs. We found a software ACE 3000 Translator ($75/month) that can translate 3D FEA simulation design into 2D GDS file which can be used in Heidelberg. This greatly improves the speed at which users can rapidly prototype structures.

In this project, we explored patterning photopatternable PI using Heidelberg. We used sample wafers comprised of SiO_2 & Ge wafer + photopatternable PI (~3 um) + photoresist (Shipley 3612 - 1 um). Dose and Defoc values were studied using test patterns as shown in Figure 7.



Positive Test **Negative Test**

Figure 7. Test patterns for dose matrix. The feature sizes are from 2 um to 128 um

The test patterns have both negative and positive counterparts of same design. Each design has squares and strips. The feature dimension spans from 2 um to 128 um. The initial design that we tried has circles instead of squares. However, the Heidelberg software can be overloaded when patterns include complex polygons. While the positive test pattern is a series of simple rectangles (or circles), the negative pattern is described by a more complex series of polygons that are created when the positive pattern is subtracted from an area. Circles are converted into polygons and can further amplify complexity. Future users should carefully test the limit of Heidelberg, especially if small arcs or circles included in negative spaces.

The dose and defoc values were tested by “series” exposure mode of Heidelberg software. The detailed instruction can be found from the Heidelberg user manual in SNF wiki. We tested Dose from 55 to 100 mJ/cm^2 (step size : 5 mJ/cm^2) and Defoc values -3 to 0. After exposure we used SVG-DEV, develop time to be 2 x 6 secs. We observed that 2um features were not fully exposed due to the Heidelberg resolution(~1 um). And Defoc from -3 to 0 did not make meaningful differences. So we suggest the defoc to be -2 as the typical users’ choice.

When the pattern was exposed with insufficient dose (70 mJ/cm^2 in Figure 8), there were green stripes over the patterns. From 75 mJ/cm^2 to 85 mJ/cm^2, there was no underexposed green stripes, but as exposed at higher the dose, the more undercut occured. The measure of the smallest feature size and its undercut is as Table 2.

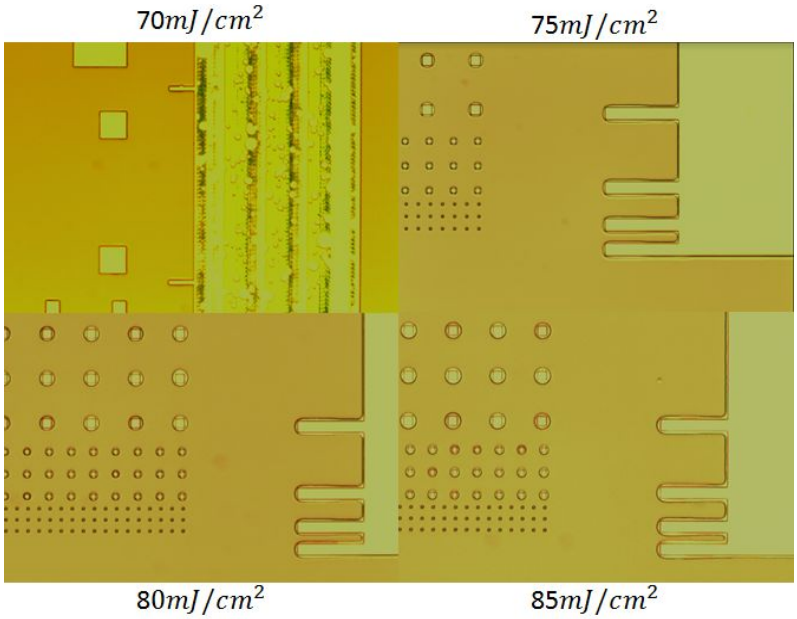


Figure 8. Microscope image for different dose value. The higher dose rate, the more undercut.

Table 2. Smallest possible feature size and undercut along the dose rate.

Dose(mJ/cm^2)	Negative	Positive
75	8um (undercut = 1.8um)	4um (undercut = 1.0um)
80	16um (undercut = 3.4um)	4um (undercut = 1.2um)
85	16um (undercut = 4.3um)	4um (undercut = 2.1um)

When we tested these dose rates with same develop time (2 x 6 sec) with flexible network patterns, we found that the develop response time of SVG-DEV over the wafer is not uniform; the center area etches faster than the peripheries. Given this fact, our suggestion for the future user of this process is to expose at 85 mJ/cm^2 and develop for 2 x 7 sec to ensure it develops all over the 4" wafer (Table 3). Note that this dose and develop time may vary by the thickness of each layer and the selection of sacrificial layer. If the layers contain any highly reflective material, i.e. aluminum, then the user should decrease the dose value than suggested.

Table 3. Suggested Dose and develop for Ge-SiO2 wafer + photopatternable PI

Dose (mJ/cm^2)	Develop time	Description
85	2 x 7 sec	Fully developed over 4" wafer, Undercut of 6.1 um (center), 2.5 um (periphery)

XeF_2 Release Characterization

Table 4. Xactix XeF_2 etch parameters (per cycle)

Etch Time	30 s
XeF_2 Pressure	3.0 T
N_2 Pressure	0.0 T
Vacuum Wait	0.0 s

XeF_2 dry etching of a sacrificial germanium layer was chosen as our release method for its high speed, clean, stiction free etching. We began with an established recipe on the Xactix tool (Table 4). Blue tape (commonly used in wafer dicing) is used to cover the backside of the wafer and front edges to protect the Si wafer while preventing excess consumption of XeF_2 (Figure 9).

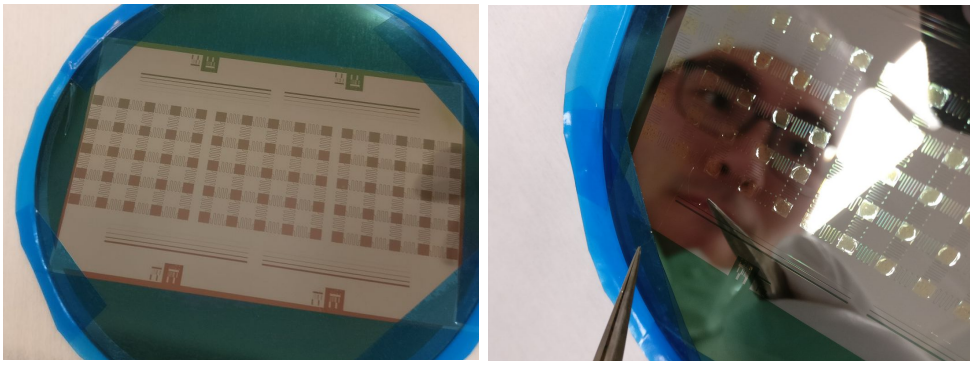


Figure 9. PI network structure before (left) and after (right) XeF2 etching of germanium.

To better understand the etch rates of this process, the parameters of this recipe were held constant while the number of etch cycles was varied from 10 to 40 cycles in 10 cycle increments. With each increment, we imaged the wafer to understand what size of features could be released. Figure 10 shows a representative image comparison of before and after a 10 cycle etch.

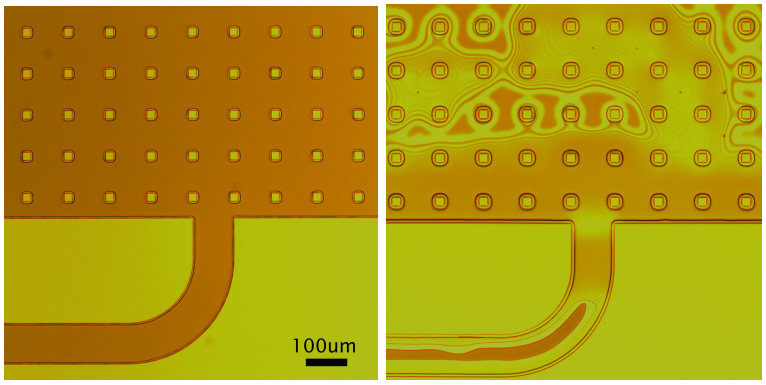


Figure 10. Polyimide plate before and after 10 etch cycles in the Xactix. The germanium is mostly removed from the square plate but remains beneath the connecting wire.

As the number of etch cycles increases, the process is able to release larger and larger structures (Figure 11). Using 100 um features as a benchmark, it can be seen that these features begin to release after 10 cycles, are mostly released after 20 cycles, and are completely released after 30 cycles. As a time reference, 30 etch cycles takes approximately 30 minutes to perform.

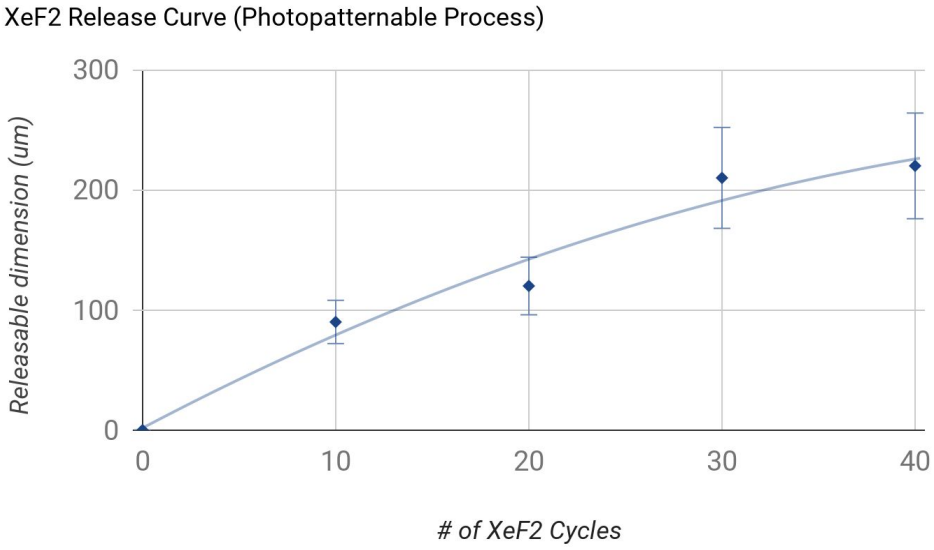


Figure 11. XeF2 release curve with error bars representing variability between structures on a single wafer.

It can also be seen that etch rate decreases as the number of etch cycles increase. It is possible that the thin, flexible nature of our PI layer contributed to this effect. As the germanium layer is etched, the released PI may be bending towards the substrate and inhibiting XeF_2 access to the remaining germanium (Figure 12). The impact of this type of mechanism could be reduced by using a thicker PI layer or designing a layer stack with minor compressive strain on the top surface.

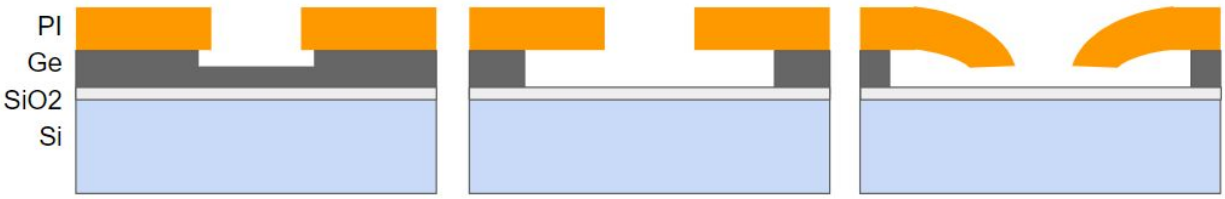


Figure 12. Theorized release progression through XeF_2 etching of germanium (left to right).

User Process Integration

The process developed in this report is intended to be compatible with standard cleanroom processes to enable the prototyping of a variety of flexible devices. Users can integrate their application specific processes directly on the patterned polyimide (Figure 13). XeF_2 is know to show desirable etch selectivity across a range of materials (Table 5). However, a second PI film can be patterned to encapsulate the devices in the case of concerns about device compatibility with XeF_2.

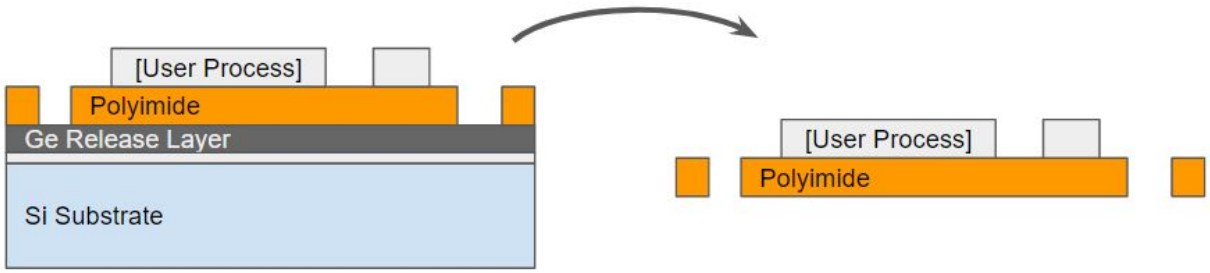


Figure 13. Release of user structures on a flexible polyimide backbone.

Table 5. XeF_2 etch selectivity as described in [10]

Etched Material	Conditionally Etch Materials (at elevated temp)	High Selectivity Materials	"Infinite" Selectivity Materials (i.e. not etched by XeF_2)		
			Metals	Compounds	Polymers/ Organics
Silicon	Titanium	Thermal oxide	Aluminum	PZT	Photoresists
Molybdenum	TiN	LTO	Nickel	MgO	PDMS
Germanium	Tantalum	Si_3N_4	Chrome	ZnO	C_4F_8
SiGe	TaN	Gold	Platinum	AlN	Silica glass
	Tungsten	Copper	Gallium	GaAs	Dicing tape
	TiW	SiC	Hafnium	HfO_2	PP
				TiO_2	PEN
				Al_2O_3	PET
				ZrO_2	ETFE
					Acrylic

Process Summary

Wafer Preparation

3. Purchase SiO_2 wafer
   > 1.5 um SiO_2

4. Deposit Ge
   Innotec E-beam Evaporator
   100 A Cr @ 0.5 A/sec
   3000 A Ge @ 2.2 A/sec

Pattern Photopatternable Polyimide

6. Spin-coat photopatternable PI
   Adhesion Promoter (VM-652) 5000 RPM, 20 sec
   PI2545 : T9039 = 1:2
   2000 RPM, 60 sec

7. Spin-coat photoresist (SPR 3612)
   Program 7
   1 um, w/o vapor prime, 2 mm EBR

8. Hotplate bake
   140 ˚C, 10 min

9. Convert FEA layout to GDS
   ACE 3000 Translator

10. Expose Photoresist
    Heidelberg
    85 mJ/cm^2

11. Develop wafer
    SVG
    2 x 7 sec

Release Devices

2. Dry etch Ge
   Xactix etch
   30 s/cycle 3 mTorr
   (30 cycles to release 100um features)

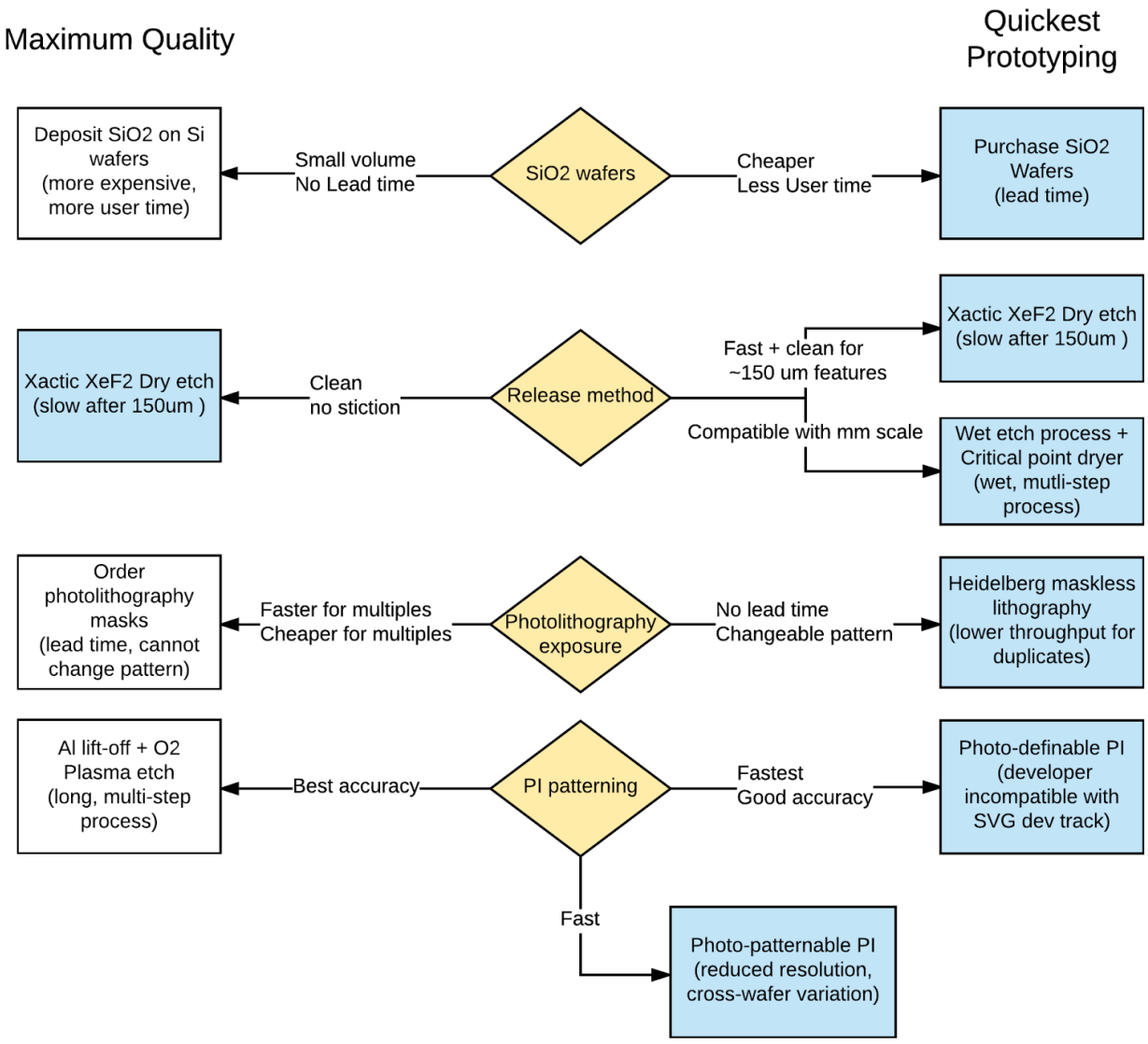


Figure 14. Summary of trade-offs between processes for flexible device fabrication. Processes highlighted in blue were developed in part during this course.

Conclusions

Results

In a high standard cleanroom such as SNF, time is equivalent to money -- every minute you wait in a process, every dollar you waste of an account. Therefore as a result of our process development, we made a comparison of the time and cost between the old methods and new methods of the four main processes, which can be shown in the following table.

Table 6. Comparison between the old method and the new method.

Main Process	Old Method	New Method	Time	Cost	Feature Size
Wafer preparation	LPCVD growth of SiO2 on Si wafer	Purchase SiO2 wafers	10 hrs → 4 hrs	$60/wafer → $49/wafer	N/A
Release method	Ge + XeF2	Ge + XeF2 + release facilitating holes	3-6 hrs → 1 hrs	$270/wafer → $60/wafer	N/A
Photolitho-graphy	KarlSuss Contact Aligner	Heidelberg MLA	Almost the same (2 min → 8 min/wafer)	Saved $500/mask	Almost the same (1 um vs 0.9 um)
PI patterning	PI2611+Al mask+O2 plasma	PI2545 photopatternable	10 hrs → 2 min	Saved ~$400/wafer	2 um → 20 um

In total, we have saved 10.5 hours and $620 per wafer with the new process we developed.

To demonstrate the flexibility and stretchability of our fabricated network, we stretched the network by manually pulling away two fixtures that connect to the two edges of the network in a constant speed alternatively. Noteworthily, the area of the stretched network has been expanded to over 25 times of its original area. Then the network was successfully integrated to a “finger” shaped 3D structure composed of a hemisphere and a cylinder as can be seen in Figure 15. This stretchable network serves as a platform to carry different types of electronics (sensors, switches, LEDs, etc.) to provide data information in real-time by integrating it with a wide variety of 3D structures for designated applications.

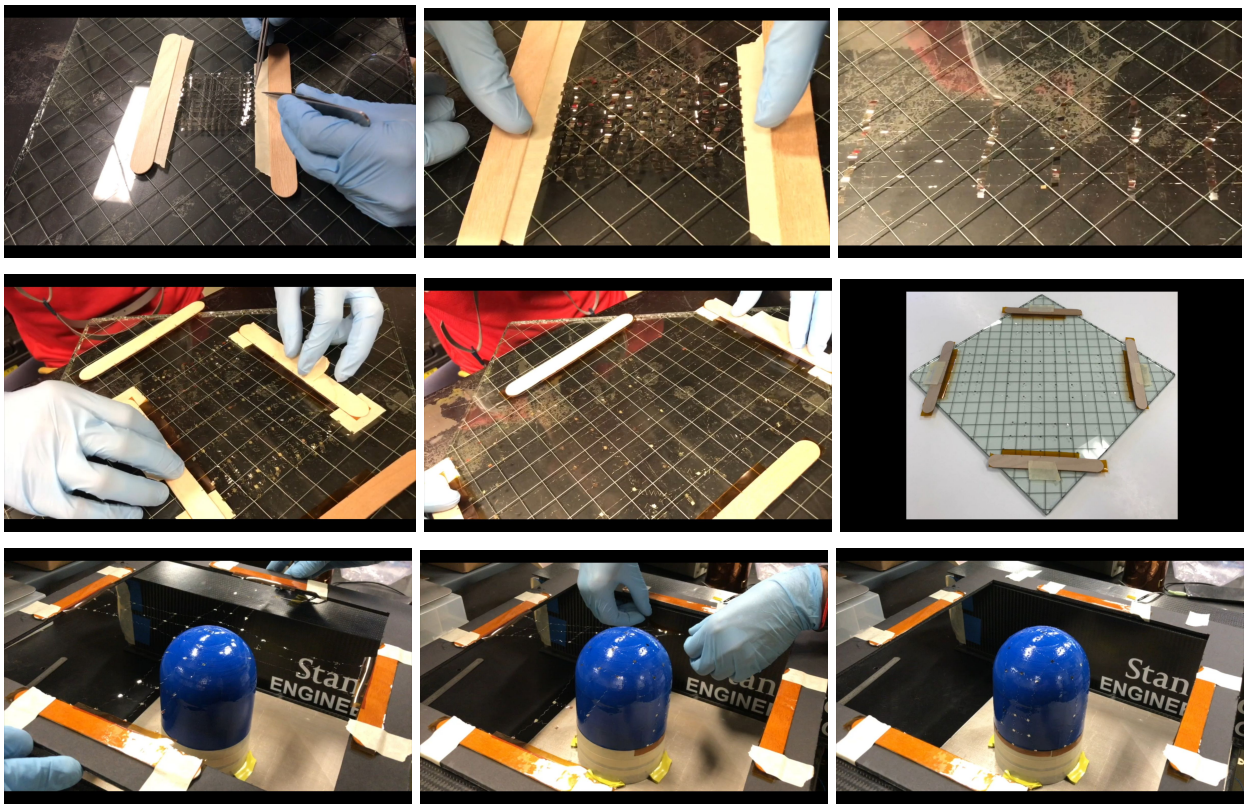


Figure 15. Network stretching and integration.

Future Work

The methods described in this project provide a great starting point for the development of flexible electronics.

Due to the time constraints of this course, we were unable to investigate a photodefinable polyimide process. However, we believe that this type of process would be almost as fast as the photopatternable PI processes while providing improved resolution and cross-wafer consistency.

A current limitation of the existing process is that large areas require release holes to expedite the release. While release holes were utilized in our work, it would be useful to characterize the effect of release holes with varying dimensions and densities across structures. This understanding would enable users to implement minimally invasive release holes in their projects.

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