Silicon Nanowires Thermoelectric Device Process Development

ENGR 241 Project
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Research Report

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Abstract

Recently thermoelectric materials have attracted great attention on their uses for thermoelectric heating/cooling purposes, or thermoelectric generator with improved performance. It has been realized that various materials and processes with many different architectures have been developed with their feasibilities for suitable thermoelectric devices. Fabricating high-quality thermoelectric devices, however, is still challenging due to the poor device performance, which is the compromise between the parameters of the materials. Several factors in the figure of merit (ZT) should be improved to increase device performance. This report will introduce the fabrication process of silicon nanowires (SiNWs) thermoelectric devices for the enhanced thermoelectric performance by optimizing their structure, post doping concentration and top metal contact condition.

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1. Introduction

1.1. Motivation

Thermoelectricity is a direct way to convert the temperature gradient to the electrical potential difference. This has attracted the interest with their advantages of solid-state operation, high reliability, stability and low cost [1]. This environmentally friendly low-cost effect is especially important since almost 90% of the world's energy is generated by fossil fuel combustion with an efficiency of 30−40% and the rest is wasted into heat. Thermoelectric materials for devices play a significant role in their operations. The efficiency of thermoelectric materials can be described by a figure of merit (ZT) as seen in the equation below,

$$ZT = \frac{\sigma T S^2}{k_{lattice} + k_{electronic}}$$

From the above equation, the relationship between ZT and the physical properties of materials shows an ideal thermoelectric material should exhibit high electrical conductivity (σ) to minimize Joule heating, high Seebeck coefficient (S) to generate a large potential difference and low thermal conductivity (κ) to maintain temperature gradient between the hot and cold side of the device [2]. The first discovery of the thermoelectric materials was Be_2Te_3 by Goldsmid in 1954, and subsequently several telluride-based materials and alloys such as $Bi_xSb_{2-x}Te_3$ and PbTe-PbSe were also developed in thermoelectric devices and intensively studied due to their useful efficiencies [3-4]. However, telluride-based materials have some drawbacks including high cost, insufficient supply, and difficulty in mass production. Silicon (Si), which has advantages of low cost, earth-abundance, well-defined technology for mass production, is regarded as a promising candidate for the thermoelectric device. However, the use of bulk Si in the thermoelectric device is limited due to its relatively high thermal conductivity and the ZT value smaller than 0.01 at 300 K [5]. Until now, significant researches have been reported with nanostructured Si with the optimized thermoelectric behavior by tuning the diameter, length, doping concentration, surface roughness and porosity [5-8]. Nanostructured Si, especially Si nanowires (SiNWs) with its size below 300 nm, shows still better performance due to the size between electron mean free path (< 100 nm) and phonon mean free path (~300 nm), which contributes to lower lattice heat flow. Even if the performance of the SiNWs thermoelectric device is 100-fold ZT over bulk Si, there is still room for improvement in it due to its relatively low ZT value. Here, we will introduce the developed performance of the single and array of SiNW to increase the ZT value, optimizing porosity via metal-assisted chemical etching (MACE) and metal-assisted anodic etching (MAAE), boron post doping with spin-on-dopant material, and top metal contact with ohmic condition.

1.2. Project SOP objectives

We will develop the silicon nanowires (SiNWs) thermoelectric (TE) devices with high ZT and the optimal amount of porosity via metal-assist chemical etching (MACE) and metal-assisted anodic etching (MAAE) method to etch Si wafers patterned by sub-micron nanoimprint lithography (NIL) method. We will also optimize the boron post doping and top metal contact conditions, and finally measure the thermoelectric performance with the developed single SiNW and array of SiNWs. We will provide the standard operation procedures (SOPs) of MACE and MAAE etching method, boron post doping process and top metal contact process for SNF.

2. Experiment Methods

2.1. Process overview

The procedures of the development of SiNWs thermoelectric device are divided into two quarters, as shown in Fig. 1. The patterning, metal deposition and MACE have been done in the fall of 2019 and boron post doping and top metal contact formation have been done in the winter quarter of 2020, to finish the development process of SiNWs thermoelectric device.

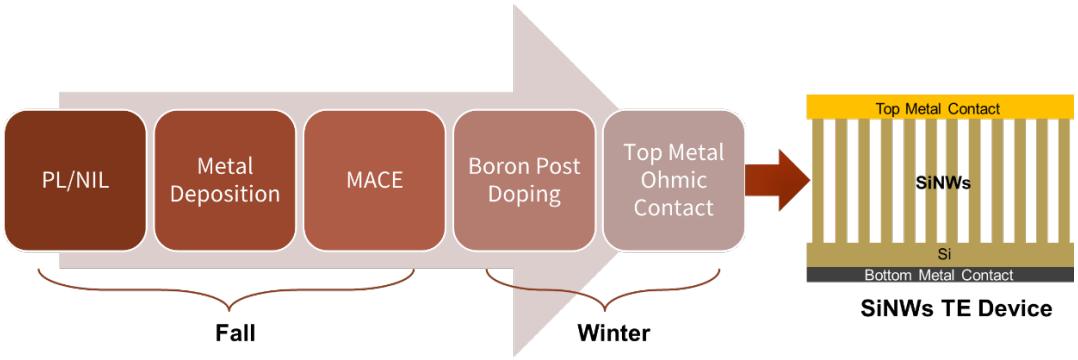

Figure 1. Workflow for the development of SiNWs TE device and schematic illustration of final SiNWs TE device.

2.2. Fabrication methods

The detailed standard operation procedures of MAAE, boron post doping, and top metal contact formation could be found in the appendixes I - III, and the schematics of the procedures are shown in Fig. 2, Fig. 3, and Fig. 4. Briefly, the fabrication started with a piece of Si wafer with SiNW fabricated on top using NIL MACE or MAAE method. The MACE condition is 4.8M HF with 0.2M H_2O_2 and the MAAE condition is 3.6M & 2.4M HF with 7mA/cm^2 applied current. The resulting SiNWs array was dip-coated with spin-on-dopant (SOD) purchased from the Filmtronics, which contains 2-2.5% boron by weight in the IPA solution. The SiNWs array with the coated SOD was then heated on 150°C for 1 min to evaporate the solution. Then the SiNWs array was put in a tube furnace at 950°C for 1 hr to anneal the SOD. The resulting SiNWs array was further coated with spin-on-glass (SOG) purchased from Filmtronics. The top few hundreds of the SiNWs were exposed after reactive ion etching (RIE). Finally, an Al metal film was evaporated on the exposed tip of the SiNWs array to form the top metal contact.

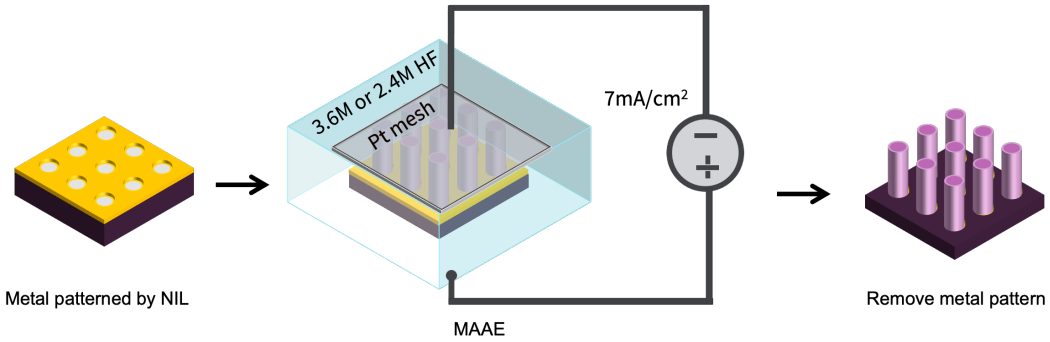

Figure 2. Schematic illustration of the SiNWs MAAE procedures.

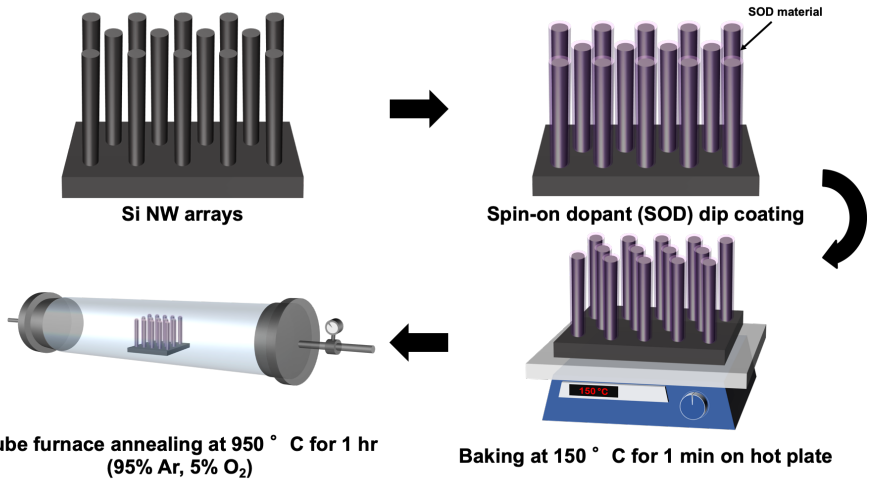

Figure 3. Schematic illustration of the SiNWs boron post doping procedures.

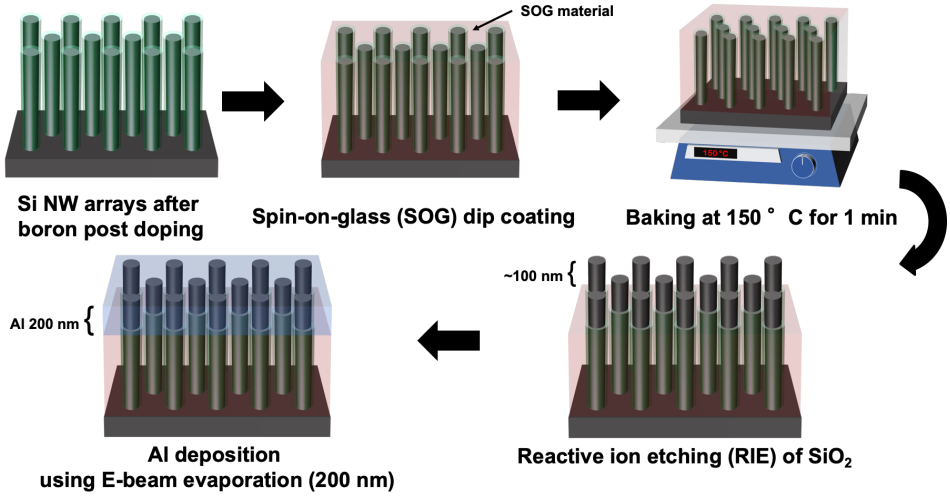

Figure 4. Schematic illustration of the SiNWs SOG filling and top metal contact formation procedures.

2.3. Characterization

The morphology of the patterned Si wafers, the etched SiNWs, the doped SiNWs and the filled SiNWs array with total metal contact was checked by scanning electron microscopy (SEM, Magellan, SNSF). The diameter and length of patterned pillars and etched SiNWs, and the thickness of the deposited metal were measured in SEM.

The thermal conductivity and electrical resistivity were measured by sonicating the SiNWs array in IPA for 5 s, picking up a single nanowire and dropping it on a fabricated measurement stage with 4 Pt electrodes. Contact between the nanowire and electrode was formed by Pt deposition, as illustrated in Fig. 5a and 5b.

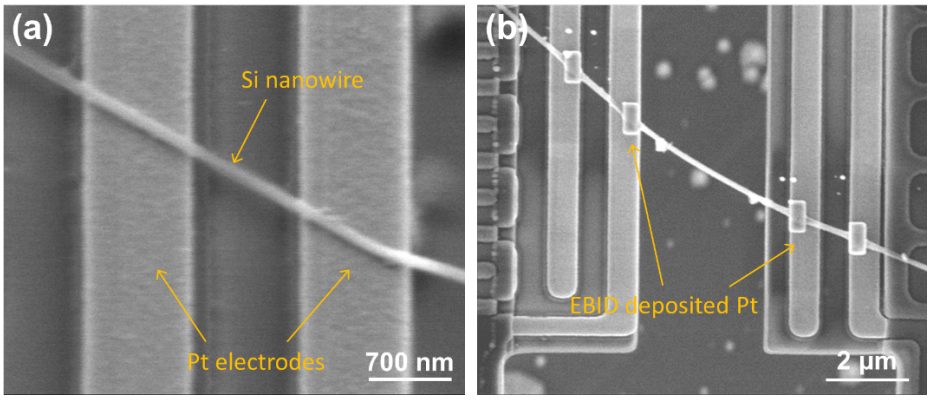

Figure 5. SEM images of (a) as-dropped Si single nanowire on Pt electrodes; (b) Si single nanowire on Pt electrodes after the formation of contact by Pt deposition.

3. Results and Discussion

3.1. SiNWs array patterning and etching

It was found in fall 2019 that the nanoimprint lithography (NIL) method is more repeatable and controllable than photo lithography (PL). Therefore, NIL is utilized as the only patterning method this quarter. The process and results of NIL are briefly discussed here, and more details can be found in our fall 2019 final report and SOP. Specifically, cleaned p type (5-10 Ωcm) and p++ type (0.005 Ωcm) wafer pieces with 1cm*1cm dimension are patterned using the NIL method to have 150 nm to 200 nm diameter circle arrays with 400 nm to 450 nm spacing in between. SOG material is used as the patterning layer and the PMMA is used as the lift-off sacrificial layer. After printing, a thick PMMA layer followed by the patterned SOG nanopillar layer can be observed on the Si wafers as shown in the SEM images in Fig. 6. While the resulting SOG layer on the top of PMMA nanopillar can be achieved by etching the SOG layer (200 W/45 sccm CHF_3, 15 sccm CF_4, 10 sccm O_2/75 mTorr/1 min/Oxford RIE) and the PMMA layer (300 W/50 sccm O_2, 10 sccm Ar/50 mTorr/90 s/Oxford RIE), as shown in Fig. 7.

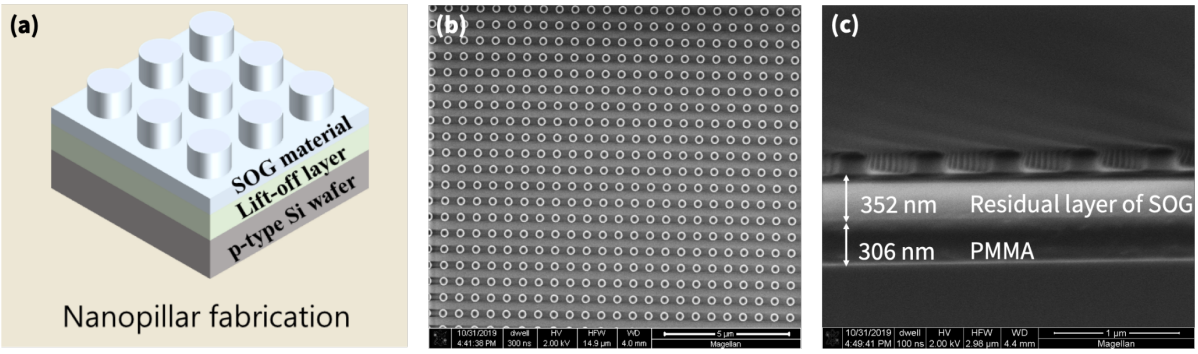

Figure 6. (a) Schematic of the SOG nanopillar layer and the sacrificial PMMA layer on Si wafer. SEM images of patterned SOG on the PMMA layer (b) top view and (c) side view.

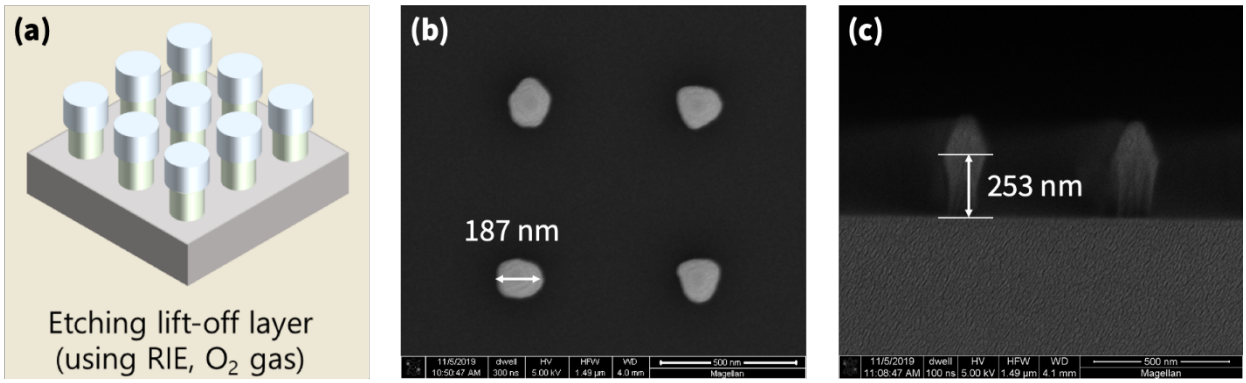

Figure 7. (a) Schematic of the SOG nanopillar layer and the sacrificial PMMA layer on Si wafer after RIE. SEM images of the after RIE patterned SOG on PMMA layer (b) top view and (c) side view.

Before the MACE or MAAE etching process, 60 nm of Ag and 20 nm of Au layers are deposited on the top of the dry-etched structures. Fig. 8 clearly shows that the PMMA lift-off layer is well separated from the bottom metal layer, which is essential to achieve a good lift-off pattern. The metal deposited wafers were dipped and sonicated in the dimethylformamide solvent to remove the lift-off layer. The resulting patterned Ag/Au layer after the lift-off on Si wafer is shown in Fig. 9. Fig. 9b shows that the 200 nm diameter hole pattern was achieved using nanoimprint lithography.

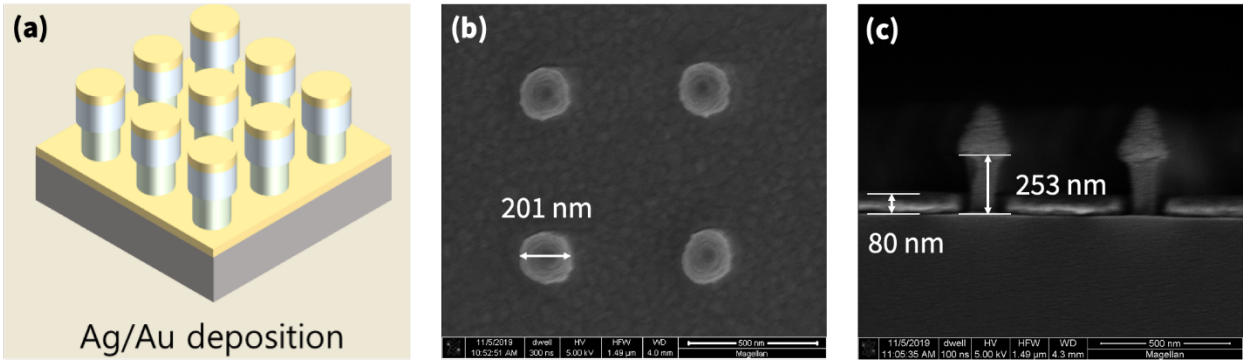

Figure 8. (a) Schematic of the SOG nanopillar layer and the sacrificial PMMA layer on Si wafer after RIE and metal deposition. SEM (b) top view and (c) side view images of patterned SOG on the PMMA layer after metal deposition.

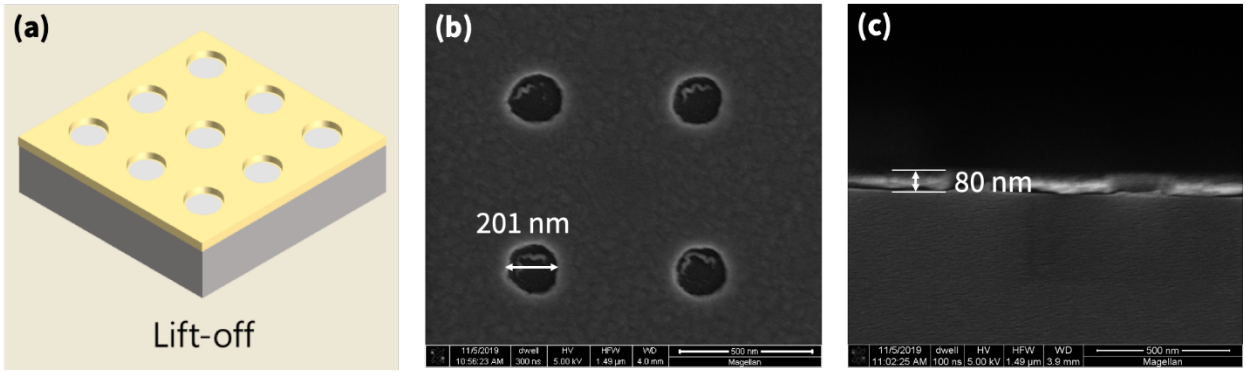

Figure 9. (a) Schematic of the lifted off metal layer on Si wafer. SEM (b) top view and (c) side view images of the lifted off metal layer on Si wafer.

The p type and p++ type Si wafers with metal layer patterned by NIL are put in the 4.8 M HF and 0.3 M H_2O_2 solution to fabricate SiNWs array by MACE. Some selective results of the SiNWs fabricated from the above two patterning method are shown in Fig. 10. The NIL patterned p-type SiNWs array shows an etch rate of ~ 15 μm/hr during the first hour of the MACE process, and it keeps an average etch rate of ~ 10 μm/hr over the 20 hr of etching. SiNWs array with a high aspect ratio (>900:1) is achieved, as shown in Fig. 10b. While the p++ type SiNWs array exhibits a relatively constant etch rate of ~ 13-15 μm/hr for 5 hr of MACE. For the MAAE process, the NIL patterned p-type wafer is etched in 3.6M or 2.4 M of HF solution with an applied current density of 7 mA/cm^2. SiNWs array etched in 3.6 M HF shows an etch rate of 10 μm/hr, which is higher than that of SiNWs etched in 2.4 M HF (8 μm/hr) (Fig. 11).

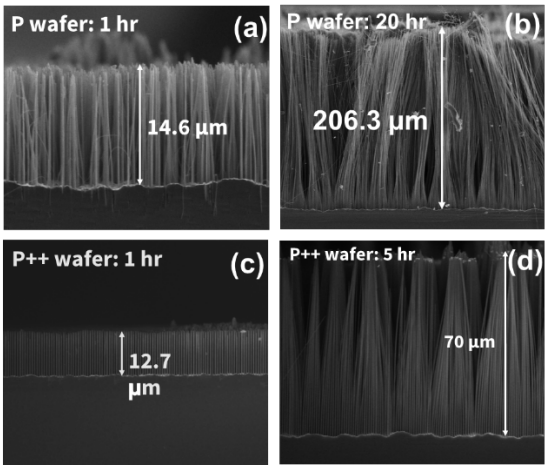

Figure 10. SEM images of SiNWs array fabricated by MACE with (a) 1 hr, p type wafer; (b) 20 hr, p type wafer; (c) 1 hr, p++ type wafer, (d) 5 hr, p++ type wafer.

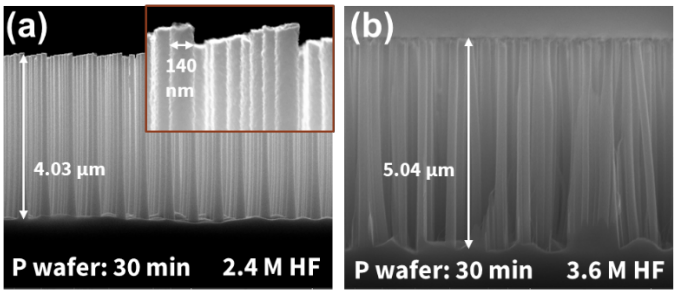

Figure 11. SEM images of SiNWs fabricated by MAAE with (a) 30 min, p type wafer, 2.4M HF; (b) 30 min, p type wafer, 3.6 M HF.

3.2. Boron post doping and thermoelectric characterization of single SiNW

SiNWs (NIL, 2 hr MACE) array is selected for the boron post doping process and subsequent thermal conductivity and electrical resistivity measurements due to its appropriate length, diameter, and porosity. The SiNWs array is dip-coated by SOD and baked to remove the solvent. 1 hr of annealing in a tube furnace (95% Ar + 5% O_2) at 950 ºC is enough for boron diffusion from coated SOD into SiNWs. To investigate the thermal conductivity and electrical resistivity of the doped SiNWs, the as-annealed array is dipped into 2 wt% HF solution for 10 min to remove the SOD residue (SiO_2) coated on the wire surface. The morphology before and after the residue clean step is shown in Fig. 12. The length and diameter of the nanowires remain consistent after the residue clean process. While the SOD removed SiNWs exhibit messy

alignment (Fig. 12b), it is still acceptable since this process is only needed for single nanowire measurement. For the final device of SiNWs array, the SiO_2 filling in the gaps of nanowires is desired, which will benefit the top metal contact formation.

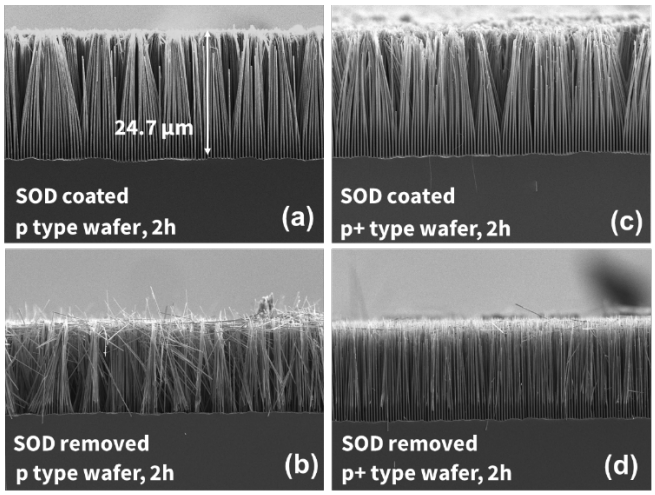

Figure 12. SEM images of SiNWs array after boron post doping and after SOD removal. (a) boron post doped p type SiNWs with SOD coating; (b) SOD removed p type SiNWs; (c) boron post doped p+ type SiNWs with SOD coating; (d) SOD removed p+ type SiNWs.

The measured thermal conductivity and electrical resistivity of representative SiNWs are summarized in Table 1. For undoped wires, both the p type and the p++ type SiNWs exhibit similar thermal conductivity because the porosity of the two types SiNWs are similar. The p++ type SiNWs show a higher electrical conductivity than the p type SiNWs due to the higher doping level of the original wafer. However, the electrical resistivity of the p and p++ SiNWs is much higher than that of the initial p and p++ wafer, which should be ~ 1e+1 and 1e-2 ohm·cm, implying the dopant lost during the fabrication process and the reduced electrical conductivity due to the porous structure. After boron post doping, SiNW fabricated from p type wafer shows an electrical resistivity of 2.7e-2 ohm·cm, which is lower than that of p type wafer. The corresponding doping concentration of this doped p type SiNW is ~ 1e+18 cm^{-3}. For boron post doped SiNW fabricated from p+ type wafer, the electrical resistivity is even lower, which is 5.4e-3 ohm·cm with a corresponding doping concentration of 1e+19 cm^{-3}. It should also be noted that the thermal conductivities of all these undoped and doped SiNWs are on the same order, which may suggest that the porous structure is retained after the boron post doping process. Therefore, it can be concluded that the boron post doping process can successfully increase the dopant concentration of the etched SiNWs without changing the morphology and porosity of nanowires, thus enhancing the electrical conductivity of the SiNWs.

Table 1. Thermal Electric Characteristics of the undoped and doped SiNWs

Sample (MACE NIL SiNW)	Thermal Conductivity (W/m·K)	Electrical Resistivity (ohm·cm)
312 nm diameter, P+	3.81	1275
259 nm diameter, P++	4.52	1.1
216 nm diameter, P, post doped	6.43	2.7e-2
168nm diameter, P+, post doped	4.37	5.4e-3

3.3. SiNWs thermoelectric device development

SiNWs (NIL, 1 hr MAAE) array is used to investigate the filling condition and top metal contact formation. As shown in Fig. 13a and 13b, SiNWs array can be filled by dip-coating concentrated SOG or SOD. The SiO_2 filled the gaps in the array, which provides mechanical support for the device. The top surface of the filled array is etched by RIE to remove the top SiO_2 film and expose the SiNW tip with a thickness of 100 nm (Fig. 13c and 13d). Then 200 nm of Al is deposited directly on the top of the exposed SiNW tips. Because of the support of the SiO_2 filling, Al forms a continuous film on the top, which is essential for the thermoelectric performance measurement of the final device. Therefore, the filling of SOD/SOG and subsequent RIE and metal deposition processes are effective to develop the thermoelectric device of SiNWs array.

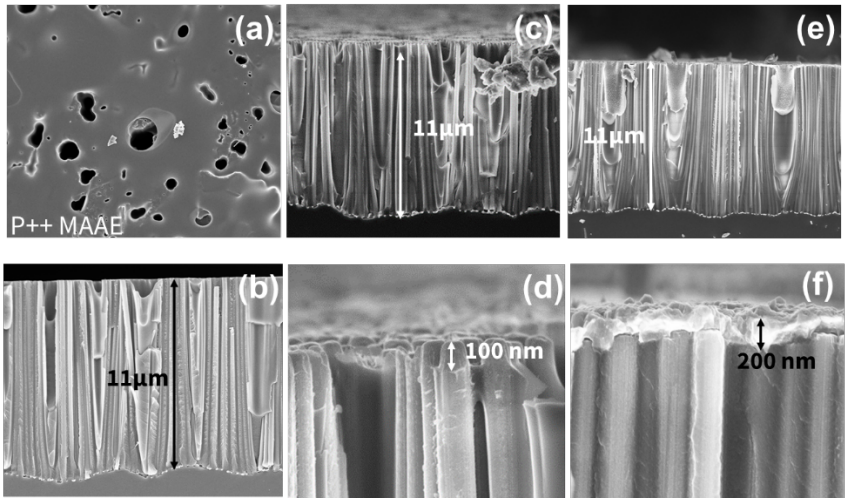

Figure 13. SEM images of SiNWs (a) with SOG filling (topview); (b) with SOG filling (sideview); (c) and (d) after tip expose; (e) and (f) after top metal contact formation.

However, it should also be noted that, when the same process is applied to the 400 µm SiNWs array with an aspect ratio of 1000 (Fig. 14), the exposed tip length is larger than 200 nm (Fig. 14b), which results in a discontinuous Al film on the top (Fig. 14d). This can be attributed to a thinner SiO_2 film left on the top of the filled array after SOG dip coating. Therefore, we need to further decrease the RIE time to reduce the exposed tip length, which is desired to be about 100 nm, thus achieving the final thermoelectric device by forming a continuous Al film on the top of the filled SiNWs array.

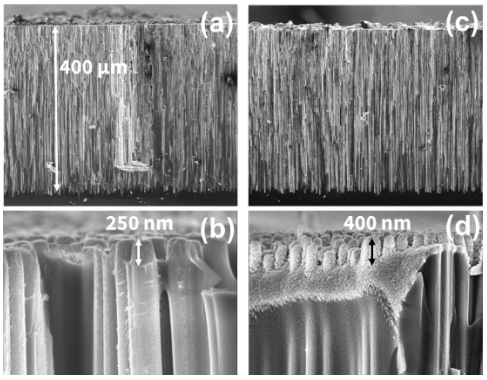

Figure 14. SEM images of SOG filled 400 µm SiNWs (a) and (b) after tip expose; (c) and (d) after top metal contact formation.

4. Conclusion and Future Work

In this project, we have developed the NIL process to pattern the Si wafer with good repeatability, refined the MACE and MAAE methods to fabricate SiNWs array with controllable morphology, developed boron post doping process to increase the dopant concentration, and thus the electrical conductivity, of the SiNWs without affecting the thermal conductivity, and created top ohmic metal contact on the fabricated SiNWs array, which is necessary for both the thermoelectric performance measurement and the requirement of practical use. As mentioned, the next step is to further refine the boron post doping and metal contact formation methods to develop the thermoelectric device of 400 μm SiNWs array and conduct thermoelectric performance measurement of the device using the Z-meter method (Fig. 15) [9], proving the feasibility of using SiNWs as the thermoelectric device with a relatively high ZT (ideally ZT >1).

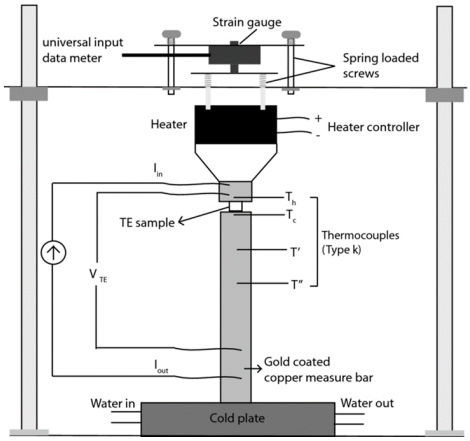

Figure 15. Schematic illustration of the Z-meter set up, which is used for thermal/electrical resistivity/conductivity measurement of SiNWs thermoelectric device at elevated temperature [9].

5. Reference

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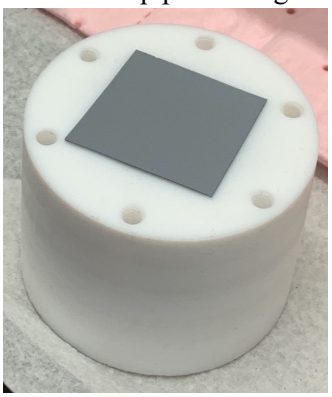
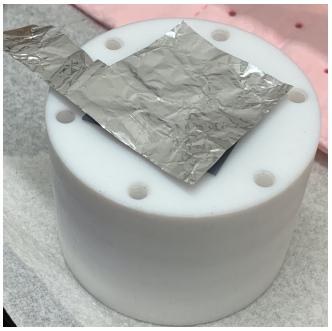
Appendix I. SOP for the SiNWs MAAE

1. Obtained the patterned Si with 15 nm Ag/ 5 nm Au on the top surface from the NIL patterning method.
2. MAAE in the reactor.
    a. Place the top part facing the cell opening.

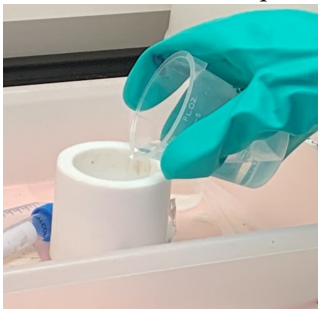


    b. Cut some Al foil to put on the back of the Si wafer as the back contact.

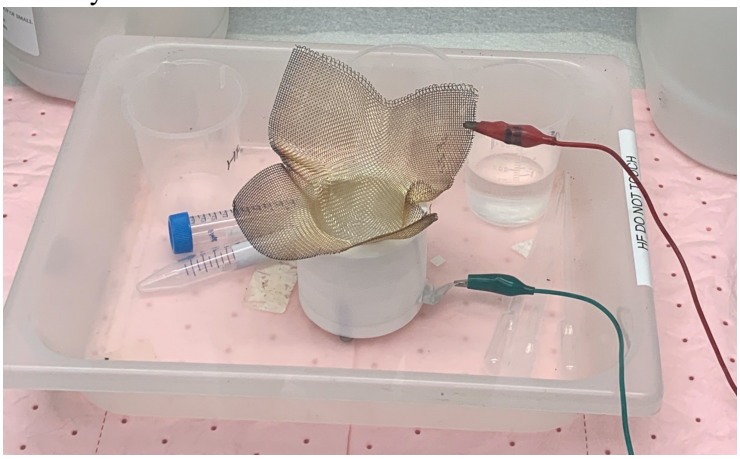


    c. Screw to secure the back of the cell firmly.

    d. Put the cell with the opening facing up. Pure the 3.6 M or 2.4 M HF solution into the cell.



e. Connect the anode to the Pt mesh and the cathode to the Al. Apply 7mA/cm^2 using a Keithley 2420 SourceMeter.

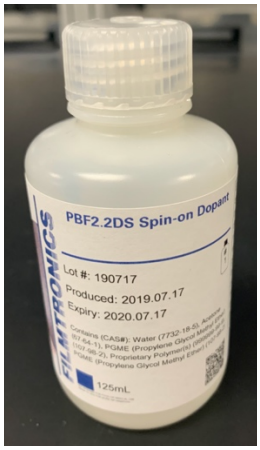


f. After 1 or 2 hrs. The vertically allied porous SiNWs array is obtained.
g. Store the SiNWs array after etching in IPA to avoid agglomeration.

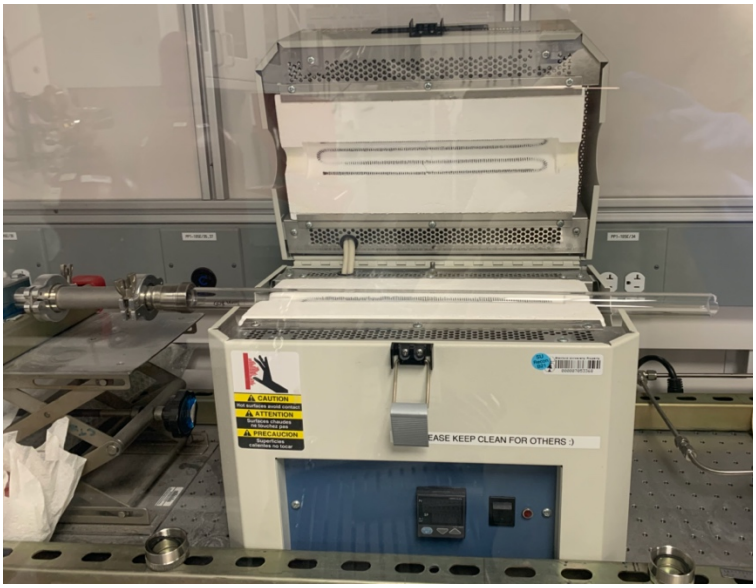
3. Critical point drying.
    a. Check valves, Fill 1.1/Bleed 0.14/Purge-Vent 0.15
    b. Press Chiller Power ON and wait for 30 minutes.
    c. Press Condenser Power and Chamber Power ON and wait for 3-5 minutes.
    d. Check inside of chamber lid, o-ring, inserts, and baskets for particles and rinse off particles using IPA.
    e. Place inserts in the chamber and use another wafer as a lid to prevent dirt on the sample.
    f. Press Vent and it will blink, and subsequently fill sufficient IPA to cover the wafers in the chamber.
    g. Transfer wafer and lower the chamber lid onto the chamber.
    h. Set purge time as 10 minutes.
    i. Press Cool and temperature will drop to 10 °C within 4 minutes. After that, press Fill and the pressure will go up to 800 to 900 psi. At this time, LCO2 will enter the chamber within 8 minutes.
    j. Automatic switch to Purge, Heat, and Bleed. During Heat light is on, the system will reach critical point, pressure and temperature will be 1072 psi and 31 °C, they will go up to 1400 psi and 40 °C.
    k. Automatically the pressure will decrease and switch to Vent around 360 psi.
    l. Open chamber and remove the wafer.

Appendix II. SOP for Boron Post Doping of the SiNWs Array

1. Dip coat the fabricated SiNWs in the SOD solution (shown below) for one time.



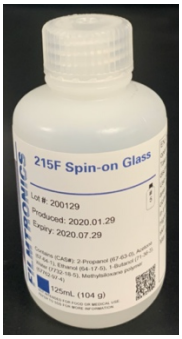
2. Bake at 150°C for 1 min on the hot plate to evaporate the SOD solution.
3. Put the SiNWs wafer piece into the tube furnace.



4. Supply 95% Ar (190 sccm) and 5% O2 (10 sccm) to flow through the tube. Set the furnace temperature to be 950°C. Leave the furnace at 950°C for 1 hour, and then cool down the furnace and take the SiNWs wafer out of the tube.

Appendix III. SOP for Top Metal Contact Formation of SiNW Array

1. Dip coat the SiNW after boron post doping in 10 wt% SOG solution (shown below) one time.



2. Bake the SiNW wafer on a hot plate at 150°C for 1 min to evaporate the solution.
3. Put the SiNW wafer in SNF Oxford RIE. Use the recipe of CHF_3: 45sccm, CF_4: 15sccm, O_2: 10sccm, and power: 200W for 20 min (etch rate: 118 nm/min) to expose the tip of the SiNWs array.
4. Use the SNF AJA metal evaporator to vertically deposit 200 nm Al with a rate of 5A/s on the tip exposed SiNW array.

Appendix IV. Expenses

The total budget of fall 2019 and winter 2020 is summarized in Table 2. We spent $ 1060 for equipment training in SNF, $ 5758.76 for equipment usage in SNF and SNSF and $ 2147.2 for materials and supplies purchase in SNF. In summary, we have spent $ 8965.96 by the end of the winter quarter of 2020, which is within our proposed budget of $ 9780.

Table 2. Budget of the ENGR241 (fall 2019 & winter 2020).

Budget			
Detailed Cost ($)	Training	Equipment Usage	Materials
	1060	5758.76	2147.2
Overall Cost ($)	8965.96		
Proposed Budget ($)	9780		
Remaining ($)	814.04		