Development of thermocompression and eutectic bond processes for pre-patterned substrates using the Finetech Lambda

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1. Abstract

The goal of this project is to find an optimized recipe of Au-Au thermocompression, Au-Si eutectic bond, and Au-Sn eutectic bond for pre-patterned substrates in the Finetech Lambda bonder. Since the development of effective heat exchangers for high power density applications requires 3D integration of microfabricated Si structures, we focus on thermocompression and eutectic bond for the 3D integration because it is a reliable bond process which can be done at low-temperature. Although there have been many studies about bonding process, the developed bonding methods are varied due to different experimental conditions and setups. Therefore, we aim to find effective thermocompression or eutectic bond recipes that are specifically applicable to the installed Finetech Lambda bonder in SNF during the quarter. Our investigation will discover the bond strength dependency on various bonding conditions such as type and thickness of bonding layer, bond temperature, bond pressure, bond time, and use of forming gas, etc. This work is important because the studied results will be used for future heat exchanger designs as well as other thermal management applications such as vapor chamber, thermal switch that are actively investigated in our group. In addition, the study will also help people who need to bond their microfabricated Si structures but don't want to go through high temperature process to protect their active electronic components in the Si structures.

2. Sample Preparation

2.1. Microfabrication

Fabrication Process (Top)			
Step #	Purpose	Process	Tools
1		Wafer clean	wbnonmetal
2		Adhesion Promotor	YES Oven
3		PR coating (Top)	SVGcoat2
4	Alignment Marks	Expose 1: Global + Contact Alignment (XPA/PM/Chip & Wafer Alignment)	ASML
5		Develop	SVGdev
6		Si etch	AMT etcher
7		Strip PR	wbnonmetal
8		Adhesion Promotor	YES Oven
9		PR coating	SVGcoat2
10		Expose 2: Island features	KarlSuss1
11	Patterning (1): Area of Bonding Interface	Develop	SVGdev
12		Descum	drytek2
13		Si etch	stsetch
14		Depth check	Nanospec/P2
15		Strip PR	wbnonmetal
16		Adhesion Promotor	YES Oven
17		PR coating	SVGcoat2
18		Expose 3: Embedded Channels	ASML
19	Patterning (2): Microchannels	Develop	SVGdev
20		Descum	drytek2
21		Hard Bake	Litho Oven
22		Curing	UV Cure
23		Si etch	stsetch
24		Strip PR	wbnonmetal
25	Metal Deposition	Ti/Au Ti/Au/Sn/Au	AJA-Evaporator Innotec
26		Au sputter/Au evaporation	Lesker Sputter Metalica

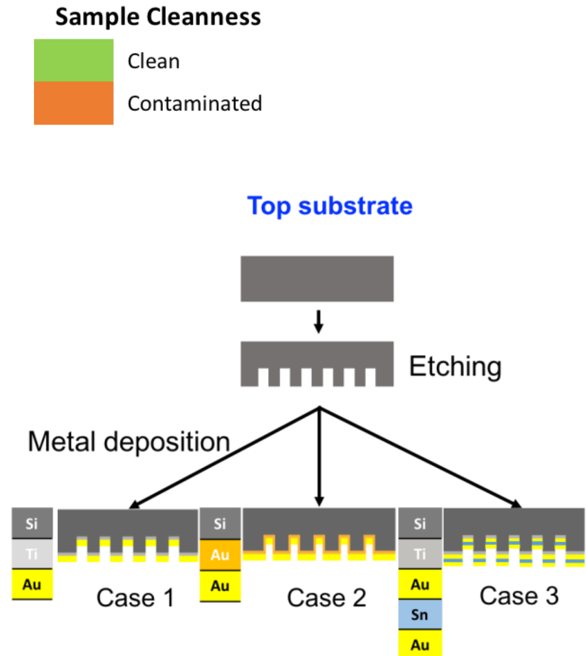


Figure 1. Fabrication steps of a top substrate

We have prepared top and bottom substrates for multiple chip-to-chip bonding trials in this quarter. Microfabrication process of top and bottom substrates consists of Si wafer clean and definition of alignment marks, deep Si etch, and metal deposition.

Wafers were cleaned in a fresh Piranha bath for > 20 min and a chip size was defined as 1.5-by-1.5 cm^2. Since the maximum force that is applied to a bonded substrate is 20 N in the finetech bonder, we implemented a square island structure per a top substrate chip, that is 0.9 – 1.1 µm high, and 5.4 mm wide, in order to apply bonding pressure of > 500 kPa to a bonded substrate. After we carefully defined the bonding area per a bonded substrate, microchannels on top and bottom substrates were patterned by deep reactive ion etch process (STS reactive ion etcher). Wafers for bottom substrates were oxidized in a 1000 ˚C furnace for 1.75 hrs to have 560 nm of thermal oxide layer. The thick silicon oxide layer on the bottom substrate acts as diffusion barrier that prevent gold layer from diffusing to silicon substrate. Therefore, it is possible to make the bond reaction occur only at top substrate side.

Metal layers were deposited on the etched microchannels as described in Figure 1 and Figure 2, and detailed geometric information of each case will be discussed later.

Although the bottom substrates are identical as shown in Figure 2, three different types of top substrates were fabricated. Case 1 through 3 in Figure 1 show material composition of each top substrate group. Case 1 and 2 samples were used for Au-Si eutectic bond trials and Case 3 samples were used for Au-Sn eutectic bond trials.

Fabrication Process (Bottom)			
Step #	Purpose	Process	Tools
1	Alignment Marks	Wafer clean	wbnonmetal
2		Adhesion Promotor	YES Oven
3		PR coating (Top)	SVGcoat2
4		Expose 1: Global + Contact Alignment (XPA/PM/Chip & Wafer Alignment)	ASML
5		Develop	SVGdev
6		Si etch	AMT etcher
7		Strip PR	wbnonmetal
8	Patterning: Microchannels	Adhesion Promotor	YES Oven
9		PR coating	SVGcoat2
10		Expose 2: Island features	KarlSuss1
11		Develop	SVGdev
12		Descum	drytek2
13		Si etch	stsetch
14		Strip PR	wbnonmetal
15		Depth check	S-Neox
16	Passivation Layer	Thermal Oxidation	thermoco-4
17	Metal Deposition	Ti/Au evaporation	Innotec

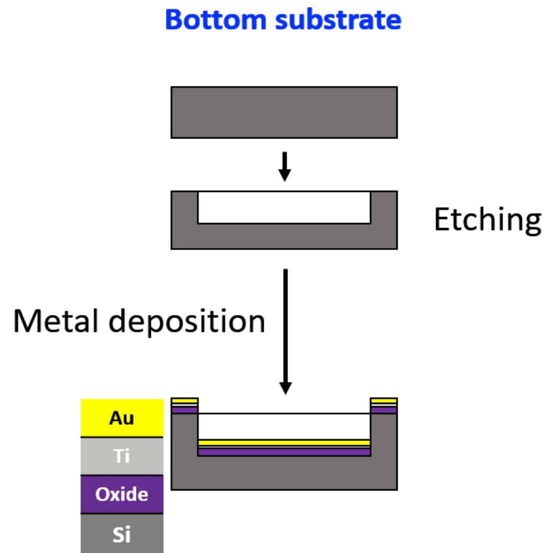


Figure 2. Fabrication steps of a bottom substrate

2.2. Sample cleaning

Cleaning steps

Step #	Process	Detailed Steps
1	Clean 1	a. Piranha: > 20 min b. 2% HF: < 1 min c. Dump rinse d. Spin-Rinse-Dry e. Megasonic clean
2	Metal Deposition	a. Evaporation b. Sputter
3	Clean 2	a. Spin-Rinse-Dry b. Megasonic clean
4	PR Coating	a. Manual PR coating b. Soft bake: 90 ˚C for 1 min c. Develop and hard bake
5	Dicing Wafers	-
6	Clean 3	a. SRS-100: 40 – 60 ˚C for > 20 min b. Manual rinse and dry c. Acetone/Methanol/IPA clean
7	Chip-to-chip Bonding	-
8	Bond Strength Characterization	a. Dicing test b. SEM (cross-section)

Figure 3. Specific sample cleaning steps and surface image

Bonding is sensitive to the surface cleanness and we have gone through a specific cleaning procedure described in Figure 3. First, we cleaned all the wafers in a fresh Piranha bath, 2% HF bath for > 20 min and < 1 min respectively to remove any organic matter and native oxide layer on the wafers. Megasonic clean was performed before and after metal deposition step because we do not want to introduce any small particle on the sample surface.

After metal layers were deposited on the wafers, we manually deposited positive photoresist layer on the wafers and went through soft-bake, develop, and hard-bake steps for preparing wafer-dicing step. One key finding is that SRS-100 is more effective to remove photoresist layer only if the photoresist layer is developed and hard-baked.

In Figure 3, the right image shows cleaned chip surface of a top and a bottom substrate. Although all the cleaning steps had been taken for cleaning, some of the samples still had small residues and it seems that those residues are from residual photoresist mask layer after DRIE step.

3. Experimental Results

We have tested three major bonding strategies, Au-Au thermocompression, Au-Si eutectic, and Au-Sn eutectic bonding strategies. Bond quality of each strategy has been characterized with 3 different methods, manual handling, wafer-saw dicing, and SEM image analysis. Among all 30 times of bonding trials, some selected samples had gone through the characterization methods. The samples that passed the manual handling test were diced in the DISCO wafer-saw machine and the cross-section of cut surface was imaged in the Sirion SEM system.
After the samples went through any bond quality test, the intact samples are marked as O and the broken (or delaminated) samples are marked as X in the test result table.

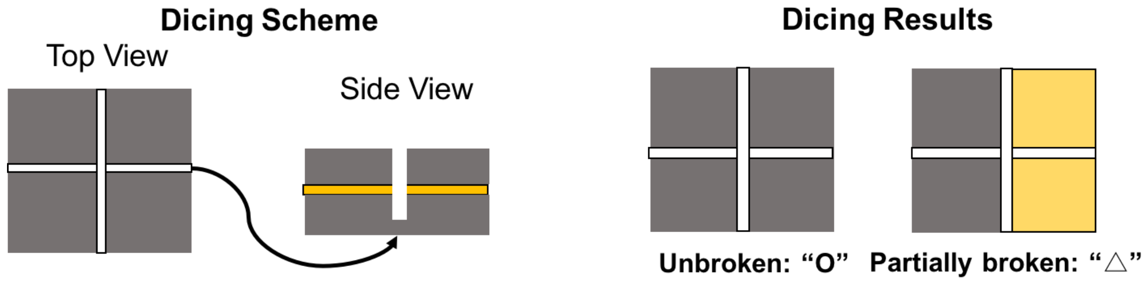


Figure 4. Dicing scheme and results

Some of the diced samples were intact but majority of them were partially broken, which means half or quarter piece of top substrate is delaminated (Figure 4). We marked partially broken samples as triangle after dicing test. The following test step is taking SEM images and these images will be discussed shortly.

3.1. Au-Au Thermocompression Bonding

Trial #	Substrate Type		Bond Parameters							Bond Results	
	Top	Bottom	$T_{uniform}$ [˚C]	$\Delta t_{uniform}$ [min]	T_{bond} [˚C]	Δt_{bond} [min]	dT_{ramp} [˚C/min]	N_2 Flow	Bond Type	Handling	Wafer-saw
1	B1	B2	200	10	300	15	180	N	Thermocompression	X	X
2	B2	B1	250	5	350	5	18	N	Thermocompression	X	X
21	B2	B2	X	X	379	50	60	N	Thermocompression	O	O

Substrate Design

B1,B2		B1,B2	
Si		Au	5010 A
Oxide	5670 A	Ti	271 A
Ti	271 A	Oxide	5670 A
Au	5010 A	Si	

Table 1. Bond quality test results of Au-Au thermocompression bonding

We have investigated conditions for Au-Au thermocompression bond and the test results are described in Table 1. The wafers for bottom substrates were diced and those diced chips were used for top and bottom substrates because we wanted to prevent Au from diffusing to Si. 20nm thick Titanium acted as an adhesion layer for Au layer.
According to thermocompression bond results, trial 21 showed the best bond quality among all three trials. We used highest bonding temperature (379˚C) and longest bonding duration (50 min) at trial 21 and the sample passed manual handling and wafer-saw dicing test. Following SEM images (Figure 5) show that there is one thin and bright layer between two Si bulk layers and it does not have any crack in the middle. Therefore, it seems that Au-Au thermocompression bond quality is improved by increased bond temperature and bond duration.

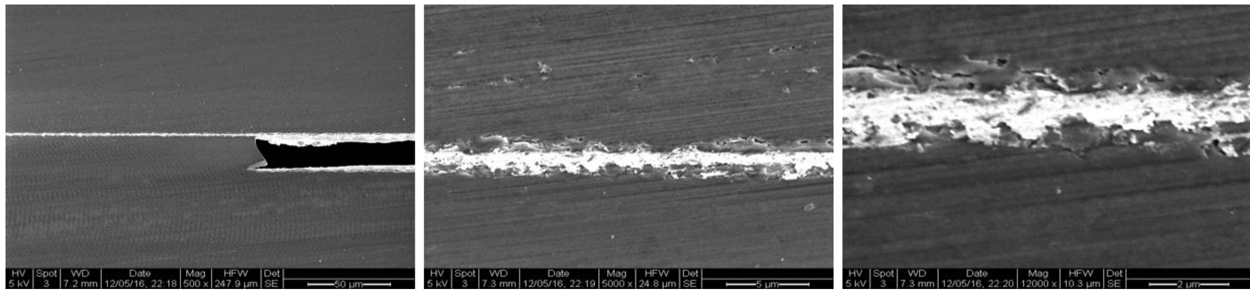


Figure 5. SEM images from trial 21

3.2. Au-Si Eutectic Bonding

Trial #	Substrate Type		Bond Parameters							Bond Results	
	Top	Bottom	$T_{uniform}$ [˚C]	$\Delta t_{uniform}$ [min]	T_{bond} [˚C]	Δt_{bond} [min]	dT_{ramp} [˚C/min]	N_2 Flow	Bond Type	Handling	Wafer-saw
6	T5	B2	300	5	379/400	20	20	N	Eutectic	O	∆
7	T3	B1	300	5	379/400	20	20	Y	Eutectic	X	X
23	T3	B3	300	5	379/400	20	20	Y	Eutectic	O	∆
25	T5	B3	300	5	379/400	20	20	N	Eutectic	O	∆

Substrate Design

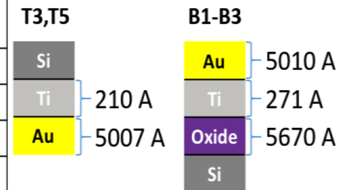


Table2. Bond quality test results of Au-Si eutectic bonding

There are numerous variables to explore for good Au-Si eutectic bonds and we mainly focused on 3 bonding conditions: the function of Ti layer with respect to its thickness, use of forming gas, and the bonding temperature. We fixed uniformity temperature, bonding duration, and temperature increase/decrease rate. Unfortunately, the flip-chip bonder is not able to maintain high temperature(> 380˚C) for longer than 2 minuntes, so we had to fix the bonding temperature at 379˚C.

The basic layer composition of top substrate is Si/Ti/Au, and that of bottom substrate is Si/Silicon Oxide/Ti/Au(Table 2). The thickness of each layer is listed in the figure in Table 2 and we only show one specific Ti thickness(21nm) in this report because there was no successful bond with thicker Ti thickness(50nm). It seems that 20nm of Ti layer works as a native oxide getter rather than a Si diffusion barrier because we have noticed Si precipitate in the bonding interface(Figure 6) which is similar to another SEM images published in E. Jing's paper(Figure 7). In both figures, silicon precipitates in the bonding interfaces are recognized. E. Jing, et al insisted that thin Ti layer worked as a native oxide getter and the bonding interface became thicker than the original Au layer thickness[1]. Also, they argued that diffused Si precipitates in the bonding interface are proofs of successful Au-Si eutectic bonding[1]. Hence, 20nm of Ti layer seems appropriate for Si to diffuse into Au layer for successful Au-Si eutectic bonds.

One thing to mention is that the sample from trial 7 was broken during manual handling despite the sample from trial 23 survived after wafer-saw dicing test. This may be due to non-uniform distribution of bonding pressure while the sample was mounted in the chip bonder. We found that if the position of bottom substrate is higher than the right focal plane, we may have a chance to apply higher pressure to one side than the other side of the sample. This issue will be discussed in section 4 in detail and we will suggest how to avoid it for future reference.

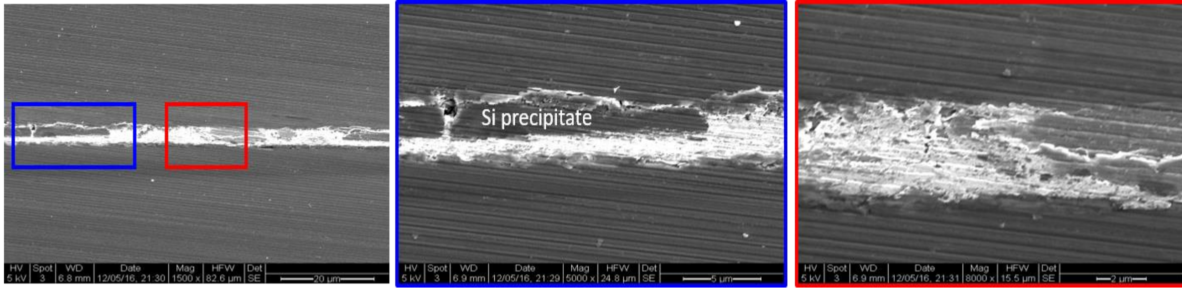


Figure 6. SEM images of trial 6

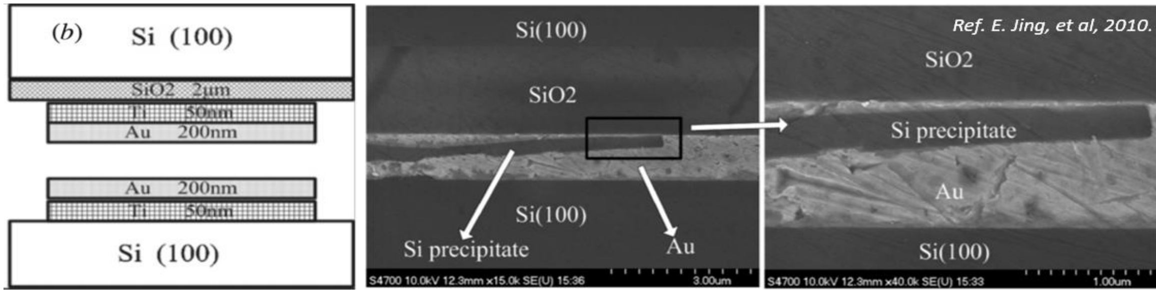


Figure 7. Bond layer configuration and SEM images of Au-Si eutectic bond from E. Jing, et al, 2010.

E. Jing, et al also insisted that there was non-uniform Au/Si reaction to create crater and non-crater regions if the native oxide layer was not removed by Ti [1]. The sample from trial 23 shows Au/Si mixed interface which seems similar to those SEM images of Au-Si eutectic bond interface from E. Jing's paper (Figure 8). We can also see a local crater in the sample from trial 23 which is filled with Au/Si mixture (Figure 8). The bond interface from trial 25 (Figure 9) shows three distinctive regions, mostly-Au, Au/Si mixture, and mostly-Si regions. The existence of these regions is due to anisotropic dissolution of Si into Au layer and the oxide layer between Si and Au tends to suppress the diffusion of Si into the Au layer [1].

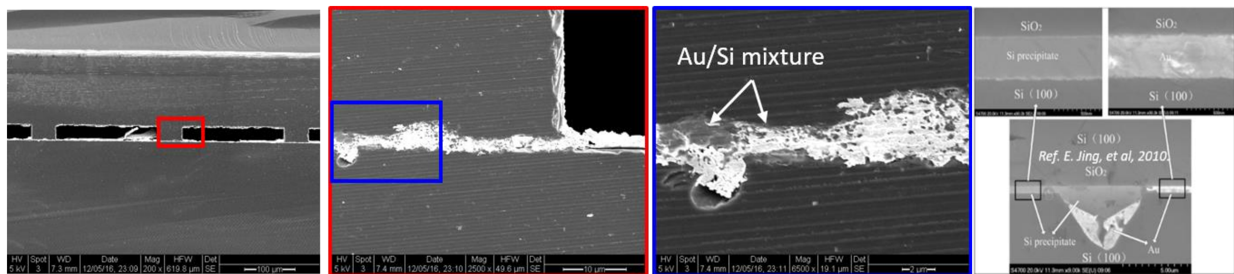


Figure 8. SEM images of trial 23 (three images from left), and that of Au-Si eutectic bond from E. Jing, et al, 2010 (right).

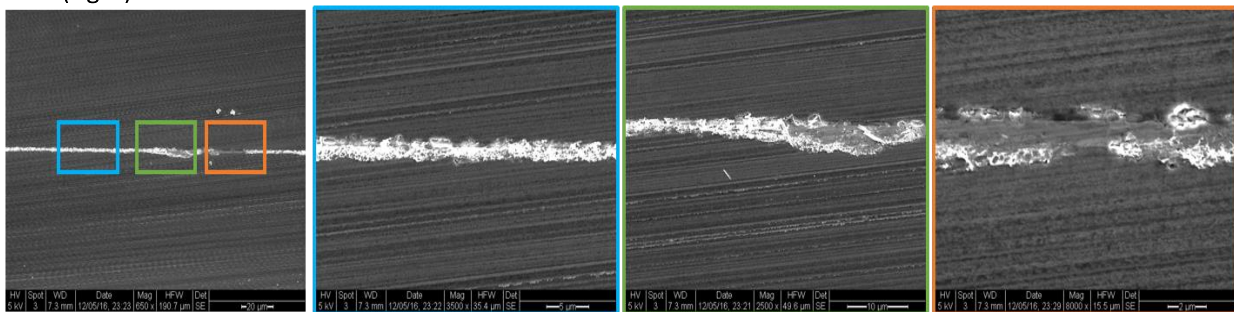


Figure 9. SEM images from trial 25

Samples from trial 23 and 25 show how N_2 gas flow affects the quality of bonding strength and it seems that N_2 gas flow is negligible to improve the bond quality. However, the number of trials is limited and there was no further effort to quantify bond strength of samples from trial 23 and 25, so it is hasty to conclude that N_2 gas flow would not affect the bond quality.

3.3. Au-Sn Eutectic Bonding

Trial #	Substrate Type		Bond Parameters							Bond Results	
	Top	Bottom	$T_{uniform}$ [˚C]	$\Delta t_{uniform}$ [min]	T_{bond} [˚C]	Δt_{bond} [min]	dT_{ramp} [˚C/min]	N_2 Flow	Bond Type	Handling	Wafer-saw
8	T11	B3	250	5	310	20	20	N	Eutectic	X	X
9	T12	B3	250	5	350	20	20	N	Eutectic	X	X
10	T12	B3	250	5	350	20	20	N	Eutectic	X	X
19	T12	B3	300	5	379/400	20	20	N	Eutectic	O	Δ
28	T11	B2	250	5	350	20	20	N	Eutectic	O	O
30	T11	B2	250	5	350	42	20	N	Eutectic	O	Δ

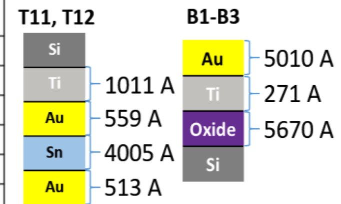


Table 3. Bond quality test results of Au-Sn eutectic bonding

We have also prepared another set of top substrates for Au-Sn eutectic bond and the layer configuration and thickness of each layer is described in Table 3. A thick Ti layer (101nm) was implemented between Si and Au layers which would stop Si from diffusion into Au. The thickness of Au and Sn layers were carefully calculated to satisfy Au:Sn eutectic ratio(Au:Sn = 80:20 wt%) and the actual thickness of those layers is listed in Table 3. The Au layer with 51nm thickness prevents further oxidation of Sn in air.

Samples from trial 8, 9, and 10 were easily broken and it is mainly due to non-uniform bonding pressure during bonding process. The other samples from trial 19, 28, and 30 showed much better bond quality because we carefully controlled the location of top and bottom substrates in order to uniformly distribute the bonding pressure over the sample surface.

We have tried different bonding temperatures, 350˚C and 379˚C(trial 19 & 28), and the lower bonding temperature showed better bond quality which is opposite to our expectation. The SEM images in Figure 10 shows the bond interface of sample from trial 19 and we can see a Au/Sn mixed layer uniformly distributed along the bond interface in general. However, Au/Sn layer at some specific regions is thicker than that at the other regions (center and right images in Figure 10) and it seems Au-Sn eutectic reaction occurred more heavily at those specific regions. This irregular reaction may cause non-uniform bond strength over the bond interface, therefore, we may expect poorer bond quality at higher bonding temperature(379˚C) than lower bonding temperature(350˚C).

We have also tried different bonding durations(20min, 42min) at the same bonding temperature, 350˚C, and shorter bonding duration showed better bond quality than longer bonding duration(trial 28 and 30 in Table 3). It may be due to non-uniform bond reaction correlated to the bonding duration. If there are some regions where active Au-Sn eutectic reaction occurs, longer bonding duration would have more chances to create Au-Sn overflow that seems similar to Figure 10.

One interesting finding is that there are multiple precipitates in the bond interface(Figure 6, trial 30) which look similar to Si precipitates. However, those precipitates are hardly Si precipitates because the bonding temperature is lower than Au-Si eutectic temperature(363˚C) and the thickness of Ti(101nm) is thick enough to prevent Si from diffusing to Au layer. Those precipitates may be remaining Sn grains which did not go through Au-Sn eutectic reaction but further investigation is needed.

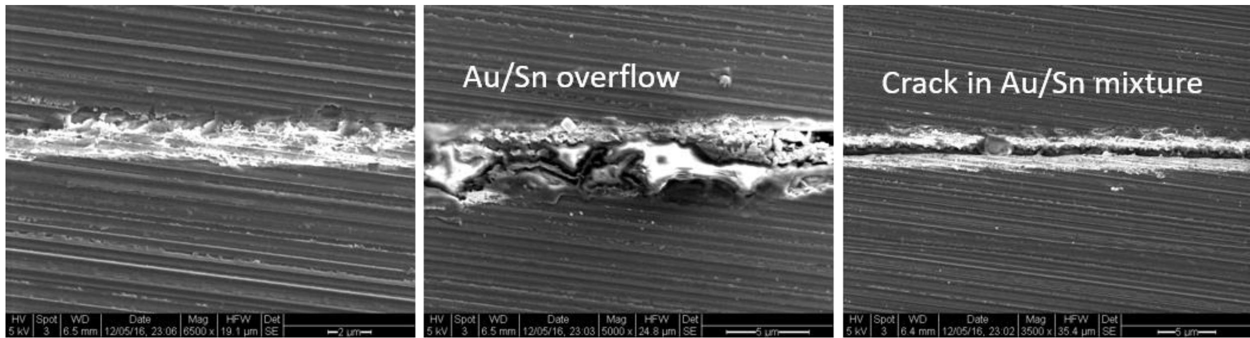


Figure 10. SEM images from trial 19

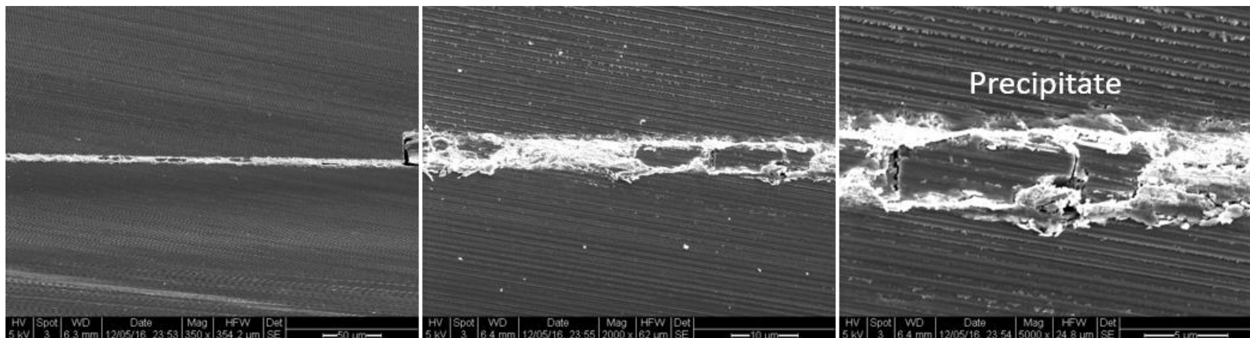


Figure 11. SEM images from trial 30

4. Non-uniform bonding pressure problem

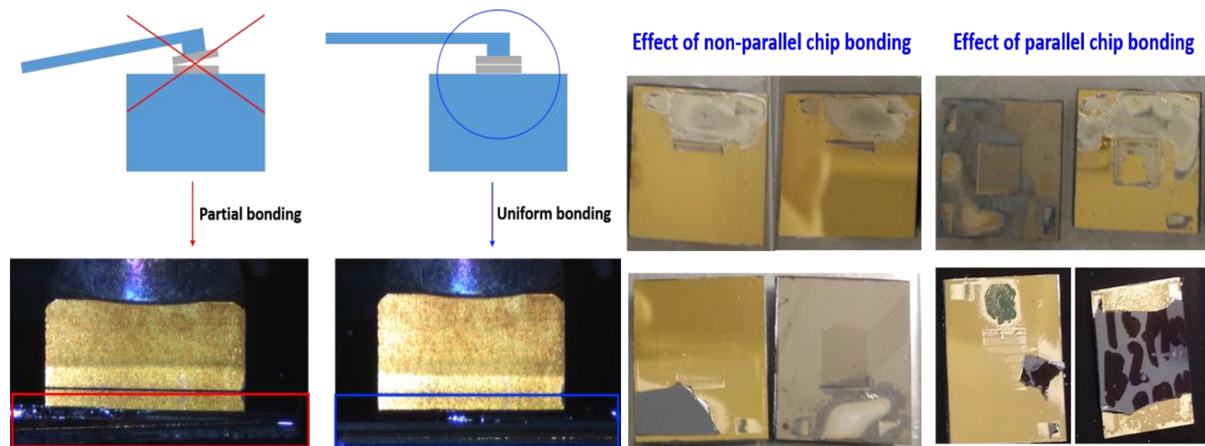


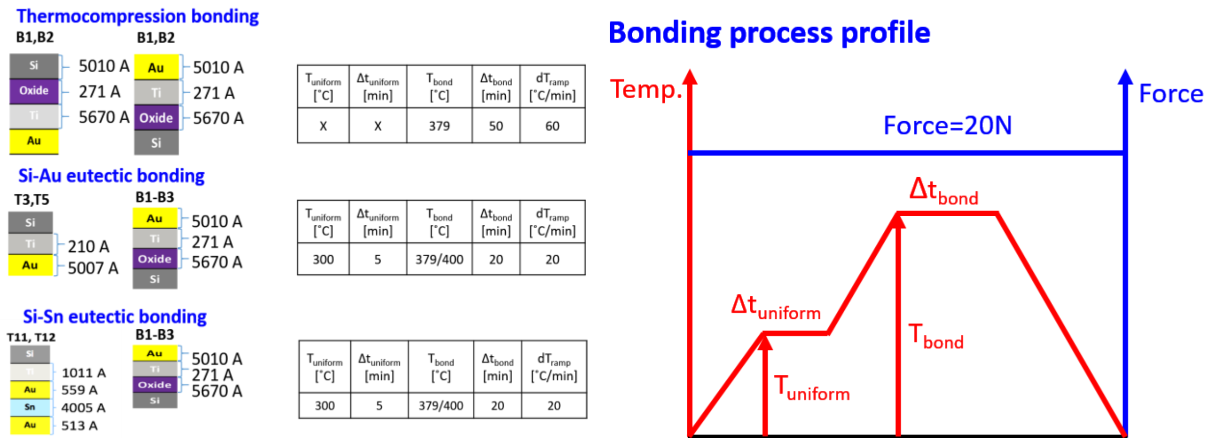
Figure 12. Configuration of partial and uniform bonding procedure and microscopic images of resulting bonding surfaces

The dislocated samples during manual handling are the samples where non-uniform bonding pressure is applied. When the bond interface is not parallel to the bottom chuck(red rectangle, Figure 12), we can see the bond reaction only at the region closer to the Finetech head arm(images on 3rd column from left, Figure 12). However, if the bond interface is parallel to the bottom chuck(blue rectangle, Figure 12) we can see that the area of bond reaction becomes wider(images on 4th column from left, Figure 12) and it means bonding pressure is distributed more uniformly.

One easy way to place top and bottom substrates in parallel is locating the bottom substrate slightly lower than the focal plane and raising it slowly until the bottom substrate hits the top substrate. Subsequently, the eutectic reaction occurs over the bond substrate more uniformly(images on 2nd column from left, Figure 12).

5. Suggestion of optimal bonding recipes

Based on results of our bonding trials, we suggest an optimal recipe of each bonding method that can be used in the Finetech flip chip bonder(Table 4). The applied force is fixed as 20N and it corresponds to > 500 kPa over the bonding surface. Values of other parameters are listed in table 4 and a brief schematic of bonding process profile is drawn to help your understanding.



$T_{uniform}$ [°C]	$\Delta t_{uniform}$ [min]	T_{bond} [°C]	Δt_{bond} [min]	dT_{ramp} [°C/min]
X	X	379	50	60

$T_{uniform}$ [°C]	$\Delta t_{uniform}$ [min]	T_{bond} [°C]	Δt_{bond} [min]	dT_{ramp} [°C/min]
300	5	379/400	20	20

$T_{uniform}$ [°C]	$\Delta t_{uniform}$ [min]	T_{bond} [°C]	Δt_{bond} [min]	dT_{ramp} [°C/min]
300	5	379/400	20	20

Table 4. Optimal bonding recipes and a brief configuration of bonding process

6. Summary

For the project, three types of bonding strategies have been tried to find optimal recipes. Based on the results of earlier bonding trials, we have analyzed how some of bonding parameters affect bond quality.

For Au-Au thermocompression bonding, bond quality seems to be improved by increasing bond temperature and extending bond duration. For Au-Si eutectic bonding, 20nm of Ti would work as a native oxide getter and we could notice improvement in the eutectic bond quality. But we could not see improvement in the eutectic bond quality when N_2 forming gas was used. For Au-Sn eutectic bonding, appropriate bond temperature and bond duration is recommended to improve bond quality. Although the number of samples is limited and there is no further effort to investigate quantification of bond strength, both of Au-Sn and Au-Si eutectic bonding strategies are applicable to real applications and further characterization of bond quality needs to be conducted. In addition, parallel chip bonding is essential for the applications that have large bonding area.

Acknowledgement

We appreciate our mentors (Prof. Roger T. Howe, Dr. Usha Raghuram, Dr. Mark Zdeblick, Dr. Roozbeh Parsa, Dr. Anthony Flannery), SNF staff members, and E241 classmates for giving us good feedbacks during the class as well as internal meetings. It was lucky for us to learn high-level skill sets for different types of chip-to-chip bondings for future reference.

Reference

1. Errong Jing, Bin Xiong, Yuelin Wang, *Low-temperature Au-Si wafer bonding*, J. Micromech. Microeng. 20, 2010.