Silicon Nanowires Thermoelectric Device Process Development

ENGR 241 Project
Fall 2019
Research Report

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1. Introduction

1.1 Motivation

Thermoelectric effect is attracting great interest for its potential applications ranging from temperature measurement, thermoelectric heating/cooling, and power generation. Thermoelectric devices can be used for the direct conversion of heat to electricity due to the Seebeck effect by using thermal sources including solar and waste heat. [1] This energy conversion is cost-effective and environmentally friendly, especially since almost 90% of the world's energy is generated by fossil fuel combustion with an efficiency of 30−40% and the rest is wasted into heat. The desired thermoelectric figure of merit (ZT) should be $\geqslant$1 to obtain a conversion efficiency of >10%. [2] According to the relationship between ZT and the physical properties of materials (Eq. 1)

$$ZT = \frac{\sigma T S^2}{k_{lattice} + k_{electronic}} \quad \text{Eq. 1}$$

, an ideal thermoelectric material should exhibit high electrical conductivity (σ), high Seebeck coefficient (S) and low thermal conductivity (k). [1] Telluride-based materials such as Bi_2Te_3 and PbTe are widely used in practical thermoelectric devices and intensively studied due to their high conversion efficiency. [3] However, telluride-based materials are not suitable for large-scale energy applications due to their high cost, insufficient supply, and difficulty in mass production.

While silicon (Si), which has the advantages of low cost, abundant earth reserves, matured manufacturing technology for mass production, is regarded as a promising candidate for the thermoelectric device. The application of Si in thermoelectric device is quite limited due to its relatively high thermal conductivity and the ZT of bulk Si is even smaller than 0.01 at 300 K. [4] Since most of the thermal energy within Si is transported by the lattice vibration rather than by electrons and holes, it is possible to reduce the thermal conductivity and thus increase the ZT of Si if the dimension of Si structure is below the mean free path of phonon, which is about 300 nm. [5] Many people have investigated the thermoelectric performance of nanostructured Si and tried to optimize the thermoelectric behavior by tuning the diameter, length, doping concentration, surface roughness and, porosity. [4-7] However, most of the reported nanostructured Si materials still have a relatively low ZT and there is still room for improvement. And most of the previous works focus on the performance of lab-scale samples, such as single nanowire or thin film of a small area, there still needs more efforts to develop controllable fabrication method of whole-wafer-large Si nanowires (SiNWs) array and make the SiNWs array a device. The thermoelectric performance of the device should also be further enhanced to meet the requirements of practical use.

1.2 Project SOP objectives

We need to develop Silicon nanowires (SiNWs) thermoelectric (TE) devices with high ZT and the optimal amount of porosity via using metal assist chemical etching (MACE) method to etch Si wafers patterned by sub-micron nanoimprint lithography (NIL) or photo lithography (PL) method.
We need to develop the standard operation procedures (SOP) of sub-micron NIL and PL patterning method and high aspect ratio SiNWs MACE fabrication method for SNF.

2. Experiment methods

2.1. Process overview

The procedures of the development of SiNWs thermoelectric device are divided into two quarters, as shown in Fig. 1. The patterning, metal deposition and MACE have been done in this fall and boron post doping and top metal contact formation will be explored in the winter of 2020.

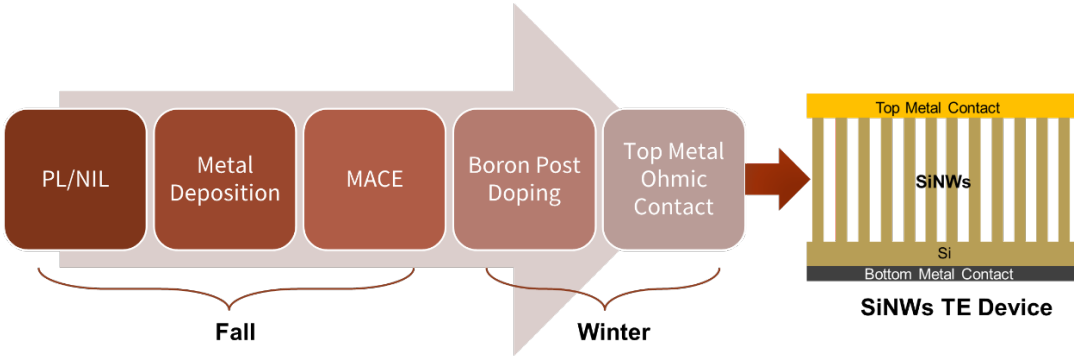

Figure 1. Workflow for the development of SiNWs TE device and schematic illustration of final SiNWs TE device.

2.2. Fabrication methods

The detailed standard operation procedures of nanoimprint lithography (NIL), photo lithography (PL) and metal assisted chemical etching (MACE) could be found in the appendixes I - III, and the schematics of NIL and PL procedures are shown in Fig. 2 and Fig. 3. Briefly, the fabrication started with a piece of Si wafer ranging from p type to p++ type. The pattern of lift-off pillars with undercut shape or straight sidewall was achieved by NIL or PL with desired dimensions. The patterned wafers were then deposited with metal catalyst (Ag and Au) with a total thickness of 80 nm. After metal deposition, the lift-off pillars were removed, and the patterned wafer was proceeded to etch step via MACE. Finally, the metal residues in the as-fabricated SiNWs array were removed and the thermoelectric properties of single nanowire were measured.

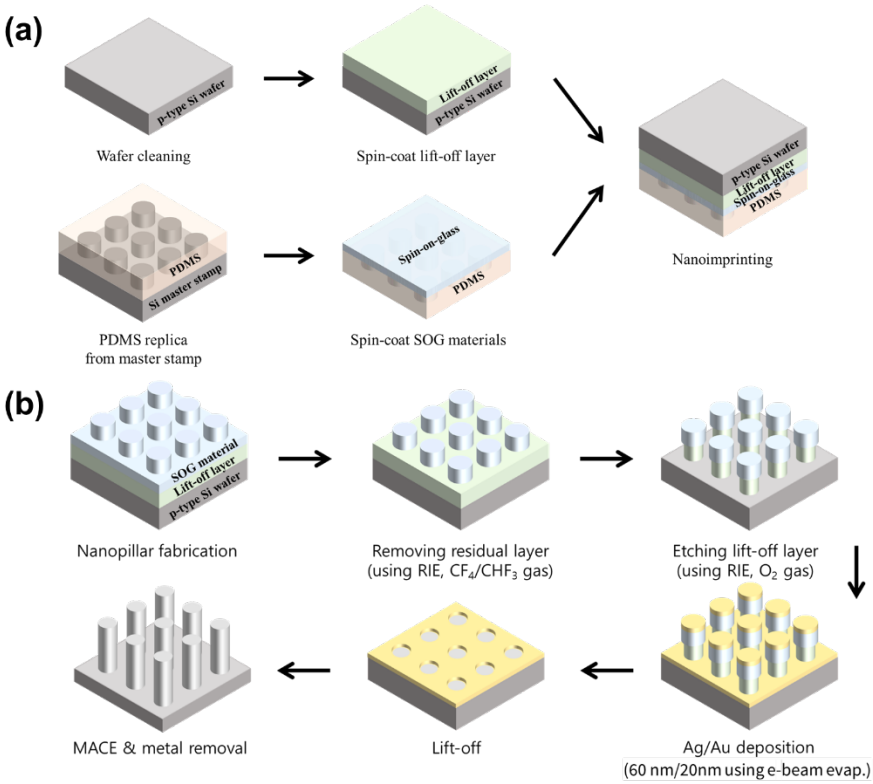

Figure 2. Schematic illustration of the SiNWs fabrication by NIL patterning method and MACE. (a) NIL procedure; (b) RIE, lift-off, and MACE.

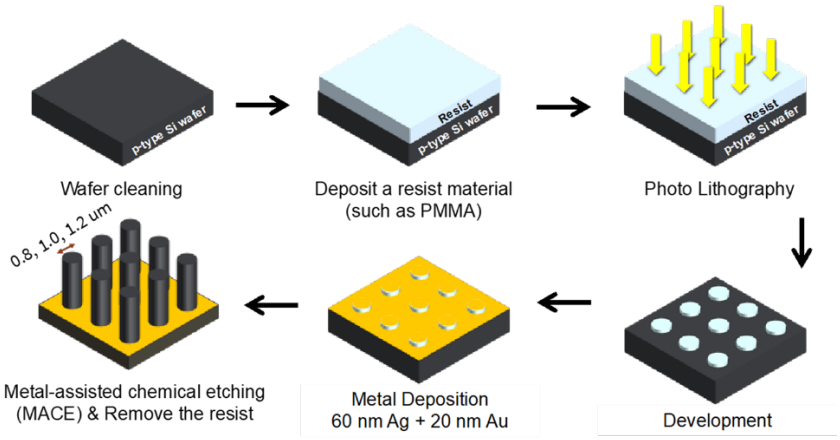

Figure 3. Schematic illustration of the SiNWs fabrication by PL patterning method and MACE.

2.3. Characterization

The morphology of the patterned Si wafers with pillars and after lift-off, and the as-fabricated SiNWs was checked by scanning electron microscopy (SEM, Magellan, SNSF). The diameter and length of patterned pillars and as-fabricated SiNWs, and the thickness of the metal catalyst were measured in SEM.

The thermal conductivity and electrical resistivity were measured by sonicating the SiNWs array in IPA for 5 s, picking up a single nanowire and dropping it on a fabricated measurement stage with 4 Pt electrodes. Contact between the nanowire and electrode was formed by Pt deposition, as illustrated in Fig. 4a and 4b.

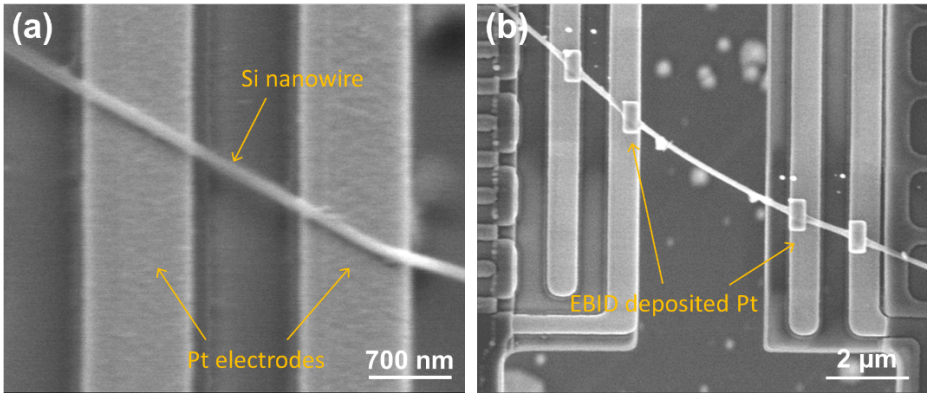

Figure 4. SEM images of (a) as-dropped Si single nanowire on Pt electrodes; (b) Si single nanowire on Pt electrodes after the formation of contact by Pt deposition.

3. Results and discussion

3.1 Nanoimprint lithography (NIL) patterning

Cleaned p type (5-10 Ωcm) and p++ type (0.005 Ωcm) wafer pieces with 1cm*1cm dimension are patterned using NIL method to have 150 nm to 200 nm diameter circle arrays with 400 nm to 450 nm spacing in between. SOG material was used as the patterning layer and the PMMA was used as the lift off sacrificial layer. Therefore, the Oxford RIE in SNF was used as the dry etch tool to etch both layers to obtain a mask for the later metal catalyst deposition. To have a clear understanding of the SOG material etch rate using the Oxford RIE, the as-imprinted SOG layer on Si wafer was tested with the desired etch condition (200W / 75mTorr / CHF_3(45sccm), CF_4(15sccm), O_2(10sccm)) as shown in Fig. 5. The SOG etch rate using the mentioned etch condition was determined to be 188 nm/min.

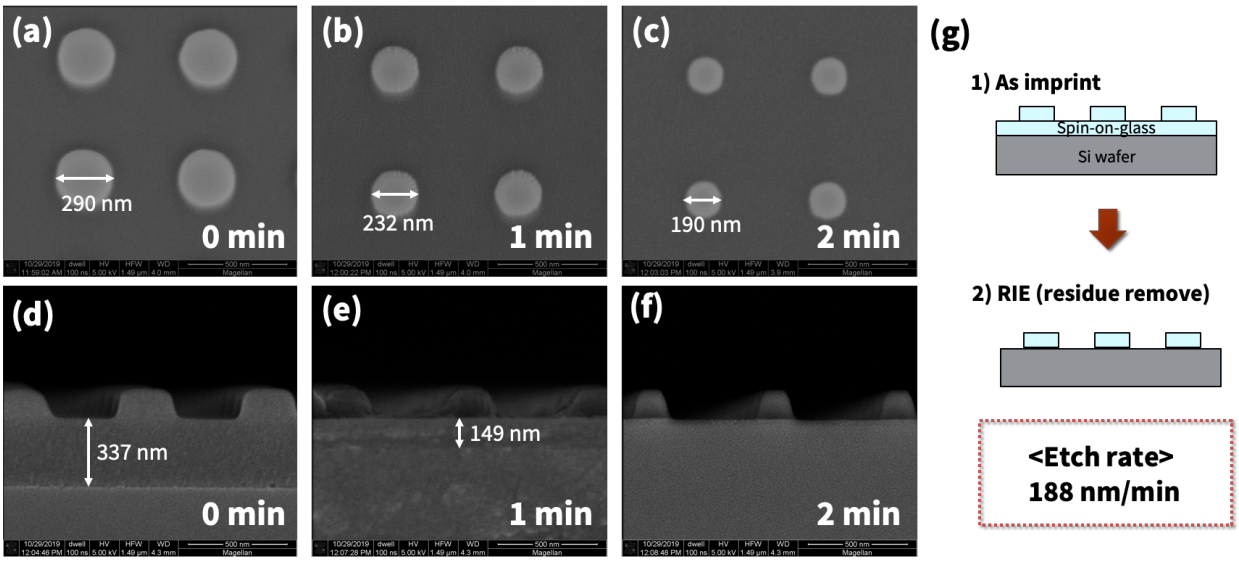

Figure 5. SEM images of patterned SOG nanopillars on Si wafer with different etch time of (a) 0 min top view, (b) 1 min top view, (c) 2 min top view, (d) 0 min side view, (e) 1 min side view, and (f) 2 min side view. (g) schematic of the side view of the SOG layer on Si before and after the RIE.

After obtaining the etch rate of the SOG layer, a thick PMMA layer followed by the patterned the SOG nanopillar layer was coated on the Si wafers as shown in the SEM images in Fig. 6. The schematic of the desired pattern is shown in Fig 2(a) and the actual SEM top view and side view of the actual SOG nanopillars and the bottom PMMA layer are shown in Fig. 6b and Fig. 6c.

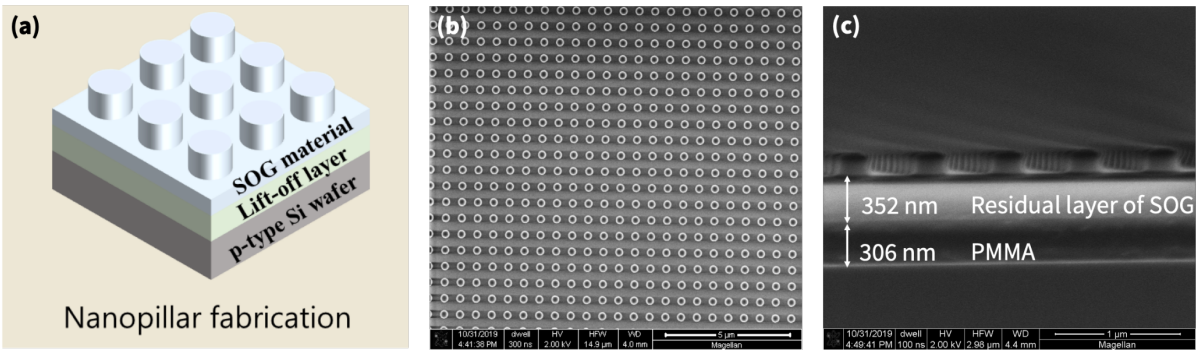

Figure 6. (a) Schematic of the SOG nanopillar layer and the sacrificial PMMA layer on Si wafer. SEM images of patterned SOG on the PMMA layer (b) top view and (c) side view.

After several trials, the optimal RIE conditions for the complete etch of the SOG layer (200 W / 45 sccm CHF_3, 15 sccm CF_4, 10 sccm O_2 / 75 mTorr / 1 min) and the PMMA layer (300 W / 50 sccm O_2, 10 sccm Ar / 50 mTorr / 90 s) were determined. The resulting SOG and PMMA layers after the RIE is shown in Fig. 7.

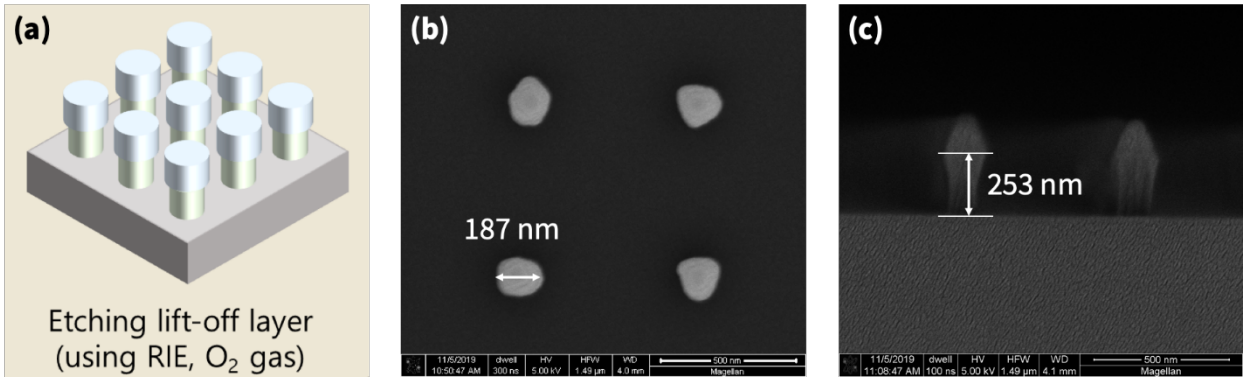

Figure 7. (a) Schematic of the SOG nanopillar layer and the sacrificial PMMA layer on Si wafer after RIE. SEM images of the after RIE patterned SOG on PMMA layer (b) top view and (c) side view.

60 nm of Ag and 20 of nm Au layers were deposited on the patterned Si wafer as the metal catalyst for the following MACE as shown in Fig. 8. Fig. 8c clearly shows that the PMMA lift-off layer is well separated from the bottom metal layer, which is essential to achieve a good lift-off pattern.

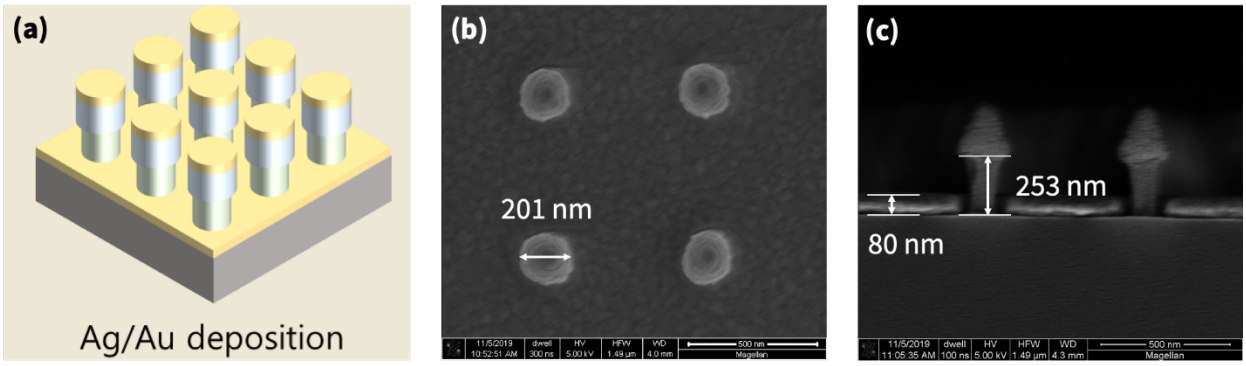

Figure 8. (a) Schematic of the SOG nanopillar layer and the sacrificial PMMA layer on Si wafer after RIE and metal deposition. SEM (b) top view and (c) side view images of patterned SOG on the PMMA layer after metal deposition.

The metal deposited wafers were dipped and sonicated in the DMF (Dimethylformamide) solvent to remove the lift-off layer. The resulting patterned metal layer after the lift-off on Si wafer is shown in Fig. 9. Fig. 9b shows that a 200 nm diameter hole pattern was achieved using nanoimprint lithography.

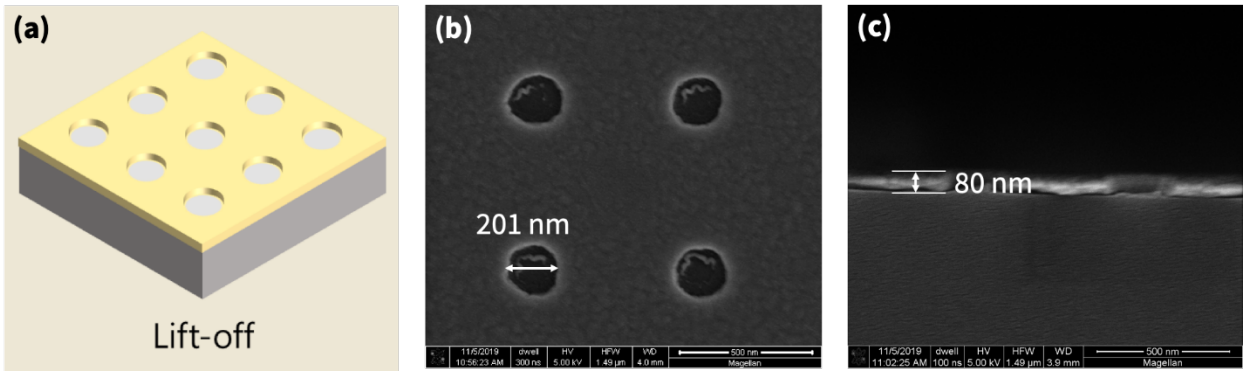

Figure 9. (a) Schematic of the lifted off metal layer on Si wafer. SEM (b) top view and (c) side view images of the lifted off metal layer on Si wafer.

3.2 Photo lithography (PL) patterning

Cleaned p type wafers with HMDS adhesion promotion layer and the photoresist layer were patterned using Heidelberg2. The mask patterns used in for the PL are 1.2 µm and 1.5 µm square arrays with 2 to 1 spacing in between as shown in Fig. 10. The pattern dimension and spacing were picked to fulfill the limitation of the Heidelberg2 with 375 nm light source. After developing and baking the photoresist, the HMDS layer was removed by the descum recipe using Technics. Similar to the NIL patterned wafers, 60 nm Ag followed by 20 nm Ag were deposited onto the patterned Si with photoresist acts as the lift off layer. The developed and the lifted off Si wafer side view SEM images were shown in Fig. 11. Fig. 11c shows that around 600 nm square hole pattern exposed from 1.2 µm square pattern mask was achieved using photo lithography method.

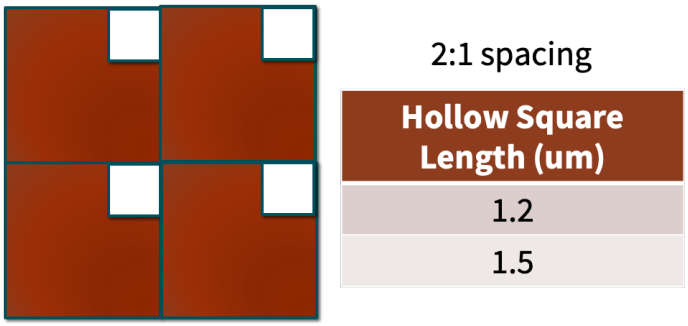

Figure 10. Schematic of the mask design used for photo lithography.

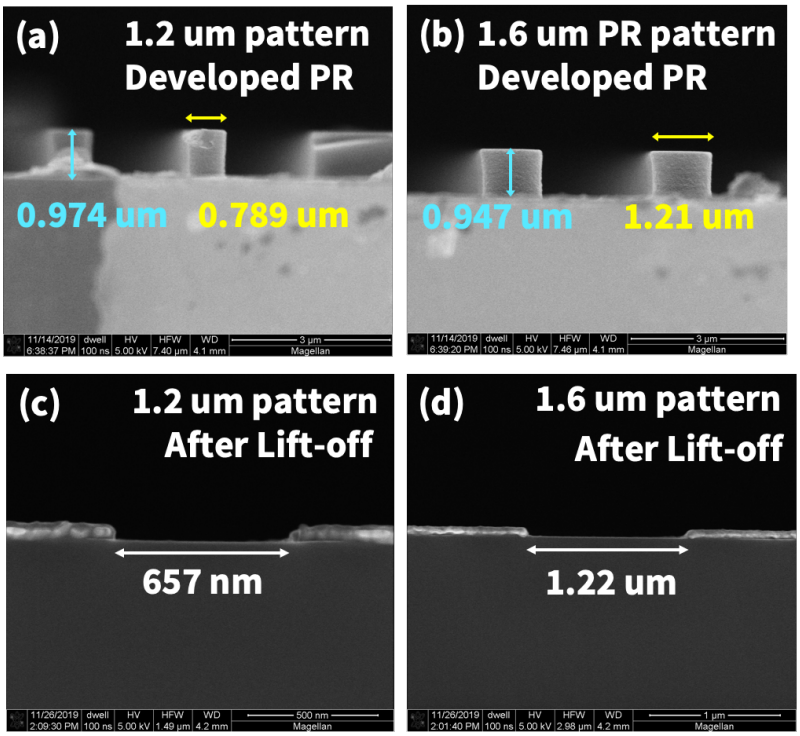

Figure 11. SEM images of the developed photoresist on Si wafer with (a) 1.2 µm and (b) 1.5 µm square mask dimensions. SEM images of the PL patterned metal layer with (c) 1.2 µm and (d) 1.5 µm square mask dimensions after lift-off.

3.3 Metal assist chemical etching (MACE) and thermoelectric characterization

The p type and p++ type Si wafers with metal layer patterned by NIL or PL were put in the 4.8 M HF and 0.3 M H_2O_2 solution for the MACE to make SiNWs. Some selective results of the SiNWs fabricated from the above two patterning method are shown in Fig. 12. The NIL patterned SiNWs show a higher etch rate during the MACE process, and it was able to achieve high aspect ratio (>900:1) SiNWs array with 20 hr etch time (Fig. 12b). The fabricated SiNWs were sent to our collaborator in the Lawrence Berkeley National Lab for thermal electric measurements. The resulting thermal conductivity and electrical resistivity results from the p type and p++ type Si wafers are summarized in Table 1. Both the p type and the p++ type SiNWs have similar thermal conductivity because the porosity of the two types SiNWs are similar. The p++ type SiNWs show a higher electrical conductivity due to a higher doping level than the p type SiNWs.

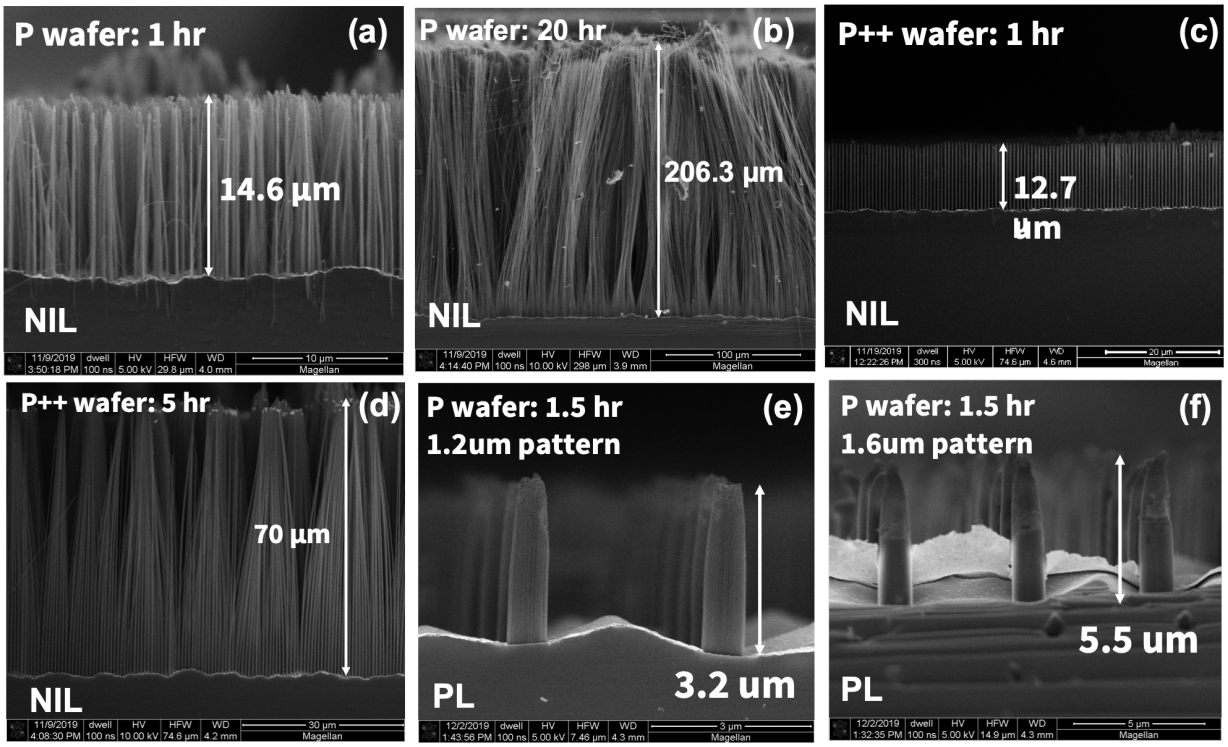

Figure 12. SEM images of SiNWs fabricated by NIL patterned p type wafer with (a) 1 hr MACE, (b) 20 hr MACE; NIL patterned p++ type wafer with (c) 1 hr MACE, (d) 5 hr MACE; (e)1.2 µm, (f) 1.6 µm square array PL patterned p type wafer with 1.5 hr MACE.

Table 1. Thermal Electric Characteristics of the P type and P++ type SiNWs

Sample	Thermal conductivity (W/m-K)*	Electrical resistivity (ohm m)*
312 nm diameter, p type Si wafer	3.81	12.75
259 nm diameter, p++ Si wafer	4.52	0.011

4. Future work

According to the preliminary results we obtained and our objectives, our future plan (Fig. 13) for the winter quarter includes: 1) to further refine the MACE etching method and explore MAAE process for better controllability of SiNWs fabrication. 2) to explore boron post doping of the fabricated SiNWs. The doping concentration of SiNWs may be improved by boron post doping and thus exhibiting higher electrical conductivity and higher TE performance. 3) to create a top and bottom ohmic metal contact of the fabricated SiNWs array, which is necessary for both TE measurement and requirement of practical use. 4) to continue the TE performance measurement. We hope to investigate the effects of dimension, porosity and doping concentration of Si single nanowire on the TE properties and show the feasibility of measuring the TE properties of SiNWs TE device with a relatively higher ZT.

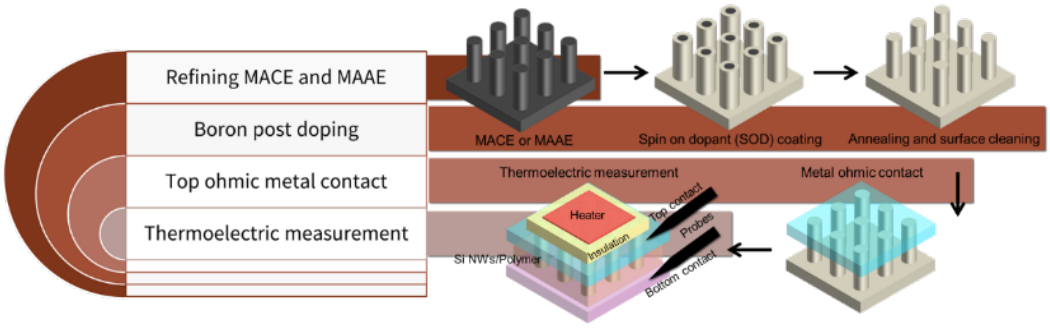

Figure 13. Schematic illustration of the future work in the winter quarter of 2020.

5. Reference

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6. Contribution

All authors contributed to this project equally.

Appendix I. SOP for Photo Lithography Patterned Si Wafers

1. Wafer cleaning and photo resist coating
    a. Clean the 4-inch Si wafer with Acetone, IPA, and water accordingly.
    b. Blow dry the wafer with N_2.
    c. Coat the wafer with HMDS (HexaMethylDiSilazane) using YES oven, using the default recipe.
    d. Spin coat 1 μm thick photoresist Shipley SPR 3612 with 2 mm EBR (edge bead removal) without vapor prime using svgcoat (automatic track).
        i. Recipe: 3612 1 μm w/o vp 2mm EBR.
2. Photo lithography (Heidelberg2)
    a. Expose the photo resist coated wafers with 1.2 μm and 1.6 μm square array patterns with 2:1 spacing in between the squares.
        i. Substrate template: Wafer 4 inch (Round shape).
        ii. Layer: FirstExposure only.
        iii. Laser wavelength: 375 nm.
        iv. Dose: 118.
        v. Defocus: -3.

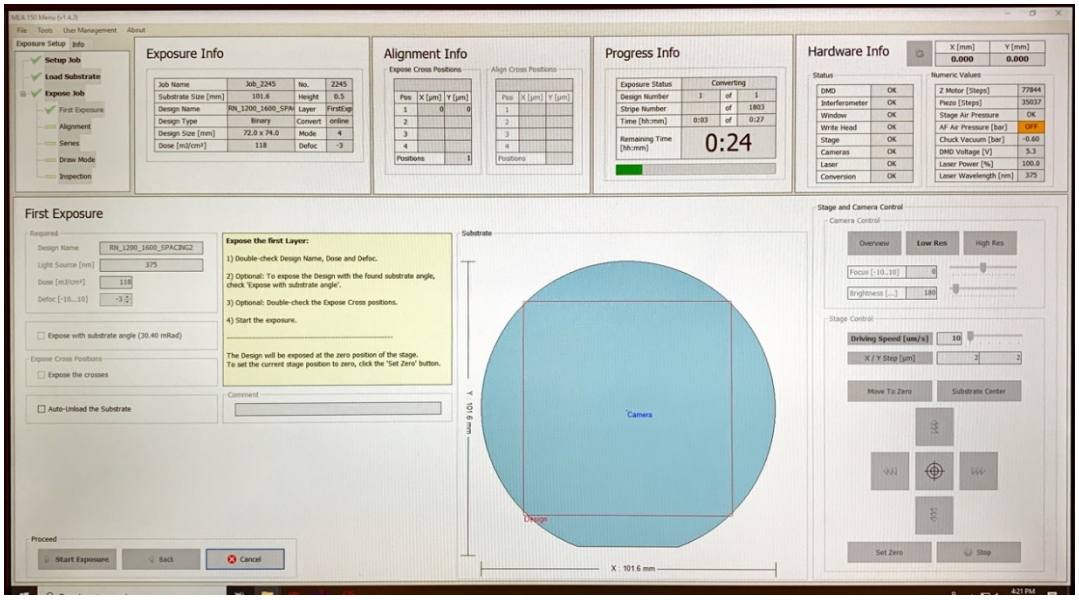

Figure 14. Heidelberg2 user interface setting information.

    b. Bake and develop the wafer using svgdev.
        i. Developer program #9 (null) + Oven program #1 (Baking only).
        ii. Developer program #3 + Oven program #1 (Developing + Baking).
    c. Check the wafer patterns using optical microscope and scanning electron microscope.
3. Remove HMDS layer using technics (descum)
    a. Gas2: 37.5 sccm
    b. Power: 50 W
    c. Time: 2 min
4. The patterned wafer is then ready for metal deposition.

Appendix II. SOP for Nano Imprint Lithography Patterned Si Wafers

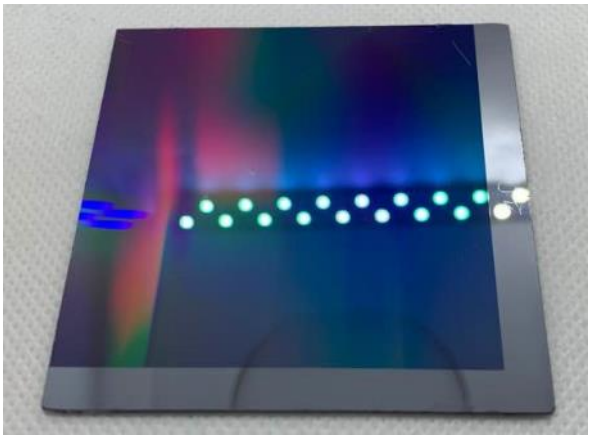

Figure 15. Optical image of Silicon master stamp with nano pattern (period: 600 nm, diameter: 300 nm, square array pillar)

1. Fabrication of PDMS mold
    a. Mix the SILGARD 184 base and SILGARD 184 agent with a ratio of 9:1 to make PDMS.
    b. Degassing in the desiccator to remove the air bubbles.
    c. Pour 6mL of mixed PDMS on the 6 cm * 6 cm master Si stamp (Fig. x) and cured for 1 hour at 120°C on hot plate.
    d. Detach the PDMS mold from the Si stamp
2. Preparation of substrate
    a. Rinse the wafer with acetone, IPA and DI water
    b. Spin coat the 6 wt% PMMA (3s acceleration, 30s spin coating, 3000 rpm)
    c. Soft baking at 80°C on hot plate for 10 min
3. Imprinting
    a. Spin coat the 3.4 wt % SOG (solution with IPA as solvent, Filmtronics) on the PDMS mold (3s acceleration, 30s spin coating, 3000 rpm)
    b. Directly contact with the prepared substrate
    c. Degassing in the desiccator for 5 min
    d. Detach the substrate from the PDMS (pattern transferred)
4. RIE (two-step etching) using Ox-RIE
    a. First step SOG materials etch: 200 W / 45 sccm CHF_3, 15 sccm CF_4, 10 sccm O_2 / 75 mTorr / 1 min
    b. Second step PMMA layer etch: 300 W / 50 sccm O_2, 10 sccm Ar / 50 mTorr / 90 s
    (After each step, it was paused 30s to prevent the PMMA layer from melting caused by the high temperature during the process)
5. The patterned wafer is then ready for metal deposition.

Appendix III. SOP for Metal Assisted Chemical Etching (MACE)

1. Deposit metal catalyst layers using the AJA e-beam evaporator
    a. First layer: 60 nm Ag (evaporation rate: 0.1 nm/s).
    b. Second layer: 20 nm Au (evaporation rate: 0.1 nm/s).
2. Metal layer lift off:
    a. Nano imprint lithography: sonicate in DMF for 20 min.
    b. Photo lithography: dip in Shipley 1165 for 20 min and then sonicate for 10 s. Rinse with IPA and dry with N_2 after the lift off.
3. Place the metal coated Si wafer piece (~ 1 cm * 1 cm) in a 2% HF solution for 1 minute to improve the direct Ag/Si adhesion. Do this step immediate before step 3
4. Transport the samples directly from the 2% HF solution to a MACE solution composed of 4.8 M HF and 0.3 M H_2O_2 (typically 30 mL of total volume) to etch the SiNWs at room temperature to the desired length. (etch rate: ~ 0.2-0.3 μm/min)
5. After MACE etching, soak the sample in IPA.
6. Dry the sample with critical point dryer to prevent agglomeration.

Appendix IV. Expenses

The budget of fall 2019 is summarized in Table 2. We spent $ 1060 for equipment training in SNF, $ 3025.34 for equipment usage in SNF and SNSF and $ 333.2 for materials and supplies purchase in SNF. In summary, we have spent $ 4418.54 by the end of 10th week of the fall quarter of 2019, which is within our proposed budget of $ 4985.

Table 2. Budget of the fall quarter of 2019.

Budget			
Detailed Cost ($)	Training	Equipment Usage	Materials
	1060	3025.34	333.2
Overall Cost ($)	4418.54		
Proposed Budget ($)	4985		
Remaining ($)	566.46		