MOSCAP Characterization of SNF ALD

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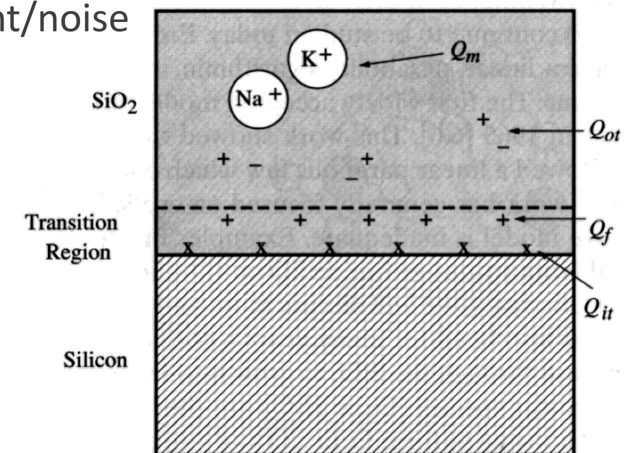
EE412, Fall 2014

Motivation

- Electrical properties of ALD dielectrics is of great importance to a wide range of devices fabricated in the SNF:
  - Si-MOSFETs
  - Untraditional FETs
  - RRAM
  - Etc.
- Despite its use, no comparison between machines or types of ALD

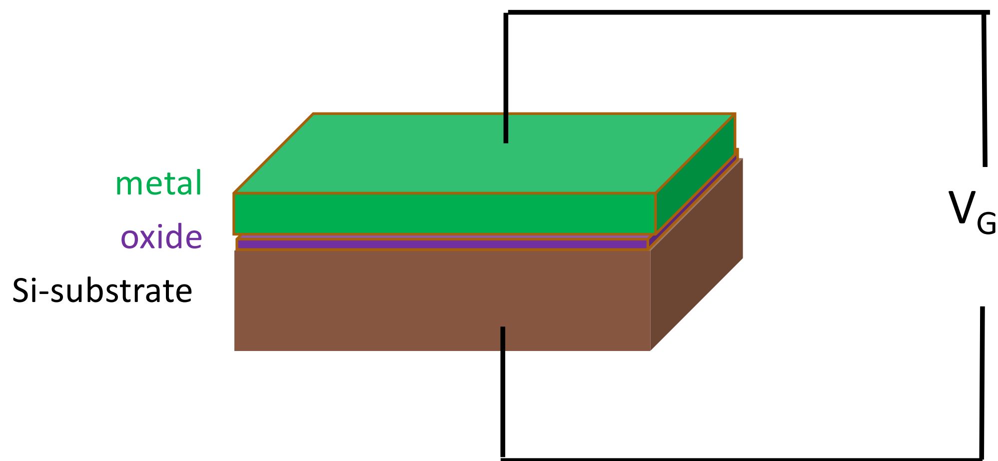
What is “electrical quality” of an oxide?

- Mobile ions create hysteresis
  - Mobile ions from atmosphere
- Oxide trapped charge create threshold shifts
  - Structure defects -> highly dependent on temperature, FN tunneling, radiation, etc.
- Interface traps create threshold shifts, hysteresis, and leakage current/noise
  - Fill or unfill trap states
  - Frequency dependent
  - Electrical communication with semiconductor



Characterization

- Moscaps (Metal-Oxide-Silicon Capacitors) are widely used to characterize electrical properties of dielectrics



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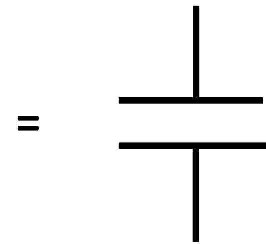
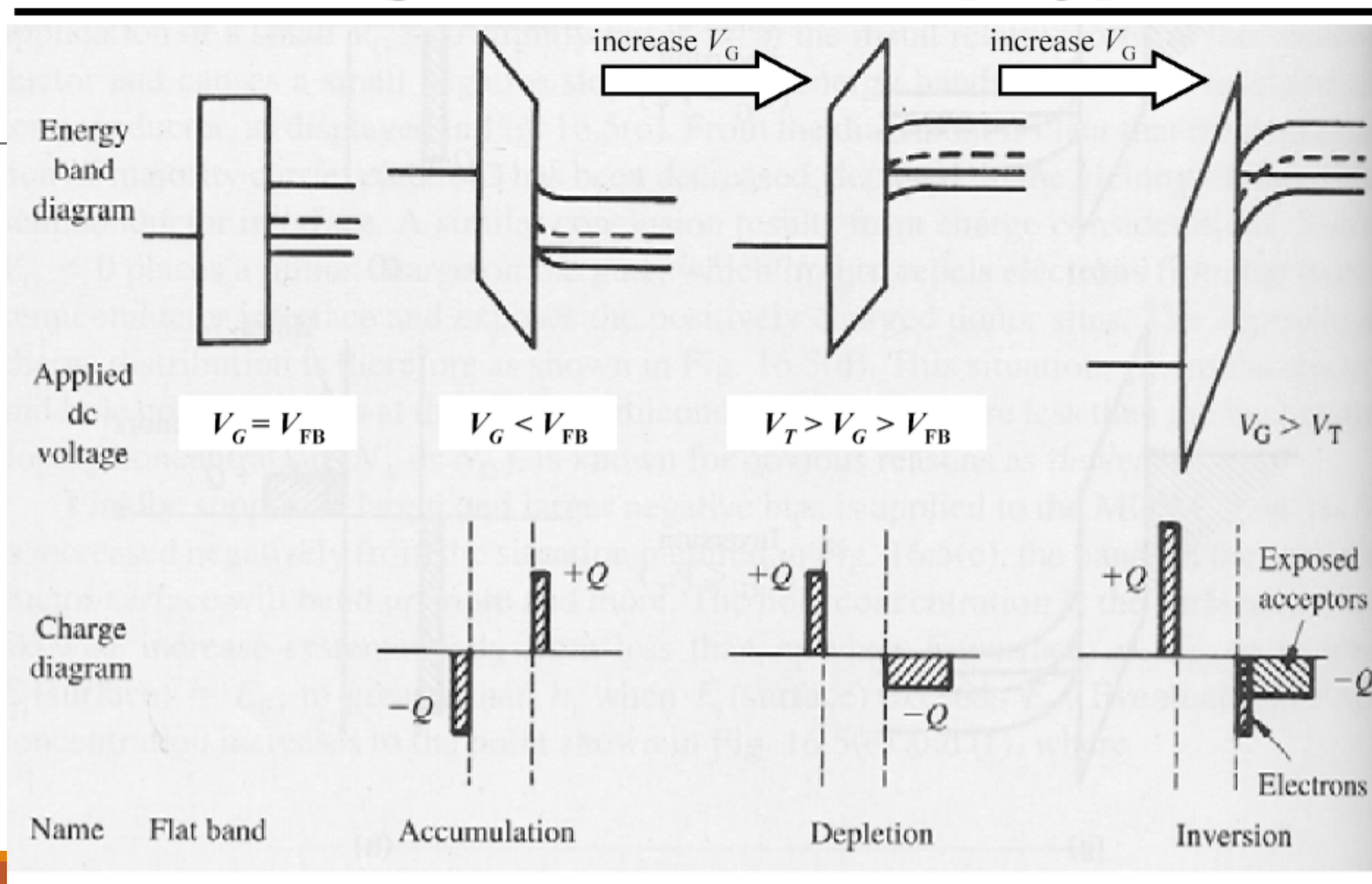


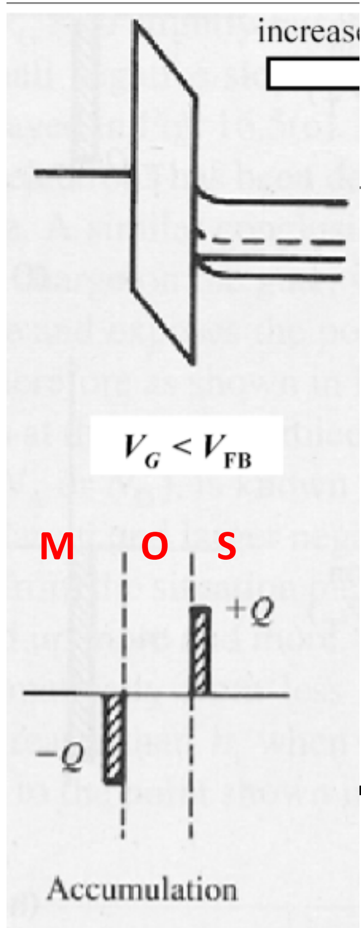
$$C = \frac{k * e_o * A}{d}$$

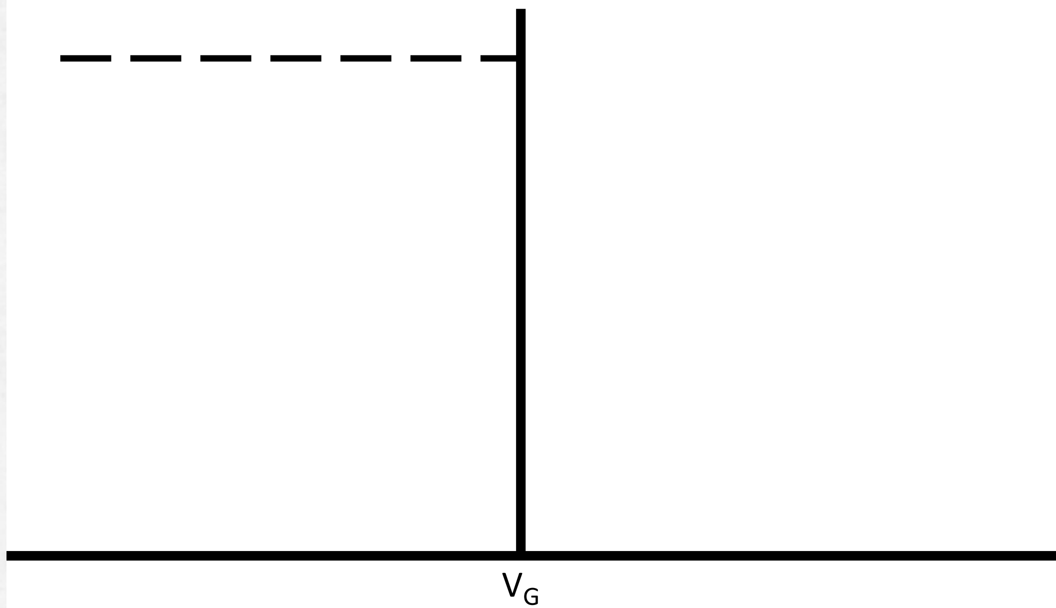
Unlike two metal plates, capacitance is frequency dependent.
Allows for analysis of interface traps (which are frequency dependent)

Biasing Conditions for p-type Si



MOSCAP operation





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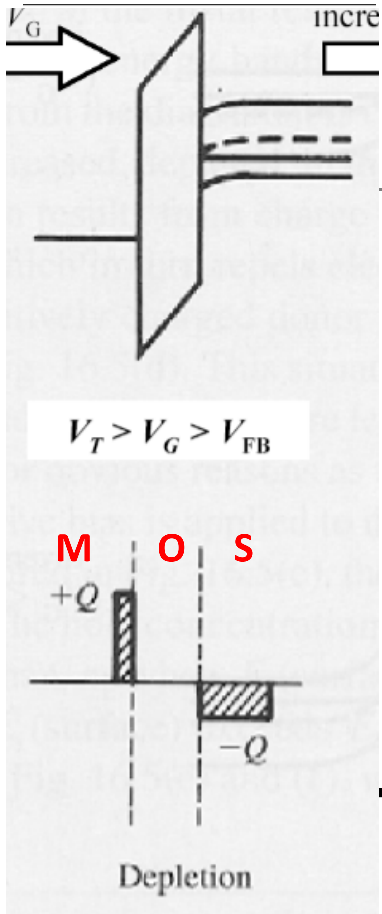

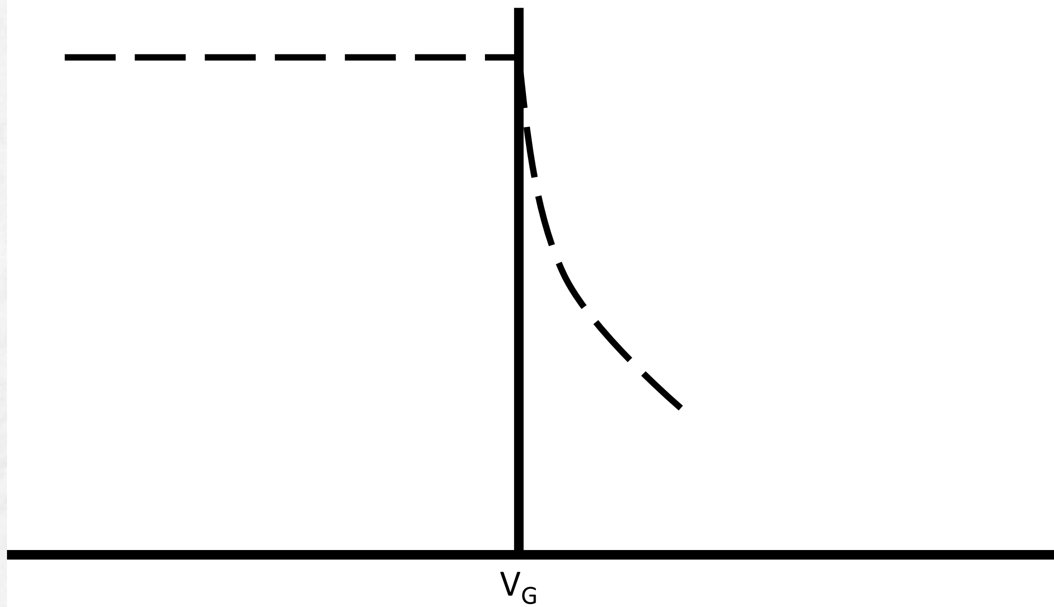

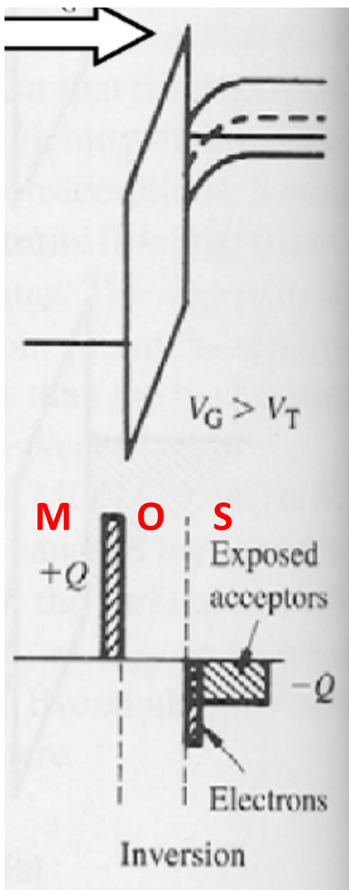

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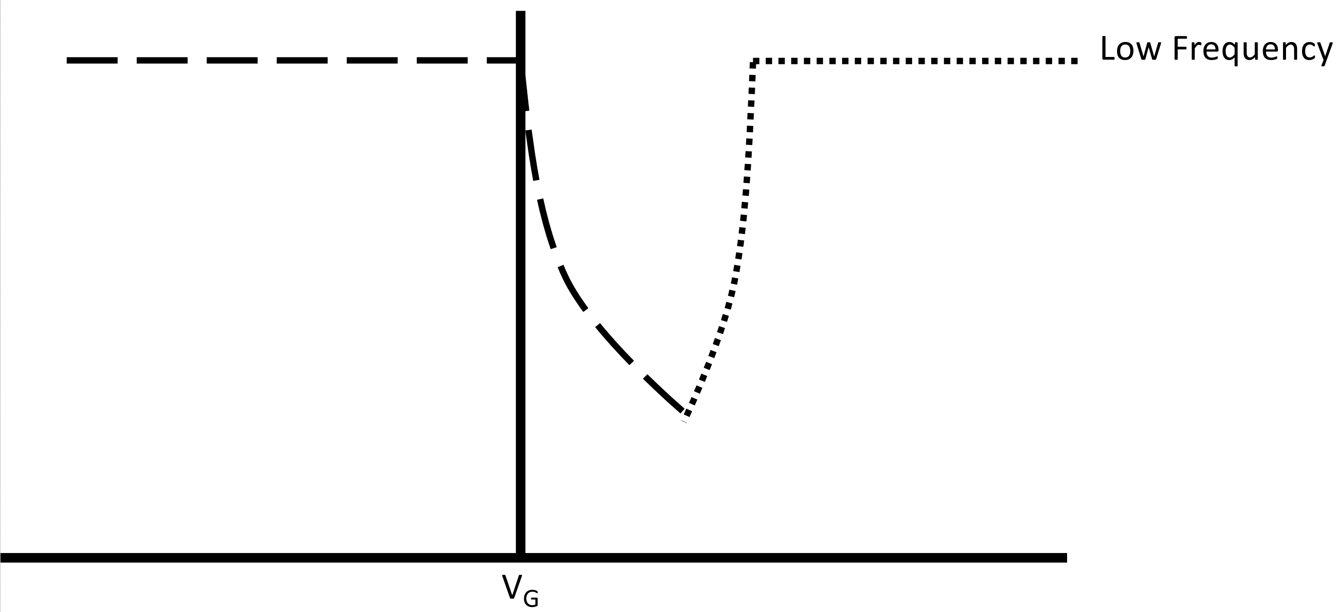

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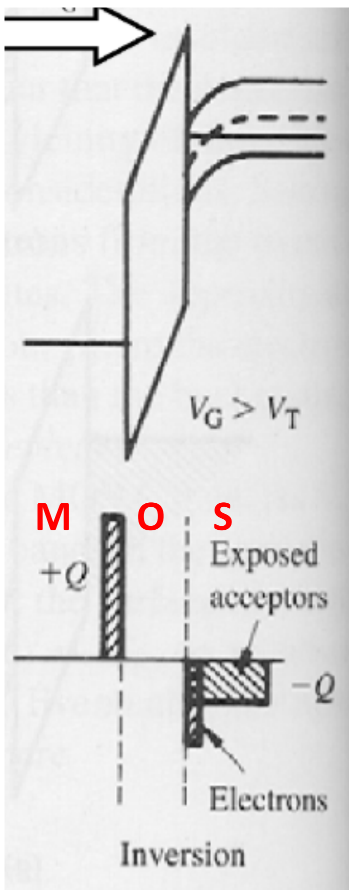
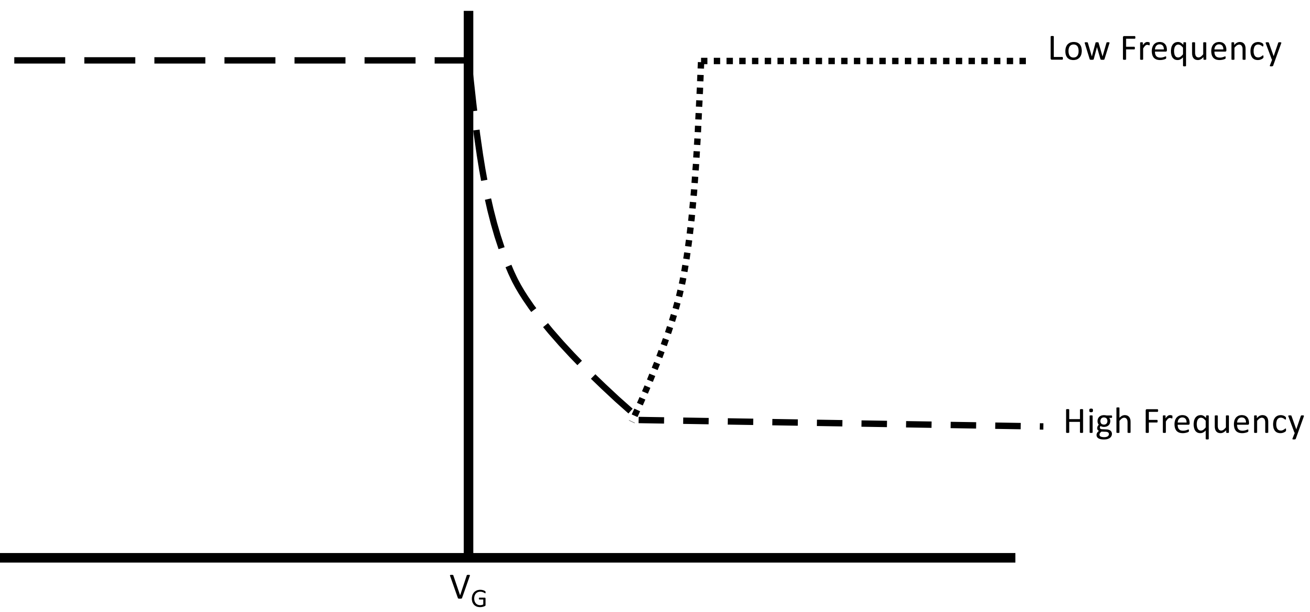
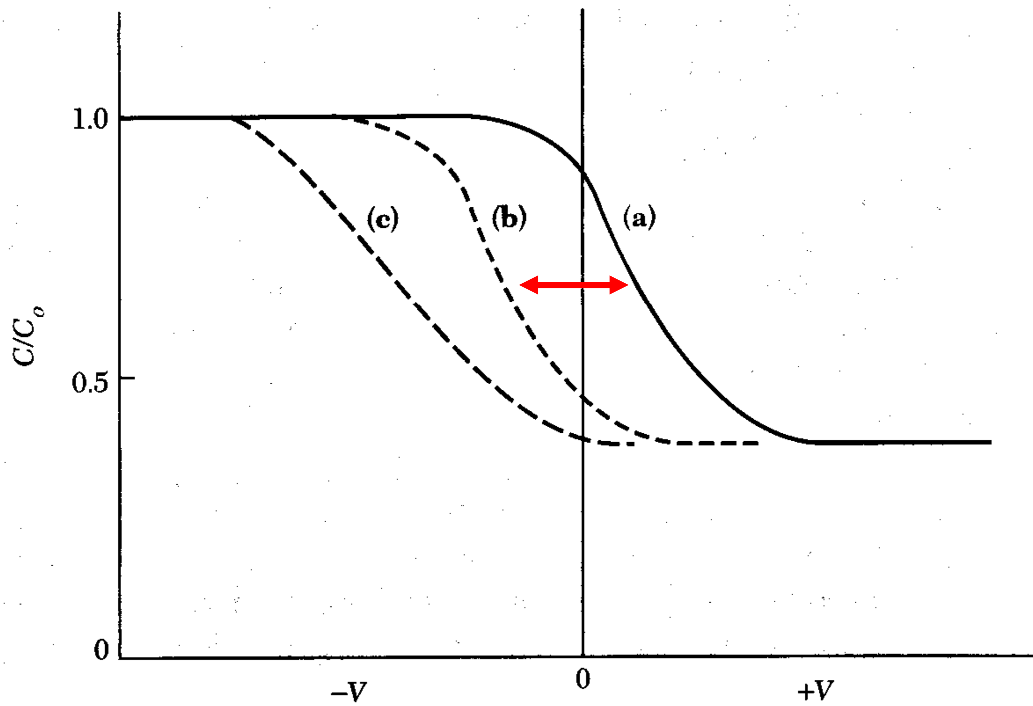




How to Interpret CV curves



A= ideal CV curve
B= fixed charges (horizontal shift)
C= interface traps (distortion)

Fabrication Process

Clean Si substrate
(RCA clean, wbdiff)

ALD dielectric deposition
200^{0}C, 250 cycles (100 cycles pre-season)

Metal deposition
90nm Al

Optional FGA anneal

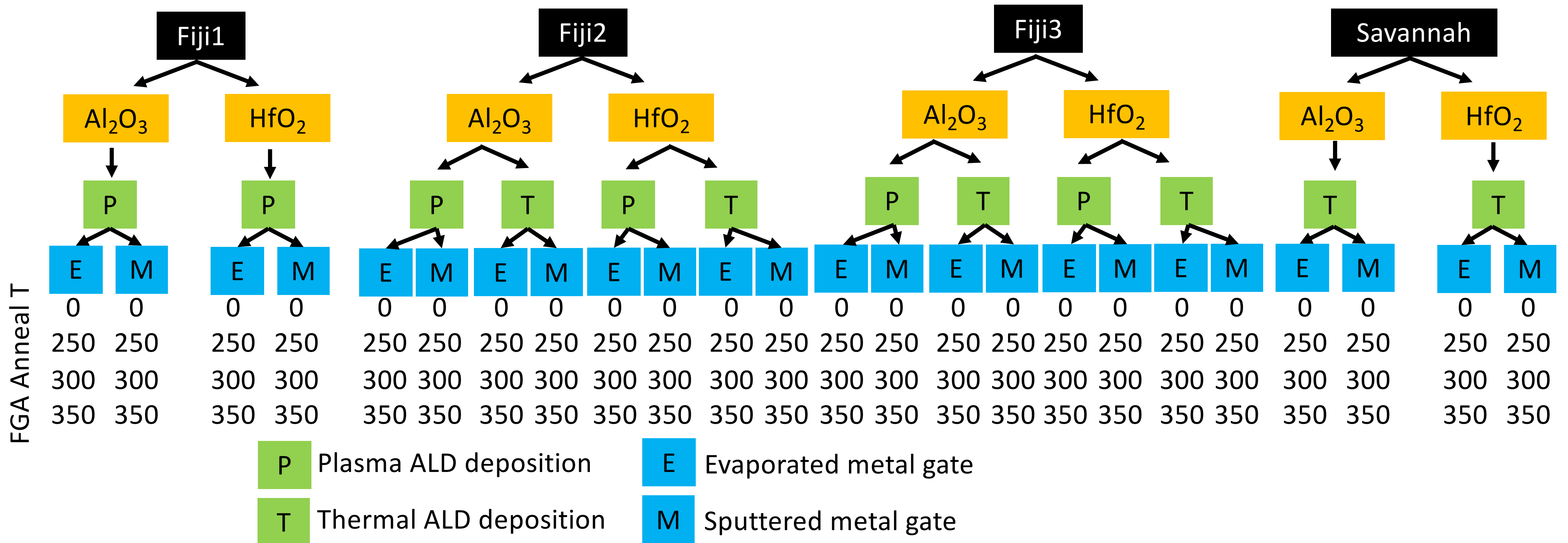
Vg

CV Measurements

Test Cases

- Difference between machines
  - Clean Fiji1, Dirty Fiji2, Oxide-only Fiji3, Savannah
- Difference between plasma/ thermal ALD
- Difference between metal deposition methods
  - Sputter vs. evaporation
- Difference with annealing temperature
  - 0, 250C, 300C, 350C FGA annealing

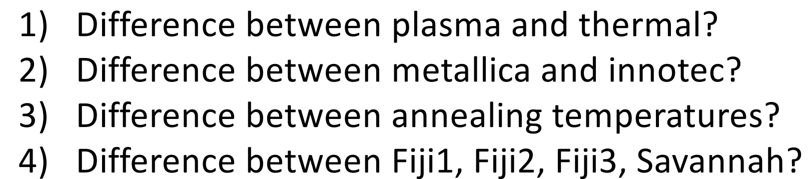
Test Cases



Results

.mat file for every oxide available for labmembers to download (~60% completed)

Can we answer some key questions:



1) Difference between plasma and thermal?
2) Difference between metallica and innotec?
3) Difference between annealing temperatures?
4) Difference between Fiji1, Fiji2, Fiji3, Savannah?

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Plasma vs. Thermal – does it matter?

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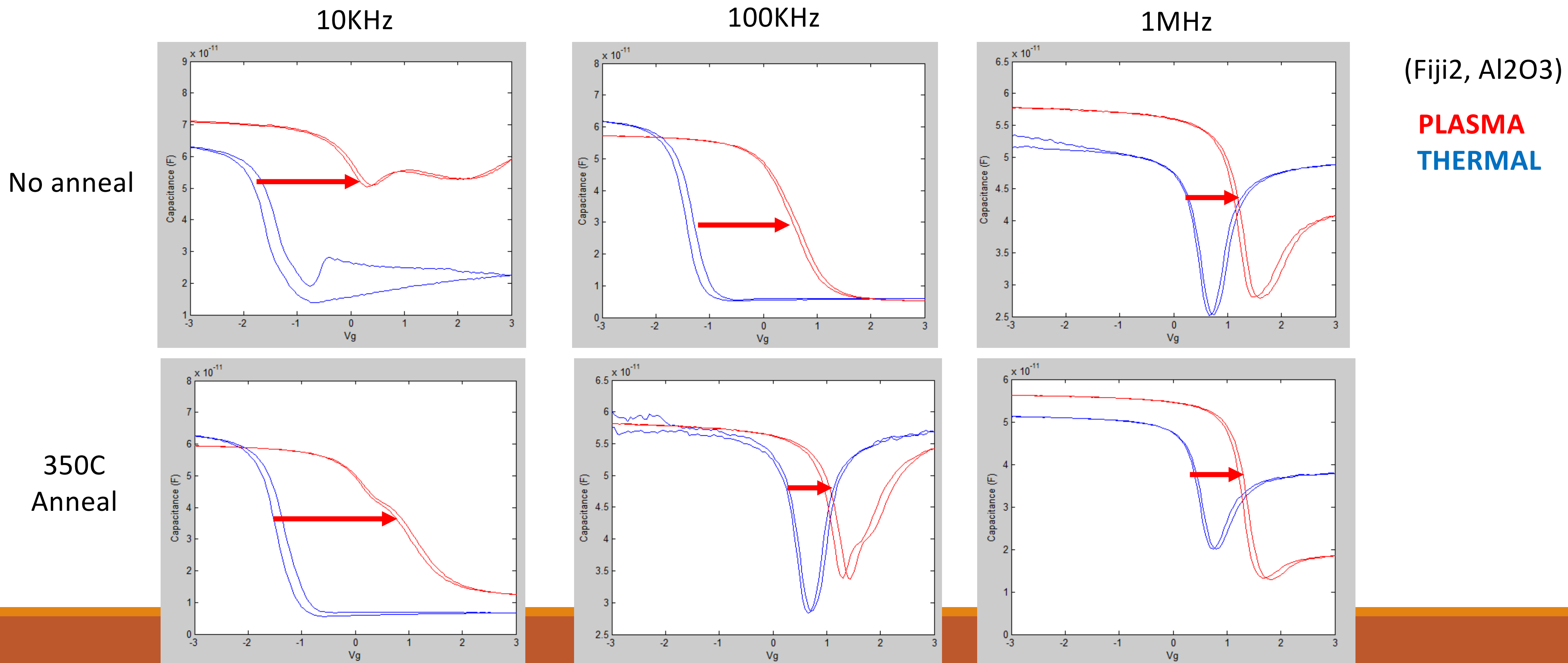
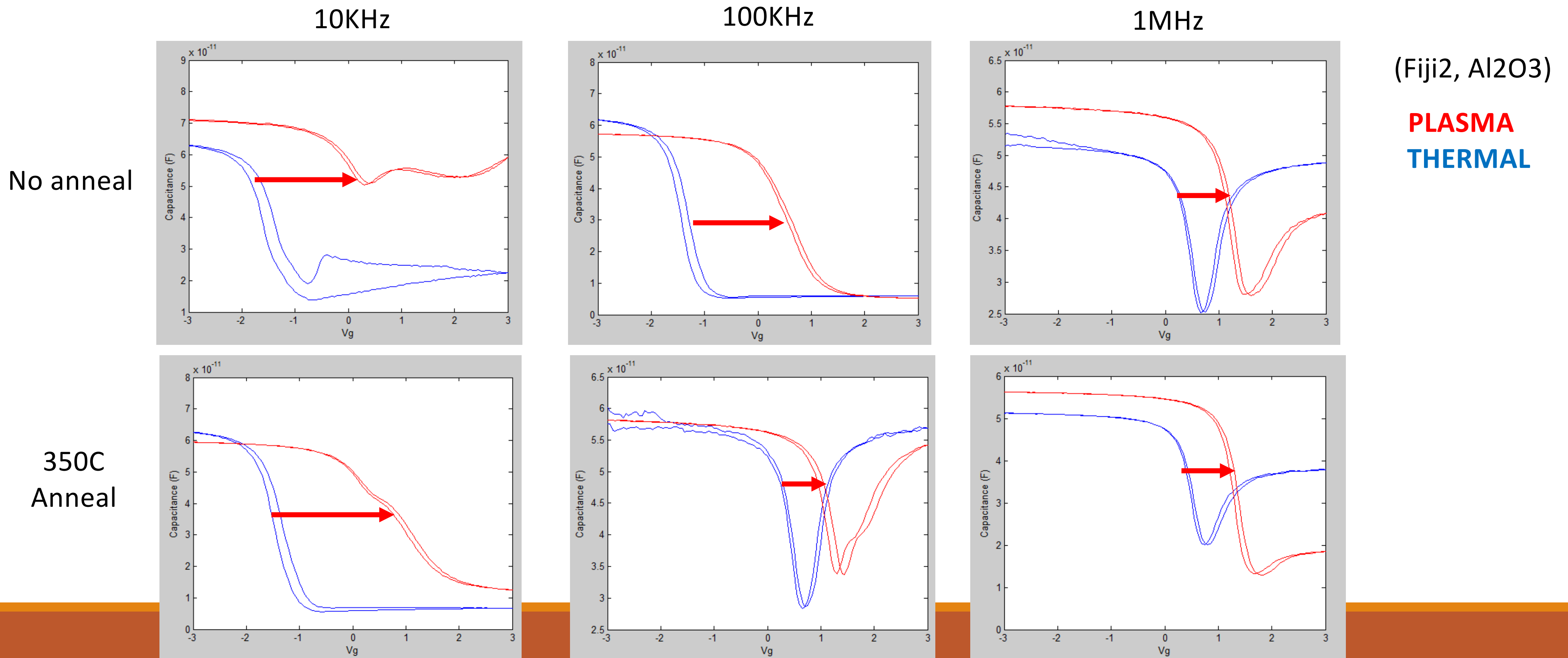


Plasma vs. Thermal – does it matter? YES



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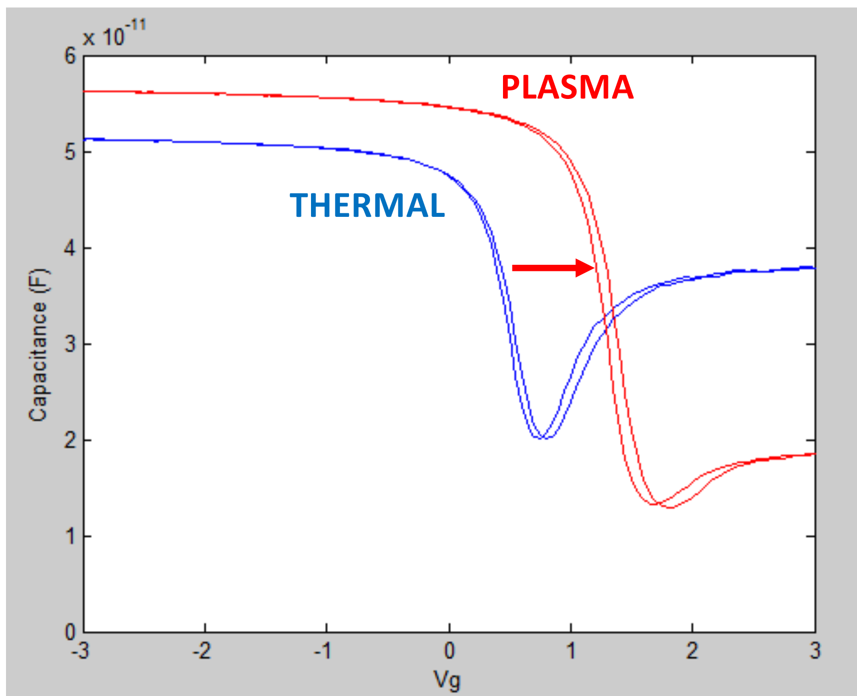
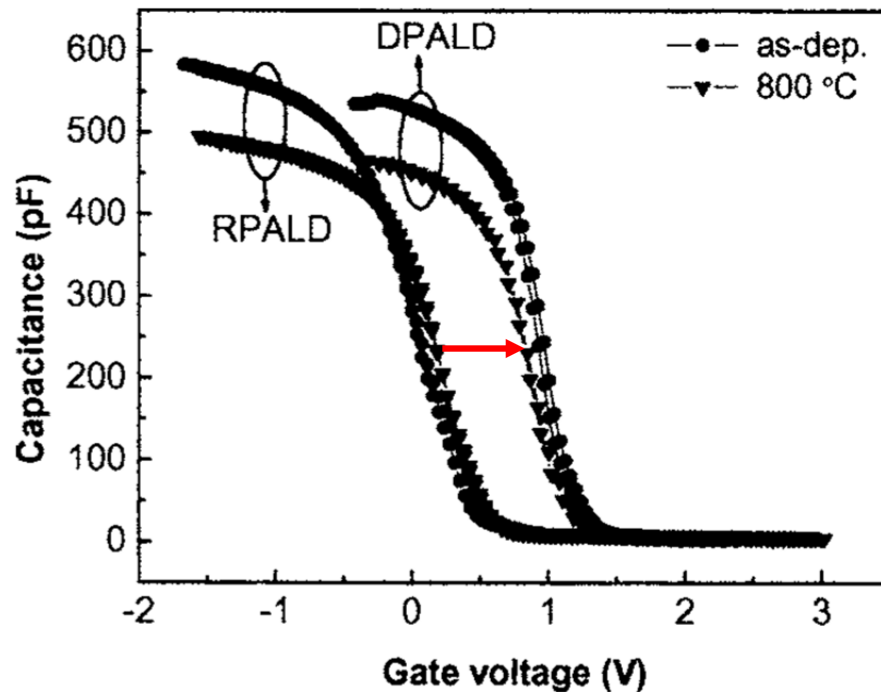
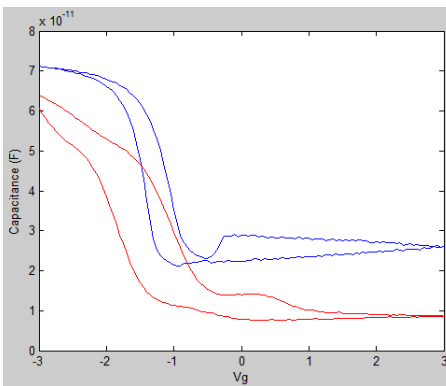
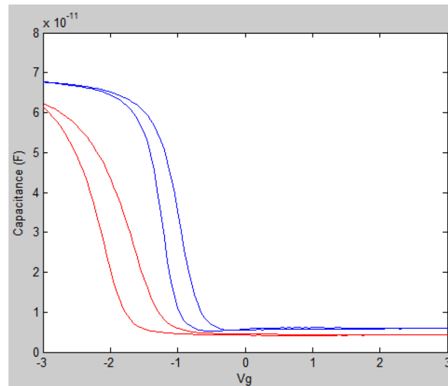
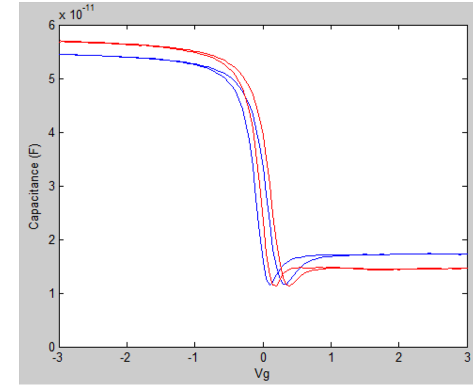
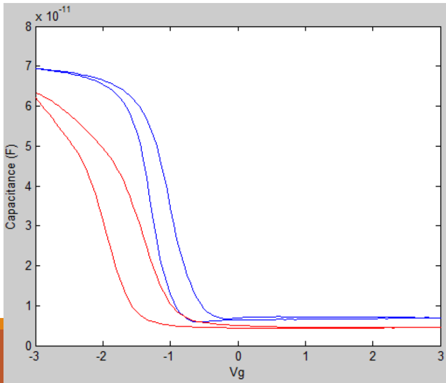
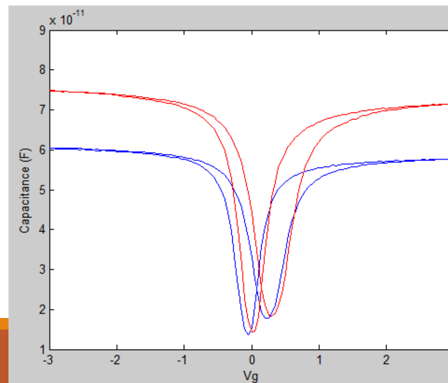
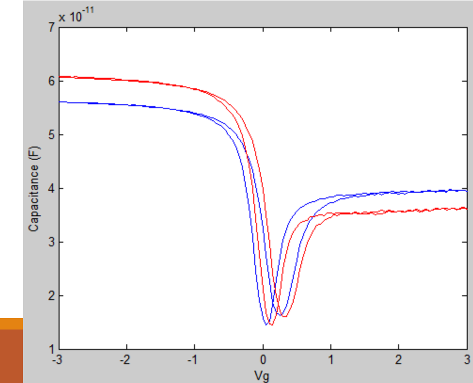




Metallica vs. Innotec – does it matter?

Metallica vs. Innotec – does it matter? 2nd order

	10KHz	100KHz	1MHz
No anneal			
350C Anneal			

(Savannah, Al2O3)

METALLICA

INNOTEC

Both work – no effect on hysteresis.

Annealing Temp.– does it matter?

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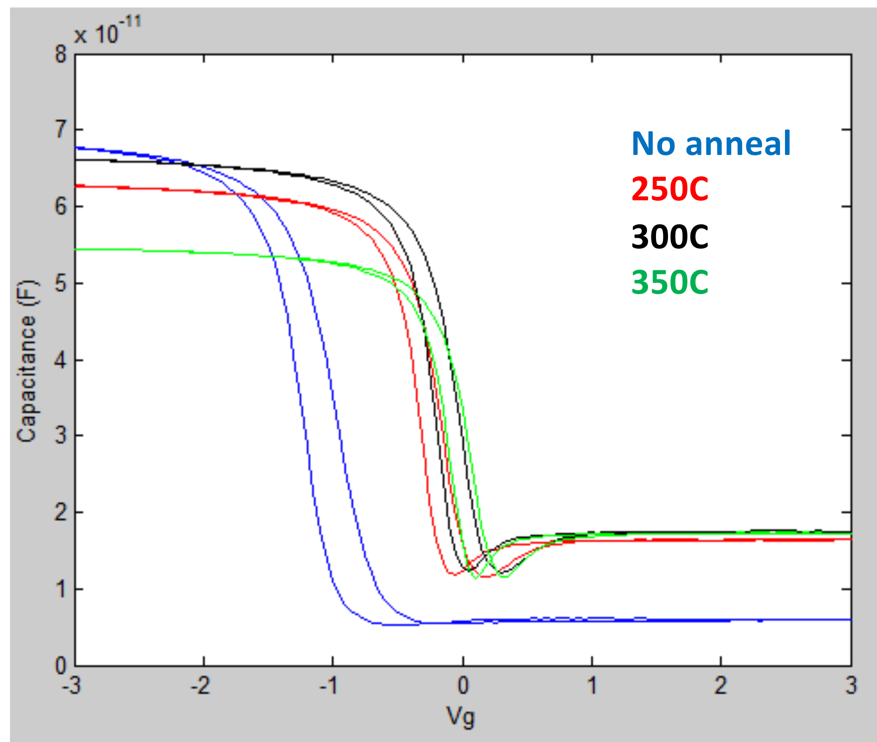

(Savannah, Al_2O_3, 1MHZ)

Diminishing returns from increasing anneal temperature.

Which Chamber – does it matter?

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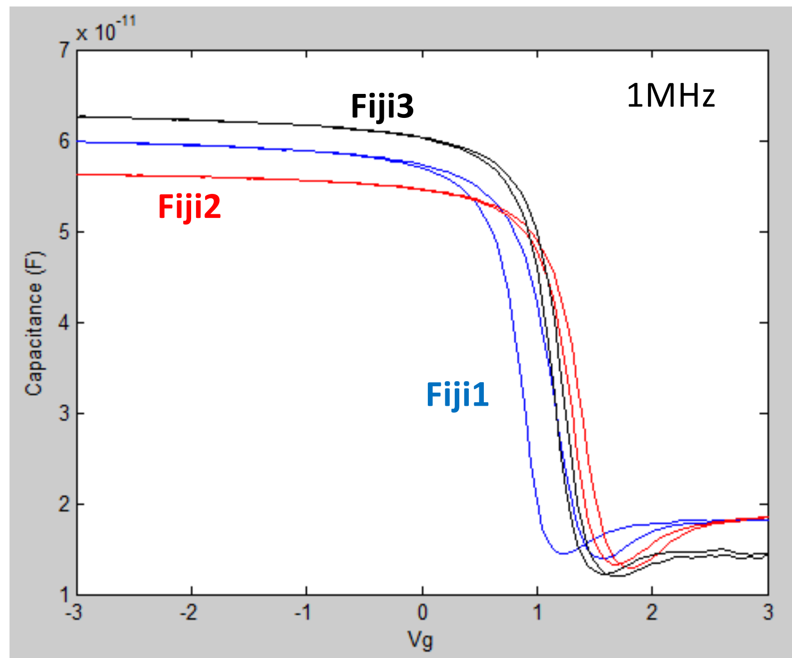
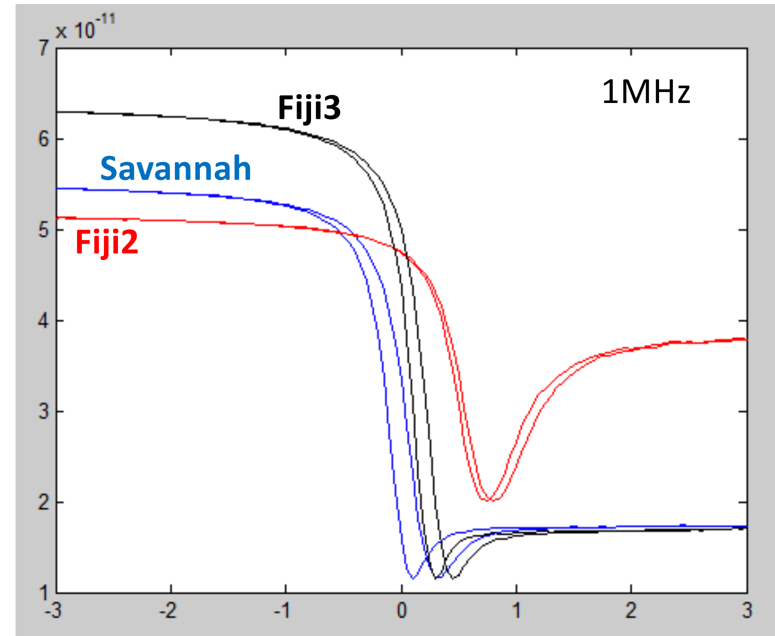
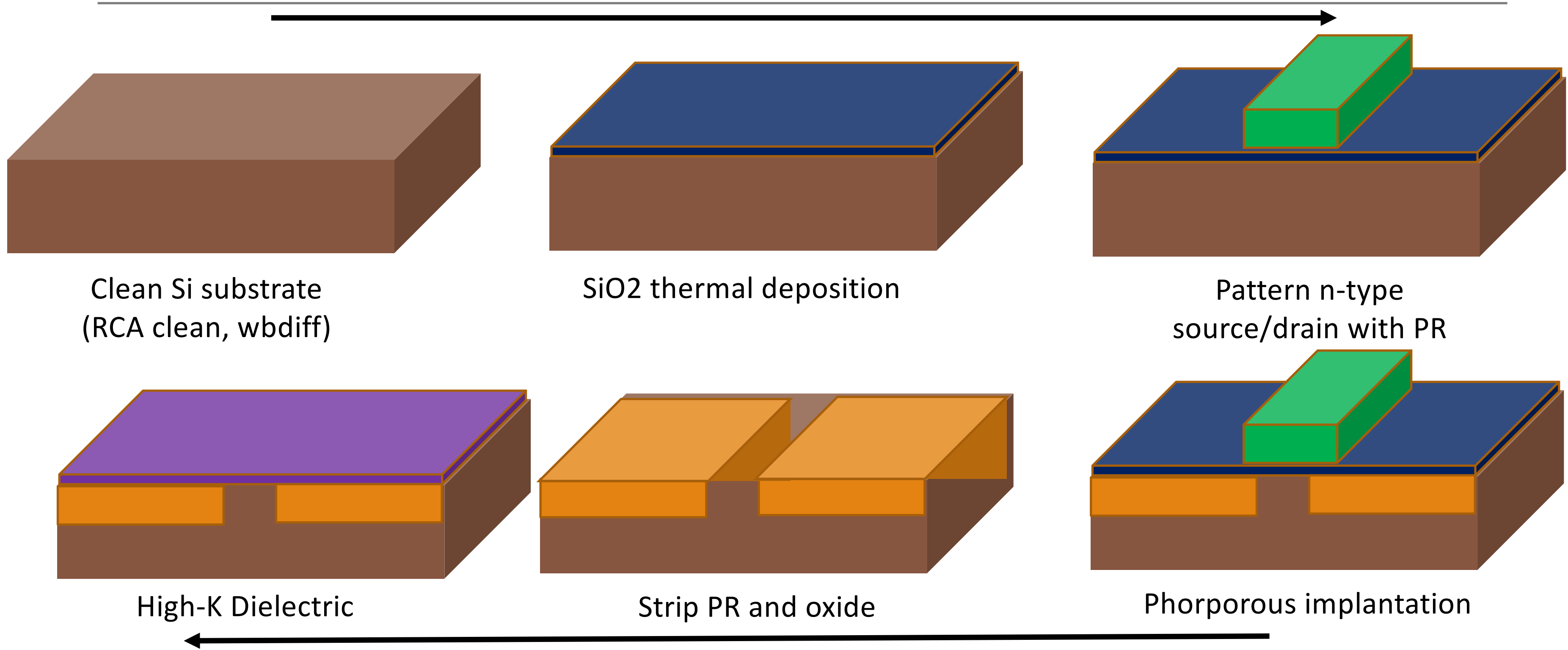
Al2O3, plasma



Al2O3, thermal



MOSFET Fabrication (NMOS)



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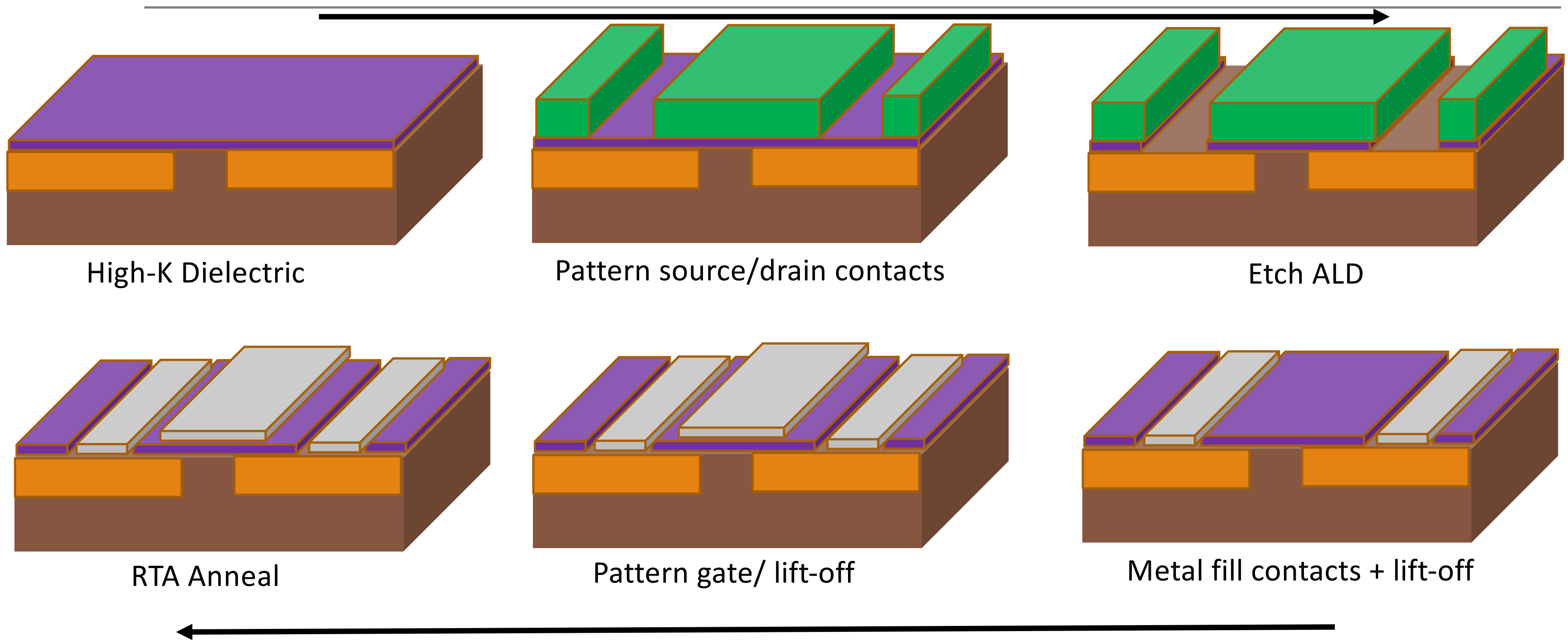

MOSFET Fabrication Details

Step	Machine	Details	Notes
Clean	Wbnonmetal+wbdiff	Regular RCA clean	Use I-prime p-type wafers. ~1e17 doping for p-type channel
SiO2 growth	Thermco1,2,3,4	22nm dry oxidation, 900C	Measure thickness after with woolum
Pattern source/drain n-type implantation regions	PR coating (svgcoat) PR exposure (ASML) PR develop (svgdev)	3612, 1um resist. No hard-bake required.	This channel length is 2um.
N-type source/drain implantation	Outsource	Phosphorous, 1e15 dose, 60keV. Energy depends on actual SiO2 thickness. This dose for 22nm yields ~60-80nm junction depth.	
Resist strip	Gasonics	Regular recipe (3) for 1um 3612.	Optional wbnonmetal clean. Do NOT do HF dip, SiO2 must be intact for flash annealing.
Flash anneal	RTA-left	1050 in argon for 5 seconds	
Strip SiO2	Wb-flexcorr1-4	2% HF dip, 5 minutes.	
ALD Deposition	Savannah ALD	Al2O3, 200C, 125 cycles	Deposit ALD as soon as possible after SiO2 stripping in HF.
Pattern Source/Drain contacts	Headway (lol2000) Svgcoat (3612 1um) ASML (expose, 55 dose) Develop (program 5)	Headway: 3000 RPM, bake in oven at 195C for 22 minutes.	
Etch source/drain contacts	Wb-flexcorr1-4	2% HF, 50 seconds	Optional oxygen descum in drytek4. (I did both ways, saw no difference. More robust with the descum though)

Step	Machine	Details	Notes
Deposit source/drain contact metal	Innotec	5nm Ti/30nm Pt	
Lift-off	wbsolvent	Lift-off in acetone Remover PG for 15 minutes to remove LOl2000. Clean with IPA.	
Pattern gate	Headway (lol2000) Svgcoat (3612 1um) ASML (expose, 55 dose) Develop (program 5)	Headway: 3000 RPM, bake in oven at 195C for 22 minutes.	Optional oxygen descum in drytek4. (I did not do)
Evaporate gate metal	Innotec	5nm Ti/30nm Pt	
Lift-off	wbsolvent	Lift-off in acetone Remover PG for 15 minutes to remove LOl2000. Clean with IPA.	
Optional: Passivation	Savannah ALD	10 nm Al2O3.	Need to re-etch contacts to source/drain. Used to covered exposed regions of source/drain due to undercutting of oxide to pattern source/drain contacts.
Anneal	RTA2	FGA anneal, 300C, 5 minutes	

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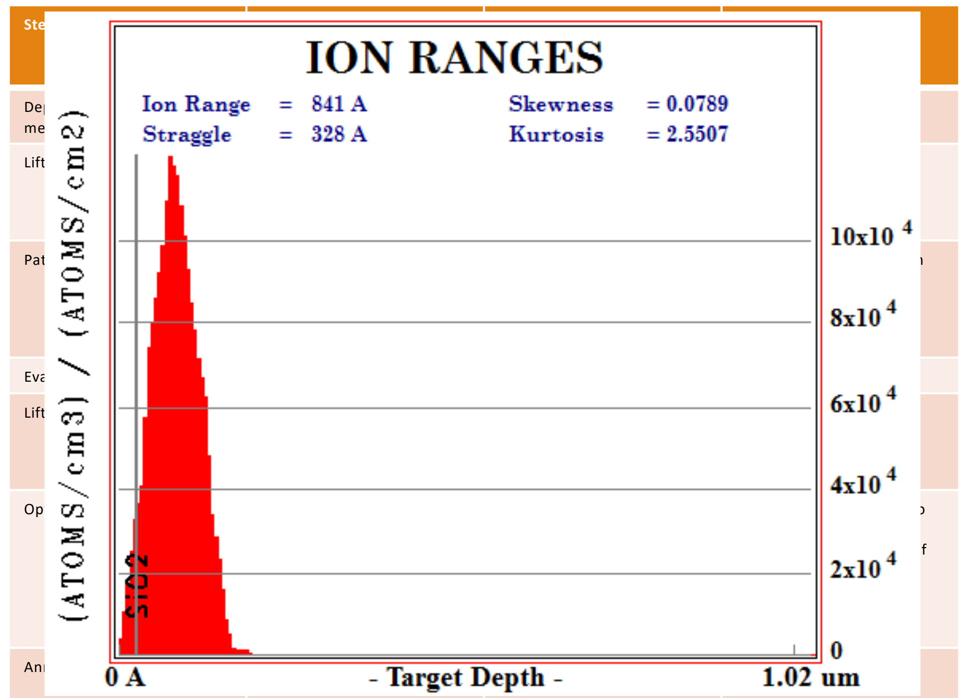
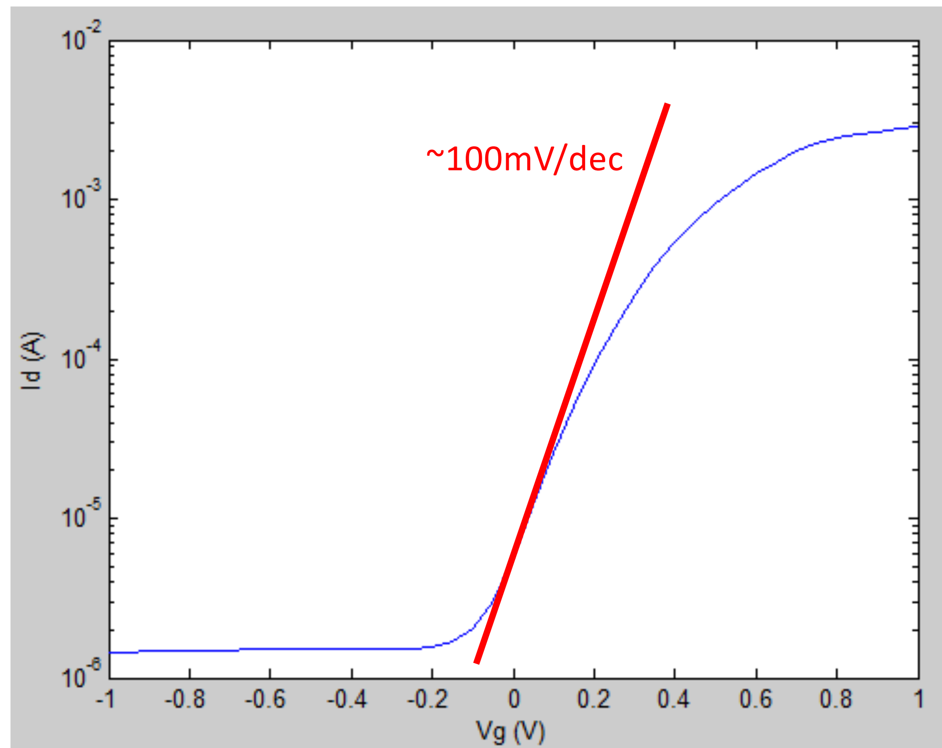


MOSFET Results



Conclusions

- Database for labmembers to look-up and analyze every HfO_2/Al_2O_3 dielectric
- Wafers with every HfO_2/Al_2O_3 dielectric for labmembers to test for their own projects
- Plasma versus thermal ALD has the largest effect, with large +Vt for plasma ALD
- Fiji1 offers the worst gate dielectrics
- Innotec and Metallica are interchangeable for gate dielectrics
- FGA annealing at 250C is sufficient
- Standard and simple N-MOSFET process

Thanks

- My great partner Kye!
- Thanks Ashish!
- Mentors: Prof. Roger Howe, Dr. Mary Tang, Dr. Michelle Rincon, Dr. J Provine
- EE412 class