EE412 Project

NMOS-Depletion Mode Process for EE410

Report prepared by

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Safety and Cleanliness

Laboratory Safety

Since laboratory safety can never be overemphasized, the students are reminded again of the importance of safe practices in the laboratory. In addition, it is to no surprise that when laboratory work is conducted safely, gross processing mistakes become less frequent, which can only mean better-quality results are likely to be attained. On another note, incidences could potentially destroy a complete batch of wafers (e.g., acts of God) do sometimes occur. The students are reminded that in the event of such a catastrophe, panic leading to careless laboratory conduct will only aggravate the situation. Remember, your safety (not the wafers' safety) is first and foremost!

Clean-Room Techniques

The cleanest room in the world cannot protect a wafer against the emissions from a human mouth. Should one decide to breathe or speak in close vicinity to a wafer, it is probably better to expectorate at the wafer so that wafer contamination becomes so clearly obvious that the wafer must be disposed of immediately. Also, remember that one fingerprint has enough sodium to "threshold-adjust" all your MOS gates and render them as valuable as the pile of sand from which they are derived. Gloved hands are unquestionably cleaner than uncovered hands, but consider what they have touched prior to your wafers. Watch your classmates and see how many times they touch their face or use the ink pen they brought in the fab without cleaning. The bottom line is "DO NOT TOUCH THE WAFERS" with any part (or former part) of your body, whether it is covered or not. Even if you do not come in contact with the wafers, there are certain lab practices one should follow to reduce particle counts in the laboratory. For instance, proper and complete gowning before entry into the laboratory is critical. In addition, while in the laboratory, rapid and abrupt motions (such as running or rushing) are considered intolerable because not only do they increase local particle counts by orders of magnitude, but also they are very unsafe!

As a final note, remember that the IC laboratory is a work environment where one has to work in cooperation with all other users of the facility. Hence, courtesy and cooperation with other fellow users is very important. Keep this is mind as you make your debut appearances into the clean room.

Photolithography

The EE410 NMOS-Depletion mode process uses conventional optical lithography techniques throughout the process flow. All masking steps use the SVG Coater, ASML stepper, and the SVG Developer. Students are asked to consult the respective manuals in the laboratory for more detailed information about equipment operation. The process intentionally uses several different common lithography-related concepts, in order to introduce students to as many different concepts as possible (i.e., etching and lift-off).

General Lithography Procedure

The procedure for standard photolithography steps is shown in Figure 1 with descriptions below. This is repeated many times throughout the entire process, so it is important that students are familiar with the basic photolithography steps.

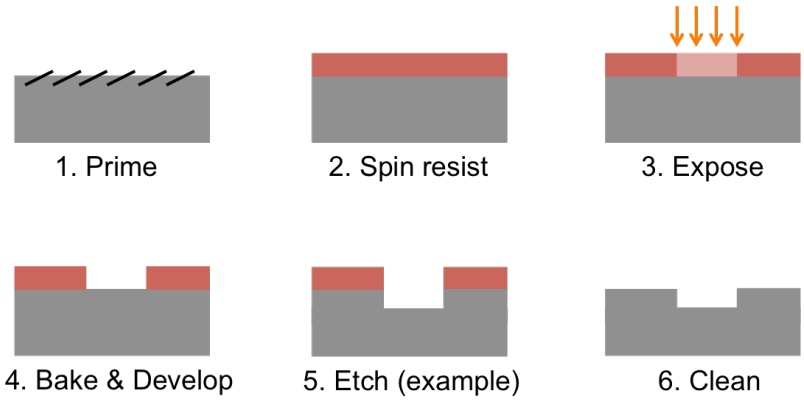


Figure 1. General Lithography Procedure

1. Wafers are first primed to remove any adsorbed moisture and then coated with HMDS for improved resist adhesion. (Equipment – Yes Oven). Without HMDS, small features of resist will not all adhere to the wafer, and will instead fly off while the wafer spins during development.
2. Positive resist is spun onto the wafers. (Equipment – SVG Resist Coater). In the EE410 process, the standard 3612 1µm thick resist is used.
3. The wafers are exposed using an ASML stepper (capable of 0.45µm resolution). The ASML mask levels used in the process is described in Table 1. (Equipment – ASML)
4. Wafers are post-exposed baked and developed (Equipment – SVG Developer)
5. Wafers are ready for subsequent processing such as implantation or etch. (In Figure 1, the patterned region is etched as an example.)
6. Resist is removed and wafers are cleaned.

Description of ASML Mask Levels

The six ASML mask levels in the NMOS-Depletion mode process are summarized in Table 1.

No.	Mask Level	Description
0	alignment	Defines global alignment marks for pattern registration
1	Vth implant	Defines P well for implant
2	Iso implant	Defines P+ isolation regime for implant
3	S/D implant	Defines N+ implant for source and drain contacts
4	S/D etch	Defines region to etch through oxide for subsequent metal deposition to contact the source and drain.
5	S/D/G metal	Final metal deposition, for source, drain, gate, probe pads, and connecting wires.

Table 1. Description of the five ASML mask levels in the NMOS-Depletion mode process.

Process Flow

The starting material for NMOS-Depletion mode is a 100 mm, <100>-oriented, Czochralski-grown p-type (boron doped) silicon substrate of 5 to 10 Ω-cm resistivity and 525 μm thickness. A K-prime wafer provides a higher doping substrate (~1E15 boron doping), and thus more positive $V_{threshold}$, while the L-prime wafers (~2E14 boron doping) provides a more negative $V_{threshold}$. Process details are described to provide students with sufficient knowledge to understand the purpose of each procedure. Students can also consult the process schedule and run sheet (provided as separate handouts) for further detail.

Step 0. Alignment Mark Definition

To use the automatic ASML Stepper to expose the wafers, ASML alignment marks must first be patterned onto the wafer in known locations, to provide a reference for the ASML stepper to use for all future processing steps. This is the standard first process for any wafer which uses the ASML Stepper for lithography. The layer containing the alignment marks is called the zero layer, because it precedes all device layers. Alignment can be done using between two and 200 alignment marks. The job file for EE410 uses all 4 alignment marks for alignment, but will complete a job if only 2 are acceptable (i.e. improper wafer handling can scratch or damage alignments, so be careful!). While ASML can align without alignment and instead use the wafer flat, the overlay accuracy with alignments is ~50 nm, while overlay accuracy with the wafer flat is several microns.

	Equipment	Purpose	Processing Details
1	YES Oven	prime wafers	
2	SVG Resist Coat	coat photoresist	Program 7 - PR 3612 1um w/o VP backside EBR only
3	ASML	expose	**wafers must be cleaned in SRD to minimize contamination in ASML* Mask: EE410_DepNMOS Jobfile: EE410/maxms Exposure dose: 50
4	SVG Developer	bake and develop	(Initial bake) Developer 9 / Hot plate 1 (Develop + post bake) Developer 3 / Hot plate 1
Check developed region under microscope.			
5	AMT Etcher	etch alignment marks	**season chamber for 5 minutes* Program 4 Etch time: 6 minutes
6	gasonics	remove (burn-off) photoresist using oxygen plasma	Program 013
Check etched alignment marks under microscope.			

Step 1. Oxide Growth

Silicon dioxide (SiO_2) is thermally grown, which will be used as the gate dielectric. Prior to loading the wafers into the furnace (i.e. Thermco1), it is essential to have very clean wafer surface. Otherwise, contaminants (such as mobile ions such as Potassium or Sodium) can diffuse very far distances, into the transistor channel, resulting in uncontrollable transistor performance. A schematic of the result is shown in Figure 2. In silicon transistors today, the SiO_2 gate dielectric would be replaced with a high-k gate dielectric, such as HfO_X (the exact gate stacks are highly classified secrets kept by foundries) for improved electrostatic control.

Figure 2. SiO_2 thermally grown on the silicon substrate

	Equipment	Purpose	Processing Details
1	wbnonmetal	wafer cleaning	i. Piranha (9:1 H2SO4:H2O2) 120°C for 20 minutes ii. Water dump rinser iii. 50:1 HF dip for 30 seconds iv. Water dump rinser v. SRD
2	wbclean		i. RCA clean (bath 1) 50°C for 10 minutes ii. Water dump rinser iii. 50:1 HF dip for 30 seconds iv. Water dump rinser v. RCA clean (bath 1) 50°C for 10 minutes vi. Water dump rinser vii. 50:1 HF dip for 30 seconds viii. Water dump rinser ix. SRD
3	Thermco1	thermal oxidation	900°C, 2hr:40min:00sec, dry oxidation Oxide thickness target ~30nm (If oxide is too thick (> 40 nm), etch bath in 50:1 HF in wbclean. Etch rate is ~ 4nm/min.)
Check oxide thickness using Nanospec or Woollam.			

Step 2. High V_T well implantation

Implantation in the well region is performed to adjust the threshold voltage (V_T) at which the device performs. In the NMOS-Depletion mode process, transistors with two different V_T's are required. Therefore, only one of the two transistors require the well implantation step, as shown in Figure 3. The other transistor uses the substrate doping of the silicon wafer to set its V_T. Most processes use a very low doped substrate (to minimize capacitance from wires to the substrate), and would use an implant to define the V_T for every group of transistors with the same V_T in the circuit. EE410 uses the substrate doping to simplify the processing steps at the cost of circuit performance (though not functionality). As an exercise, calculate the V_T range, given the range of doping levels from the wafer supplier for a K-prime and L-prime wafer (hint: you should find the V_T range is within a sufficient small range to not have a significant impact on circuit functionality).

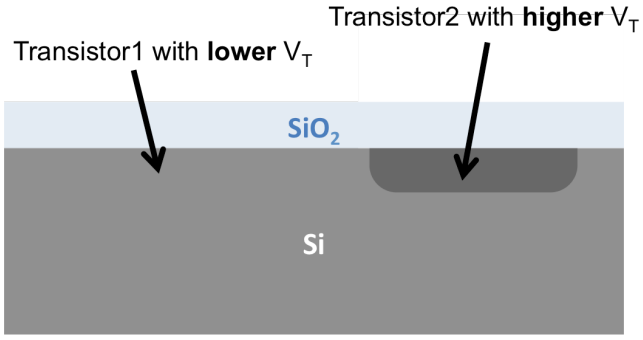


Figure 3. Two different wells are shown with higher V_T and lower V_T, where the higher V_T region is obtained by an implantation step.

	Equipment	Purpose	Processing Details
1	YES Oven	prime wafers	
2	SVG Resist Coat	coat photoresist	Program 7 - PR 3612 1um w/o VP backside EBR only
3	ASML	expose	**wafers must be cleaned in SRD to minimize particle contamination in ASML* Mask: Jobfile: Exposure dose: 50
4	SVG Developer	bake and develop	(Initial bake) Developer 9 / Hot plate 1 (Develop + post bake) Developer 3 / Hot plate 1
Check developed region under microscope.			
5	Oven 110°C	harden the resist so that it withstands the implantation	Bake for 30 minutes
6	Drytek2	descum (to remove residual photoresist before implantation)	**season chamber for 10 minutes* **make sure to use clean slots* Program 1 - pressure 150mTorr, oxygen

			flow 100sccm, power 250W (~0W reflected) for 40 seconds
7	Send out for Implantation	High V_T well implant	**The implantation is done outside of SNF* Boron 1e13 cm^{-2}, 60 keV, 7° tilt
8	gasonics	remove photoresist	Program 016
9	wbnonmetal	wafer cleaning	i. Piranha (9:1 H2SO4:H2O2) 120°C for 20 minutes ii. Water dump rinser iii. SRD

Step 3. Isolation P+ implantation

Boron (p-type dopant) is implanted in the isolation region, shown in Figure 4, to eliminate interaction between adjacent transistors.

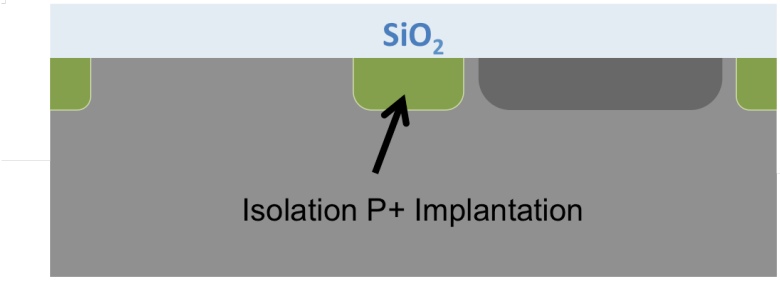


Figure 4. Isolation P+ implantation to eliminate interaction between adjacent transistors

	Equipment	Purpose	Processing Details
1	YES Oven	prime wafers	
2	SVG Resist Coat	coat photoresist	Program 7 - PR 3612 1um w/o VP backside EBR only
3	ASML	expose	**wafers must be cleaned in SRD to minimize particle contamination in ASML* Mask: Jobfile: Exposure dose: 50
4	SVG Developer	bake and develop	(Initial bake) Developer 9 / Hot plate 1 (Develop + post bake) Developer 3 / Hot plate 1
Check developed region under microscope.			
5	Oven 110°C	harden the resist	Hard bake for 30 minutes
6	Drytek2	descum	**season chamber for 10 minutes* **make sure to use clean slots* Program 1 - pressure 150mTorr, oxygen flow 100sccm, power 250W (~0W reflected) for 40 seconds
7	Send out for Implantation	Isolation P+ implant	**The implantation is done outside of SNF* Boron 5e15 cm^{-2}, 60 keV, 7° tilt
8	gasonics	remove photoresist	Program 017
9	wbnonmetal	wafer cleaning	i. Piranha (9:1 H2SO4:H2O2) 120°C for 20 minutes ii. Water dump rinser iii. SRD
8	gasonics	remove photoresist	**Reason for performing a more thorough clean: It is difficult to clean the photoresist after implanting boron with high dose of 5e15 cm^{-2}. Therefore, we make sure by running the clean in gasonics once more.* Program 013

Step 4. Source/Drain N+ implantation

The source and drain regions are defined in both transistors with high V_T and low V_T. Arsenic (n-type dopant) is chosen since it is a slow diffuser.

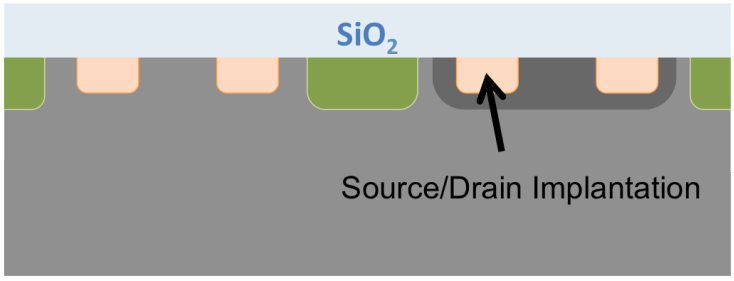


Figure 5. Source and drain (N+) implantation

	Equipment	Purpose	Processing Details
1	YES Oven	prime wafers	
2	SVG Resist Coat	coat photoresist	Program 7 - PR 3612 1um w/o VP backside EBR only
3	ASML	expose	**wafers must be cleaned in SRD to minimize particle contamination in ASML* Mask: Jobfile: Exposure dose: 50
4	SVG Developer	bake and develop	(Initial bake) Developer 9 / Hot plate 1 (Develop + post bake) Developer 3 / Hot plate 1
Check developed region under microscope.			
5	Oven 110°C	harden the resist	Hard bake for 30 minutes
6	Drytek2	descum	**season chamber for 10 minutes* **make sure to use clean slots* Program 1 - pressure 150mTorr, oxygen flow 100sccm, power 250W (~0W reflected) for 40 seconds
7	Send out for Implantation	Source/Drain implant	**The implantation is done outside of SNF* Arsenic 2e15 cm^{-2}, 60 keV, 7° tilt
8	gasonics	remove photoresist	Program 017
9	wbnonmetal	wafer cleaning	i. Piranha (9:1 H2SO4:H2O2) 120°C for 20 minutes ii. Water dump rinser iii. SRD
10	gasonics	remove photoresist	**Reason for performing a more thorough clean: It is difficult to clean the photoresist after implanting boron with high dose of 5e15 cm^{-2}. Therefore, we make sure by running the clean in gasonics once more.* Program 013

Step 5. Anneal – Drive in dopants

The flash anneal is performed to drive in the dopants and to heal the oxide that was damaged by the implantation. The regions implanted with boron (High V_T Well and Isolation) are driven-in deeper than that with arsenic (Source/Drain) since arsenic diffuses slower, as shown in Figure 6 and 7 (Sentaraus simulations). The anneal is in nitrogen as an inert gas, as well as 1 sccm flow of oxygen (to heal damage in the oxide caused by the high energy implant through the oxide). Normally, a sacrificial oxide layer is used, and after the implant, that oxide is stripped, and a high-k dielectric is grown over the exposed silicon. To simplify the process, we only grow/ deposit a single oxide layer.

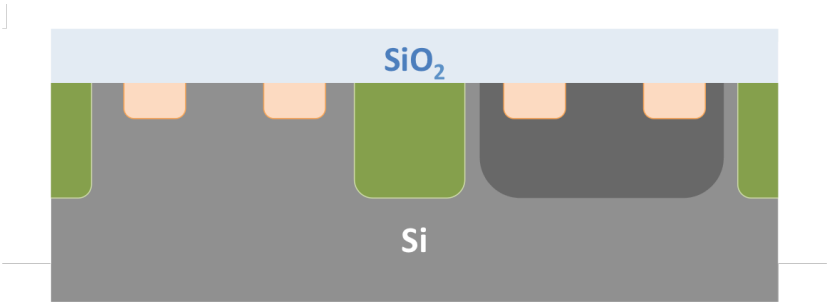


Figure 6. A flash anneal is performed to drive in the implants.

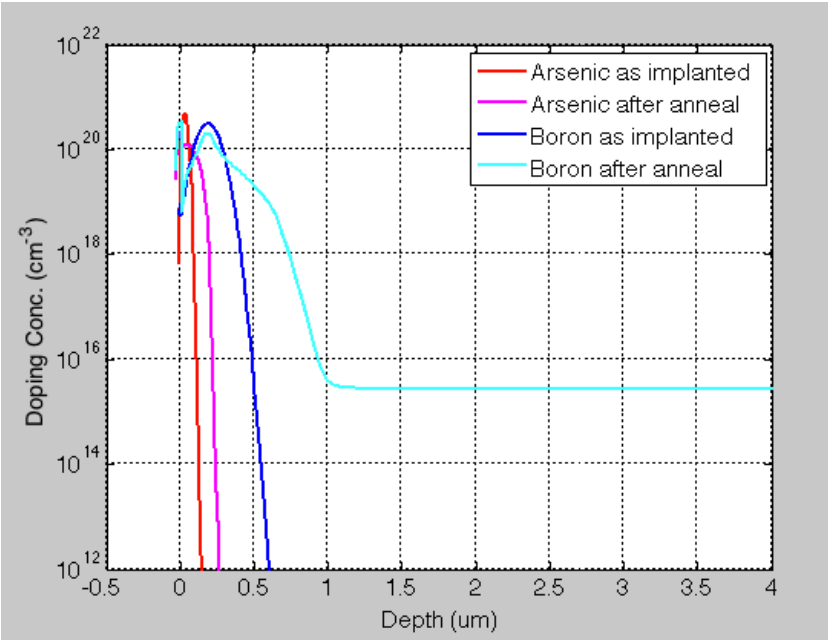


Figure 7. This is an example of dopant diffusion before and after flash anneal using arbitrary conditions. Note that the boron is diffused deeper into the substrate than the arsenic. Students are encouraged to simulate the dopant implantation and diffusion using Sentaurus.

	Equipment	Purpose	Processing Details
1	RTA-L	drive-in & oxide heal	Anneal 15 seconds, 1050°C 10 Argon flow + 1 Oxygen flow

Step 6. Source/Drain contact etch

Contact holes are etched through the SiO_2 layer to expose the source and drain regions as shown in Figure 8.

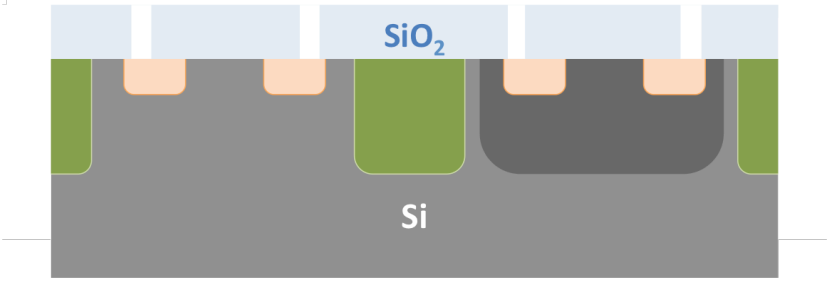


Figure 8. Etched contact holes exposing the source and drain region.

	Equipment	Purpose	Processing Details
1	YES Oven	prime wafers	
2	SVG Resist Coat	coat photoresist	Program 7 - PR 3612 1um w/o VP 2mm EBR
3	ASML	expose	**wafers must be cleaned in SRD to minimize particle contamination in ASML* Mask: Jobfile: Exposure dose: 50
4	SVG Developer	bake and develop	(Initial bake) Developer 9 / Hot plate 1 (Develop + post bake) Developer 3 / Hot plate 1
Check developed region under microscope.			
6	Drytek2	descum	**season chamber for 10 minutes* **make sure to use clean slots* Program 1 - pressure 150mTorr, oxygen flow 100sccm, power 250W (~0W reflected) for 40 seconds
8	P5000	etch contact holes	**make sure the conditions are correct. People make changes to the recipes.* Program surromed, 160 seconds, chamber B
9	wbnonmetal	wafer cleaning	i. Piranha (9:1 H2SO4:H2O2) 120°C for 20 minutes ii. Water dump rinser iii. 50:1 HF dip for 20 seconds iv. Water dump rinser v. SRD
Check etched region under microscope.			

Step 7. Source/Drain and Gate metal deposition

By now, students are probably familiar with standard photolithography, since the process was repeated four times! But the photolithography step required for metal deposition is slightly different from what was mentioned above. An additional lift-off layer (LOL2000) is spun on the wafer to prevent sidewall metal deposition. Figure 9 compares the metal deposition without the additional layer ("single" layer) and with the addition layer ("dual" layer).

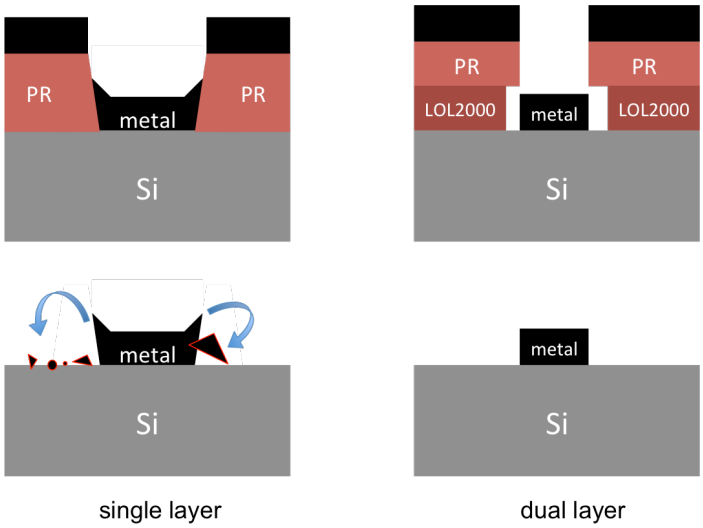


Figure 9. Comparison of metal deposition and lift-off on a single layer (photoresist layer only) and on a dual layer (photoresist and lift-off layer). Photoresist (Shipley 3612) is removed by acetone and LOL2000 is removed by remover PG.

The sidewall from the single layer may peel off in subsequent processing, resulting in particulates and shorts, or it may flop over and interfere with etches or depositions that follow. Therefore, it is important to use the dual layer processing prior to metal deposition, as the lift-off will result in better pattern definition with smoother and better-defined side-walls. The final schematic of the device structure using the NMOS-Depletion mode process is shown in Figure 10.

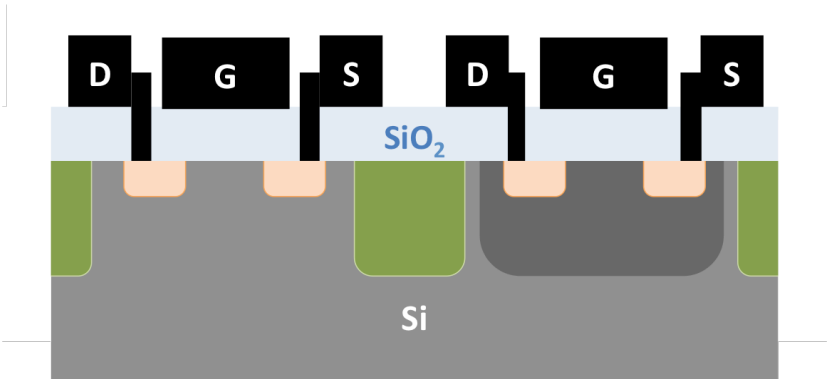


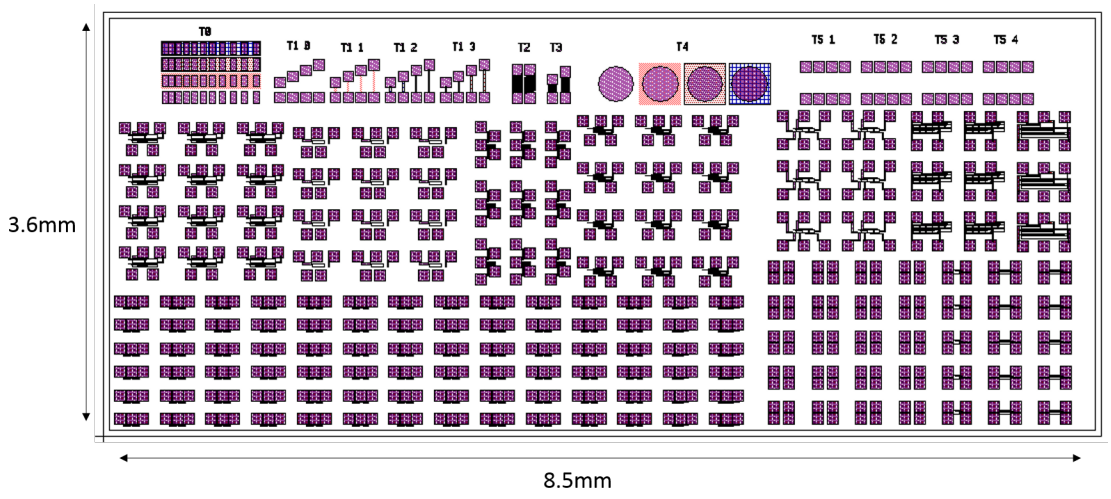
Figure 10. Final device structure after metal deposition and liftoff for source, drain, and gate metal contacts.

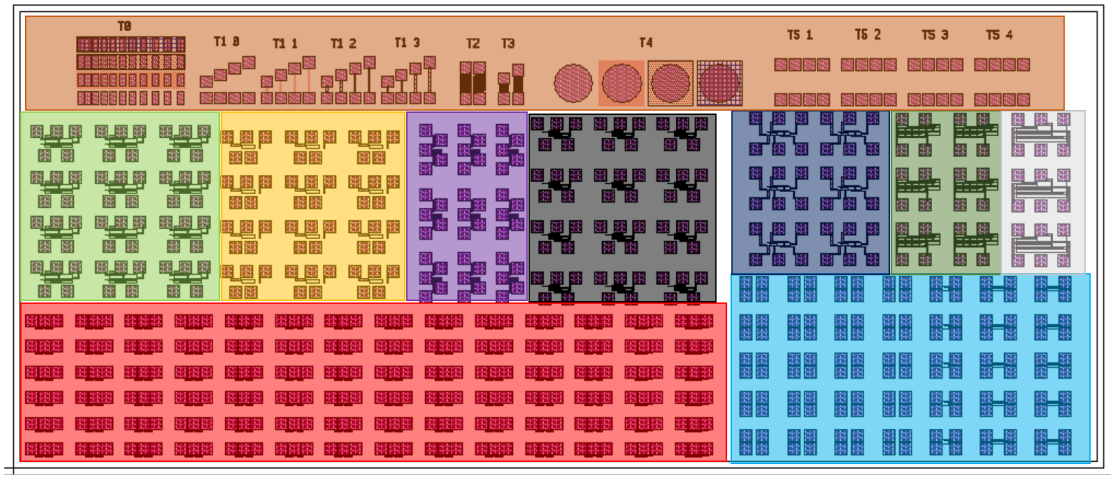
	Equipment	Purpose	Processing Details
1	Headway2	coat LOL2000	**use a filter to make sure the LOL2000 spun on the wafers is clean. Also, remove any large particles on the wafers using nitrogen blowgun.* 3000 rpm, 60 seconds
2	"White" oven	bake LOL2000	**This is a critical step, as the temperature determines the amount of undercut.* **"White" oven is actually green.* Load at 125°C, and after closing the door, set the temperature to 195°C. The total time the wafer is in the oven should be timed 23 minutes.
3	SVG Resist Coat	coat photoresist	Program 7 - PR 3612 1um w/o VP 2mm EBR
4	ASML	expose	**wafers must be cleaned in SRD to minimize particle contamination in ASML* Mask: Jobfile: Exposure dose: 50
5	SVG Developer	bake and develop	(Initial bake) Developer 9 / Hot plate 1 (Develop + post bake) Developer 5 / Hot plate 1 - Change program 5 steps 4 and 7 from 22 seconds to 21 seconds. (Don't forget to change it back!)
Check developed region under microscope.			
6	Drytek2	descum	**season chamber for 10 minutes* Program 1 - pressure 150mTorr, oxygen flow 100sccm, power 250W (~0W reflected) for 40 seconds
7	Innotec	metal deposition	**right before loading wafers in Innotec, immerse the wafers in 50:1 HF dip for 30 seconds, followed by water bath, then hand-dry with nitrogen blowgun. This is to remove any oxide that was formed from the oxygen plasma (Drytek2).* 5 nm Titanium and 40 nm Platinum
8	wbsolvent	lift-off	i. Acetone: 5 minutes (with sonication) ii. Remover PG: 20 minutes iii. IPA: 5 minutes iv. Blowdry with nitrogen gun
Check metal lift-off under microscope.			
9	RTA-R	anneal defects	Anneal 10 minutes, 350°C, 10 forming gas flow
Measure!			

Test Structures

Here we give a brief overview of the die layout and basic test structures. Please refer to the testing document for details about how to test your circuits.

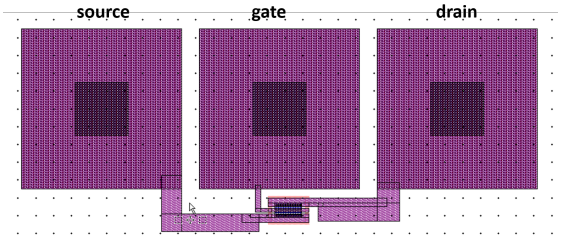
The top section of the die has several different test structures:
1) TLM structures for extract contact resistance, from the metal layer to all 4 doping levels.
2) Resistance lines: two metal pads are connected to a doped wire of silicon (all 4 doping levels), across several different lengths of the silicon doped wire. This can extract contact resistance, doping levels, etc.
3) Lithography tests: 600nm, 1um, and 2um resolution tests. Inter-digitated fingers to test no shorts after lift-off, and continuity tests to make sure no breaks in metal lines.
4) MOSCAPs (150um radium) on the 4 different doping levels.
5) contact chains, from the metal to the doped silicon, across all 4 different doping levels.



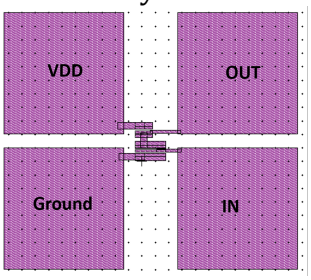


Transistor array
Inverter array
D-latch array
Nor2 array
Nand2 array
Xor2 array
Mux2 array
Ring oscillators (sized 3:1) array
Ring oscillators (sized 8:1) array
Test structures

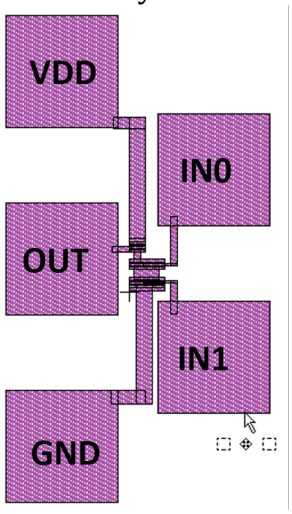
Transistor layout:



Inverter layout:



NAND2 Layout



NOR2 Layout