EE412 project:

Surface micromachining method for releasing a range of micron-scale membranes

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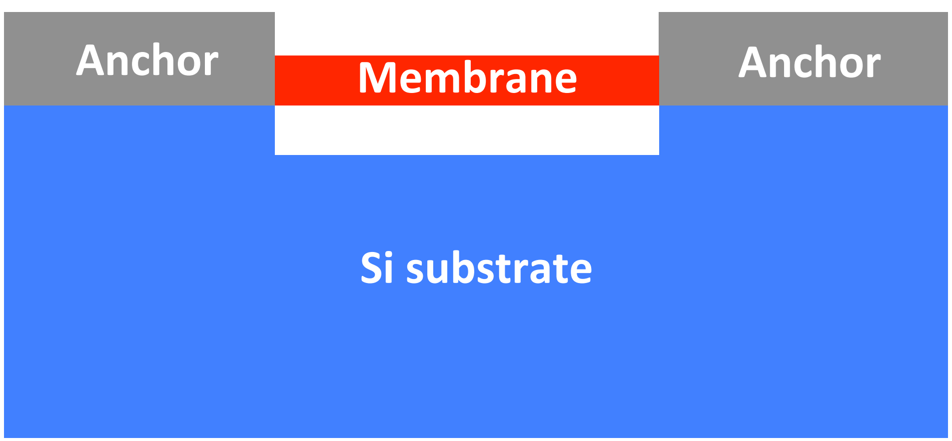
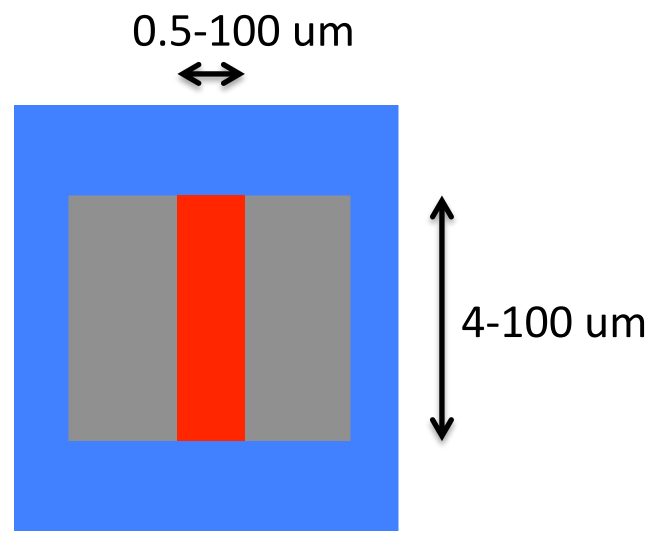
Fabrication Goal

- Fabricate and release membrane with…
  - thickness 10-100 nm
  - rectangular shape
  - lateral dimensions 0.5-100 um



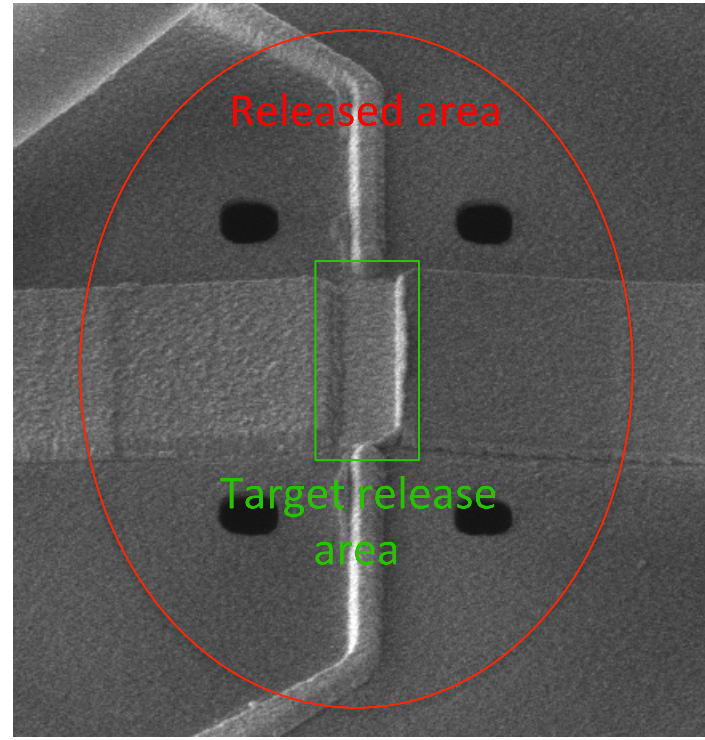
Cross-section

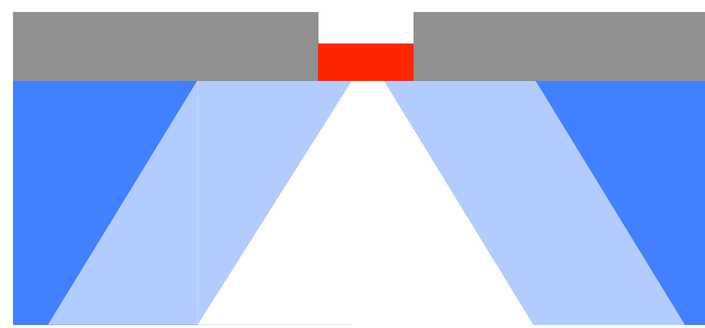


Top view

“Classical” methods to achieve release

- Passivation, holes & XeF_2 etch
  - Problem: releases much larger area than membrane
- Backside KOH/TMAH etch
  - Problem: Wafer thickness tolerance leads to >10 um lateral uncertainty
- Backside DRIE
  - Problems etching through wafer for <10 um opening
- SOI & backside litho on bottom of device layer
  - expensive & complex



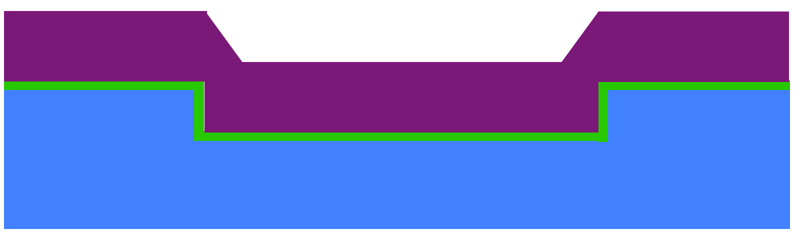


Proposed solution: build your own etch “sandbox”

1. Silicon RIE

2. Al_2O_3 ALD

3. poly-Si LPCVD



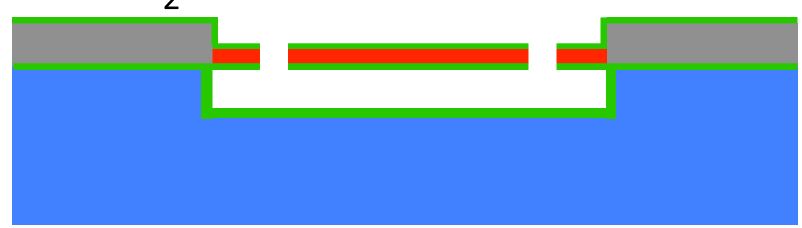
4. CMP

5. Al_2O_3 ALD

6. Membrane dep + Al_2O_3 ALD

7. Breakthrough etch

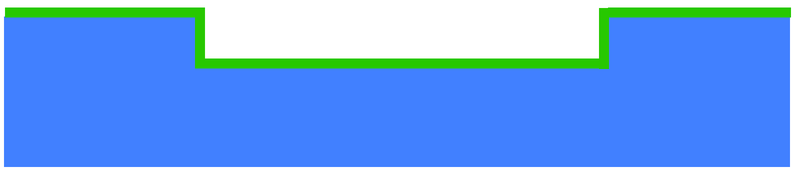
8. XeF_2 release



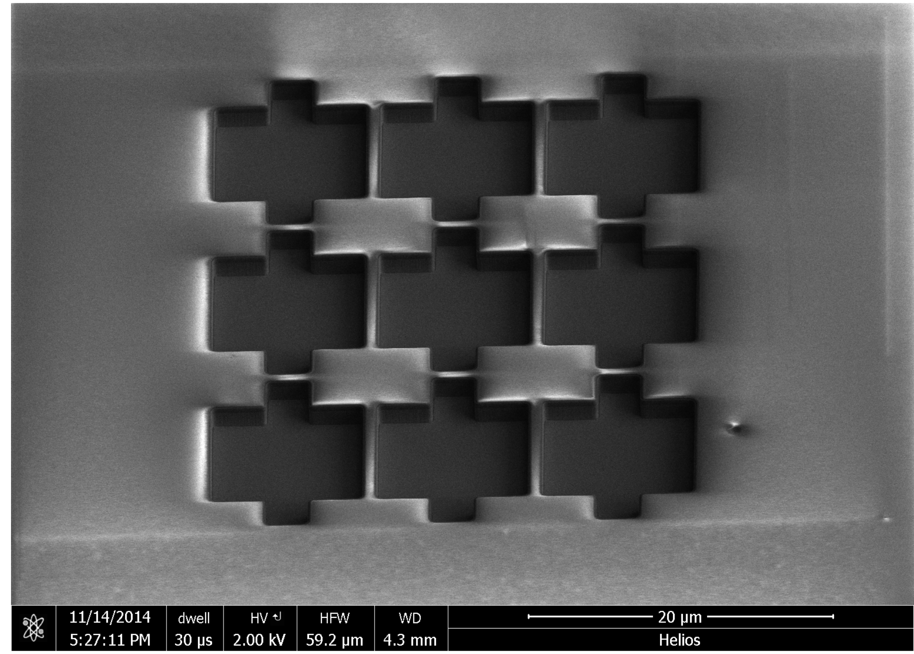
Box fabrication

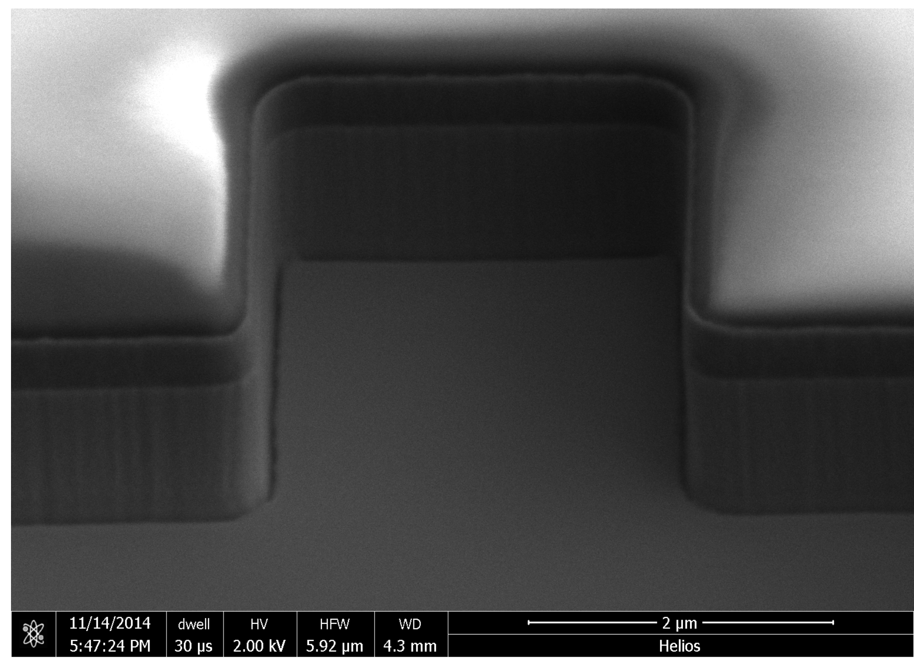
1. Silicon RIE

2. Al_2O_3 ALD

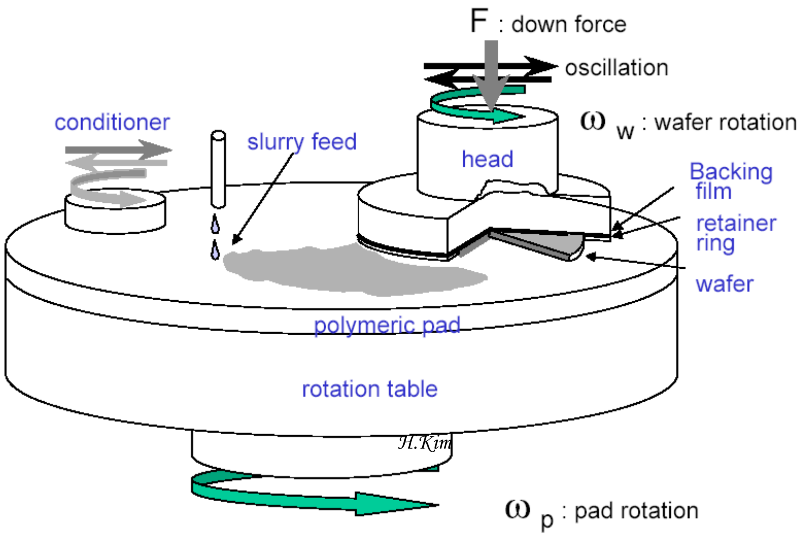


- lampoly for RIE
- fiji1/2/3 for ALD
- 250 nm,
  1 um,
  4 um depth





Polysilicon CMP

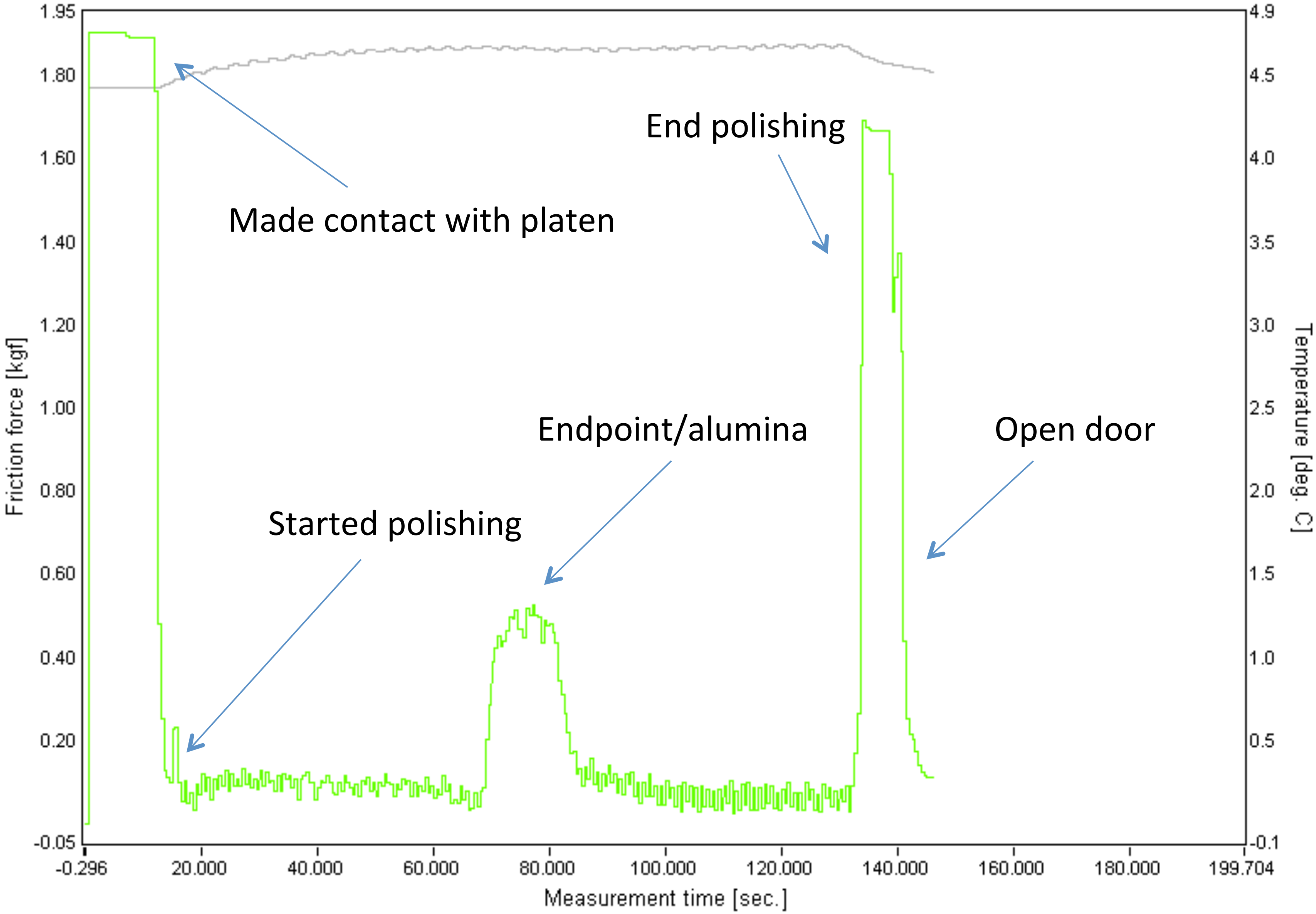


3. poly-Si LPCVD

4. CMP

- Possible to stop on Al_2O_3 layer?
- Repeatability?
- Uniformity?
- Dishing?
- Endpoint detection?

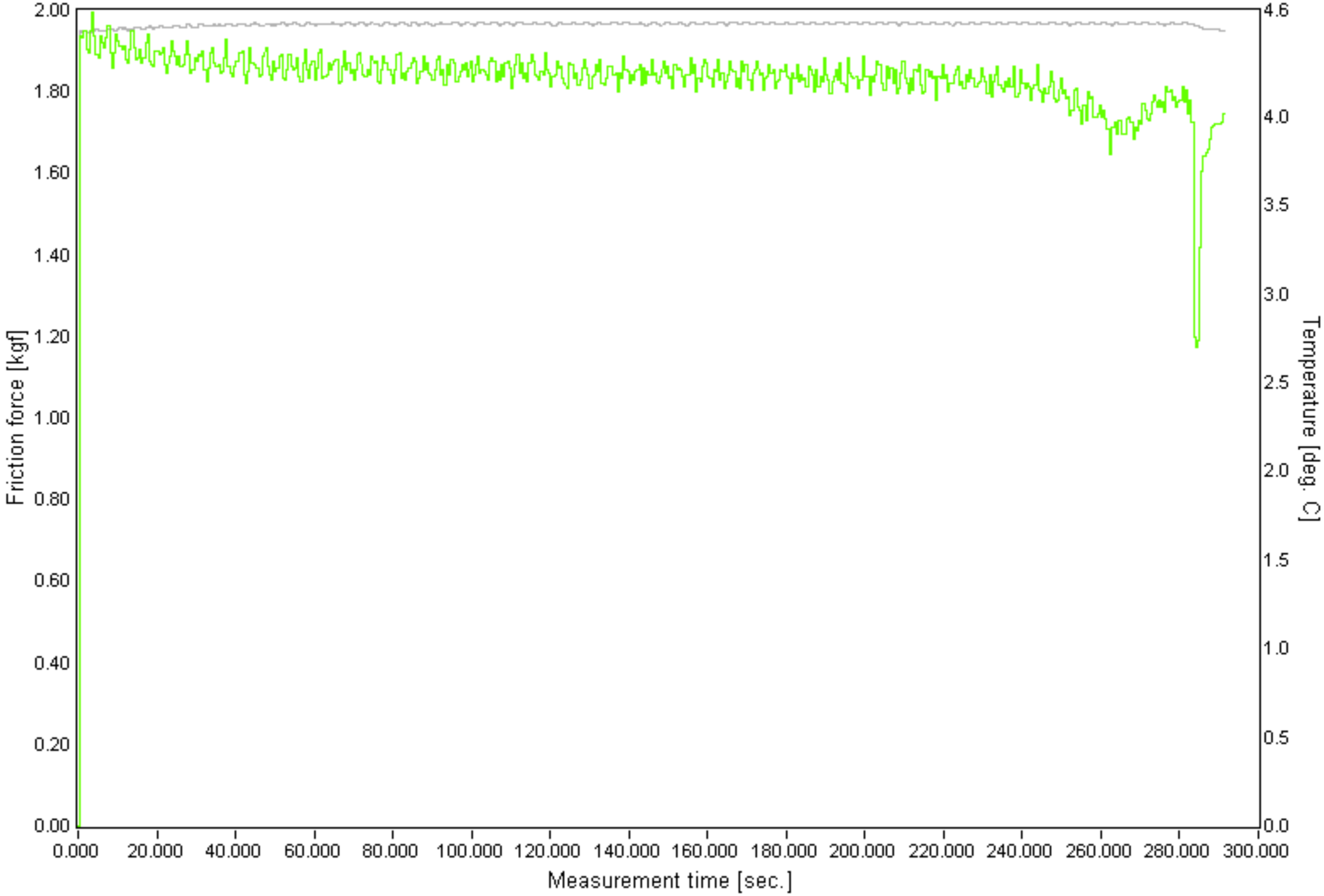
Endpoint detection



CMP Endpoint Visibility

Al_2O_3 vs poly thickness	250 nm	1 um	4 um
5 nm			
10 nm			
20 nm			
50 nm			

Endpoint 5nm Al_2O_3 + 1um poly-Si



ALD Al_2O_3 as polish stop

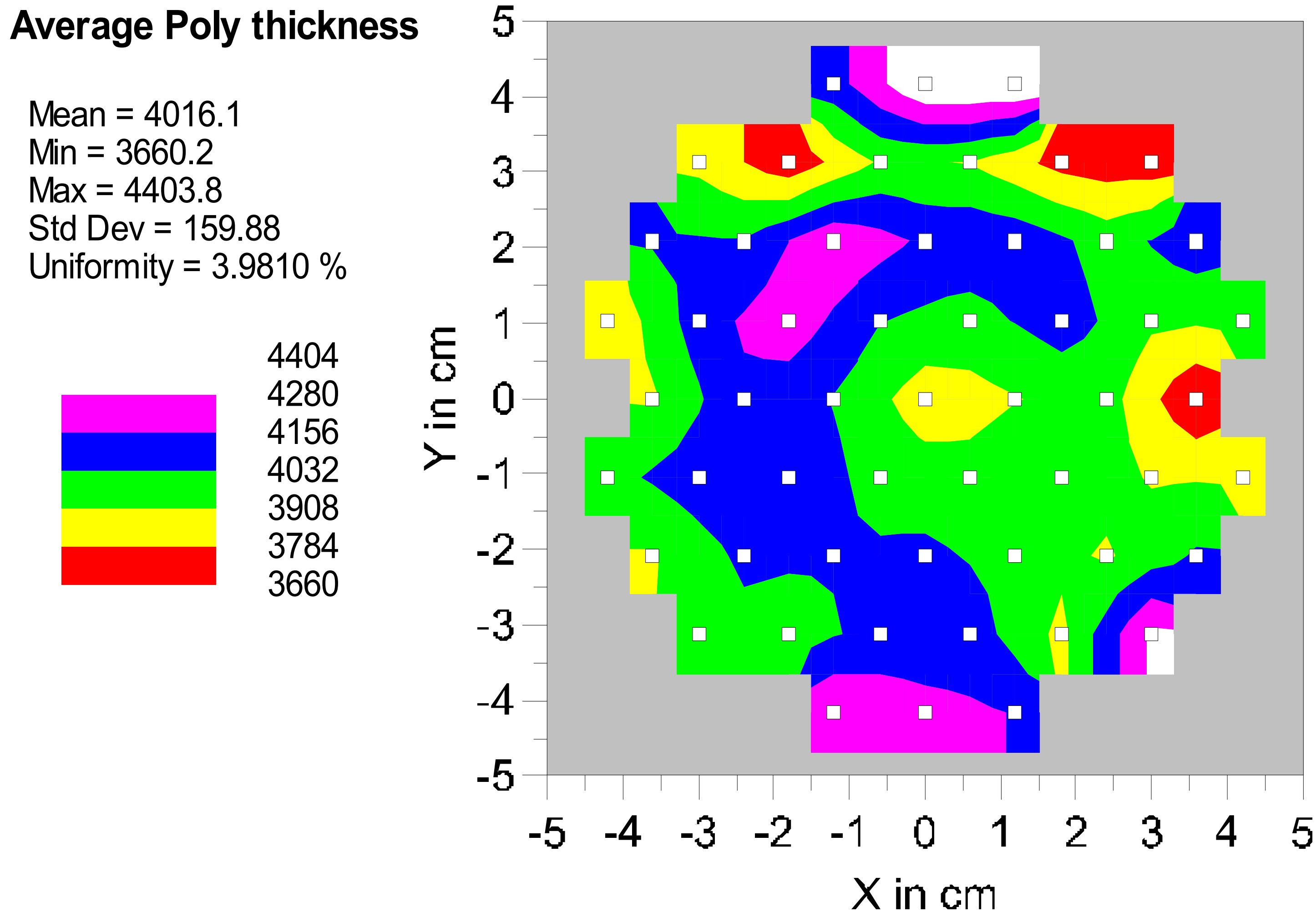
Polish rates

- Poly-Si: 3.2 nm/s – 3.8 nm/s
- $Al_2O_{3:}$ 1.3 nm/s

Al_2O_3 vs poly thickness	250 nm	1 um	4 um
5 nm			
10 nm			
20 nm			
50 nm			

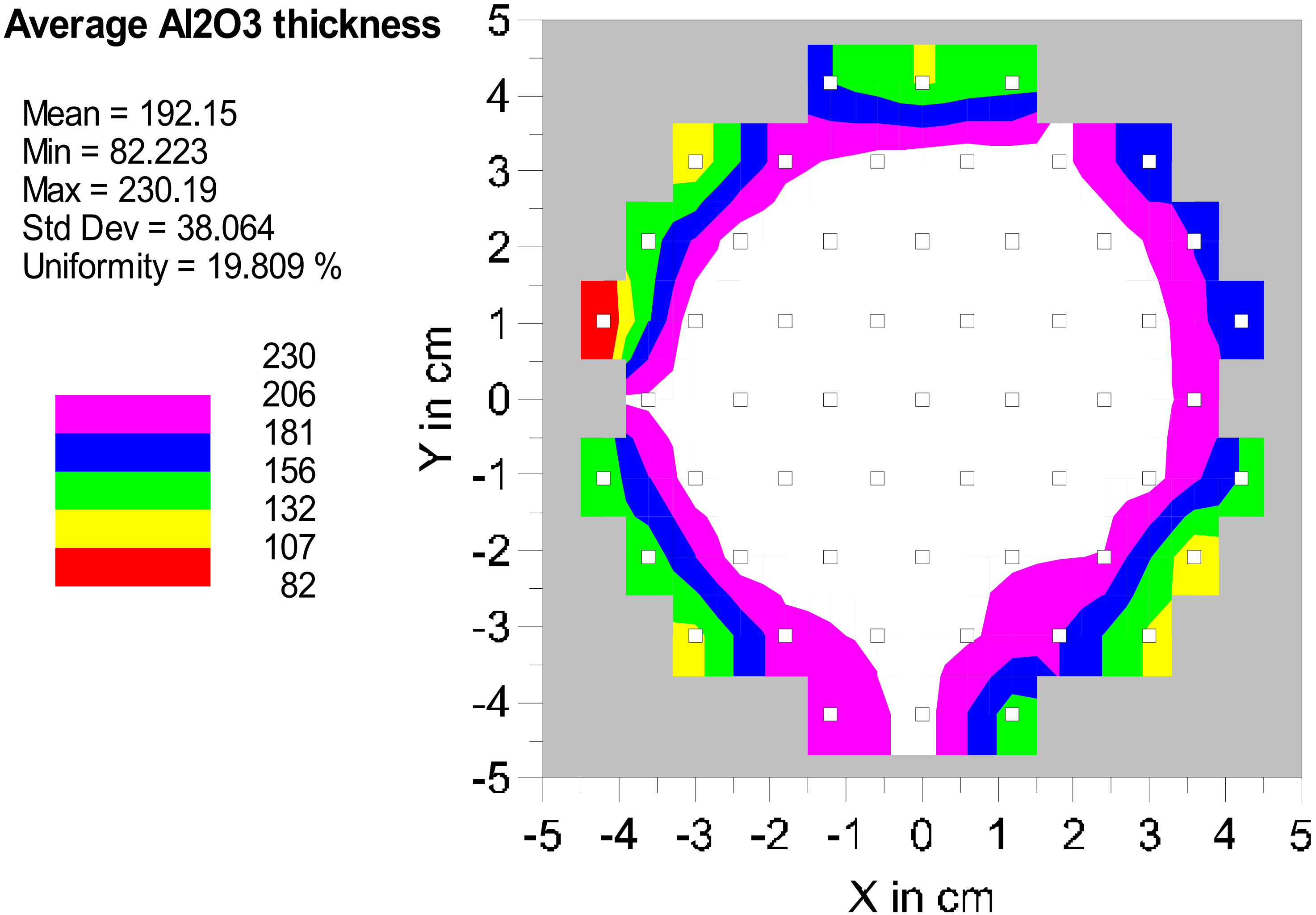
Residual thickness measurements with woollam

Polysilicon CMP uniformity



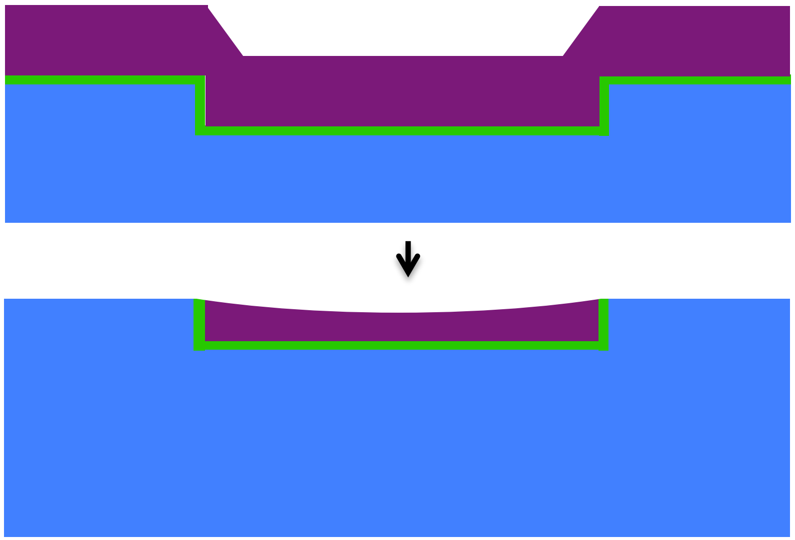
Starting thickness 1 um => Uniformity 2.6%

Al_2O_3 CMP uniformity (Si slurry)



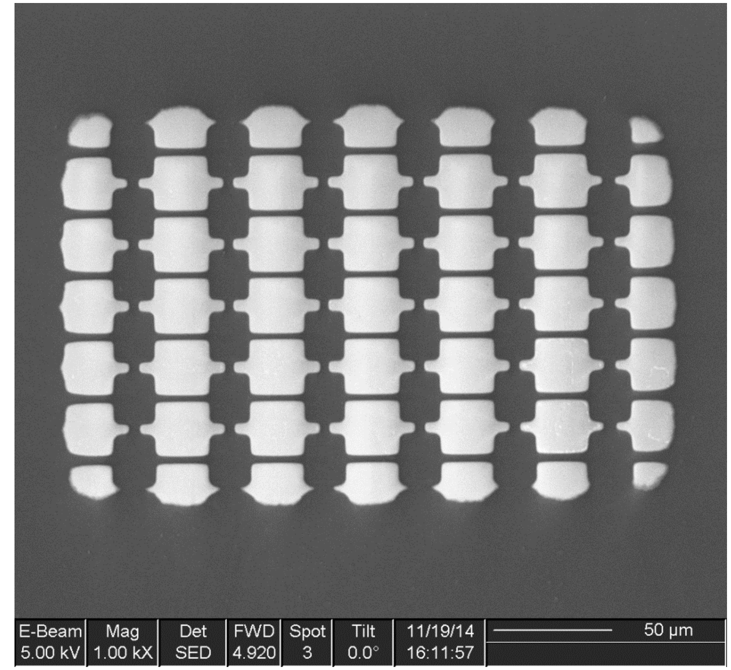
Starting thickness 50 nm => Uniformity 12.4%

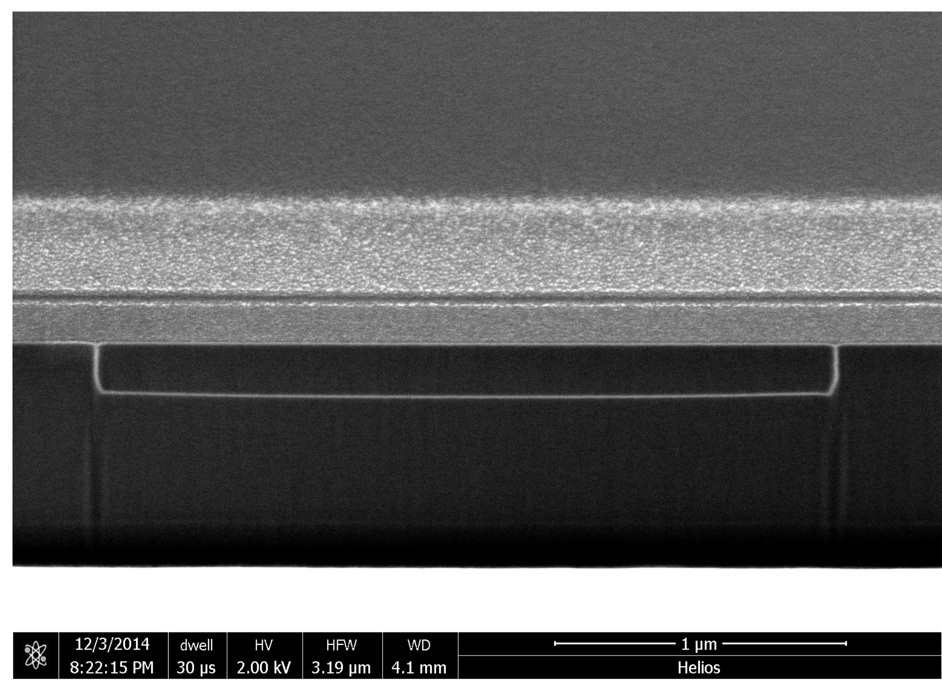
Dishing



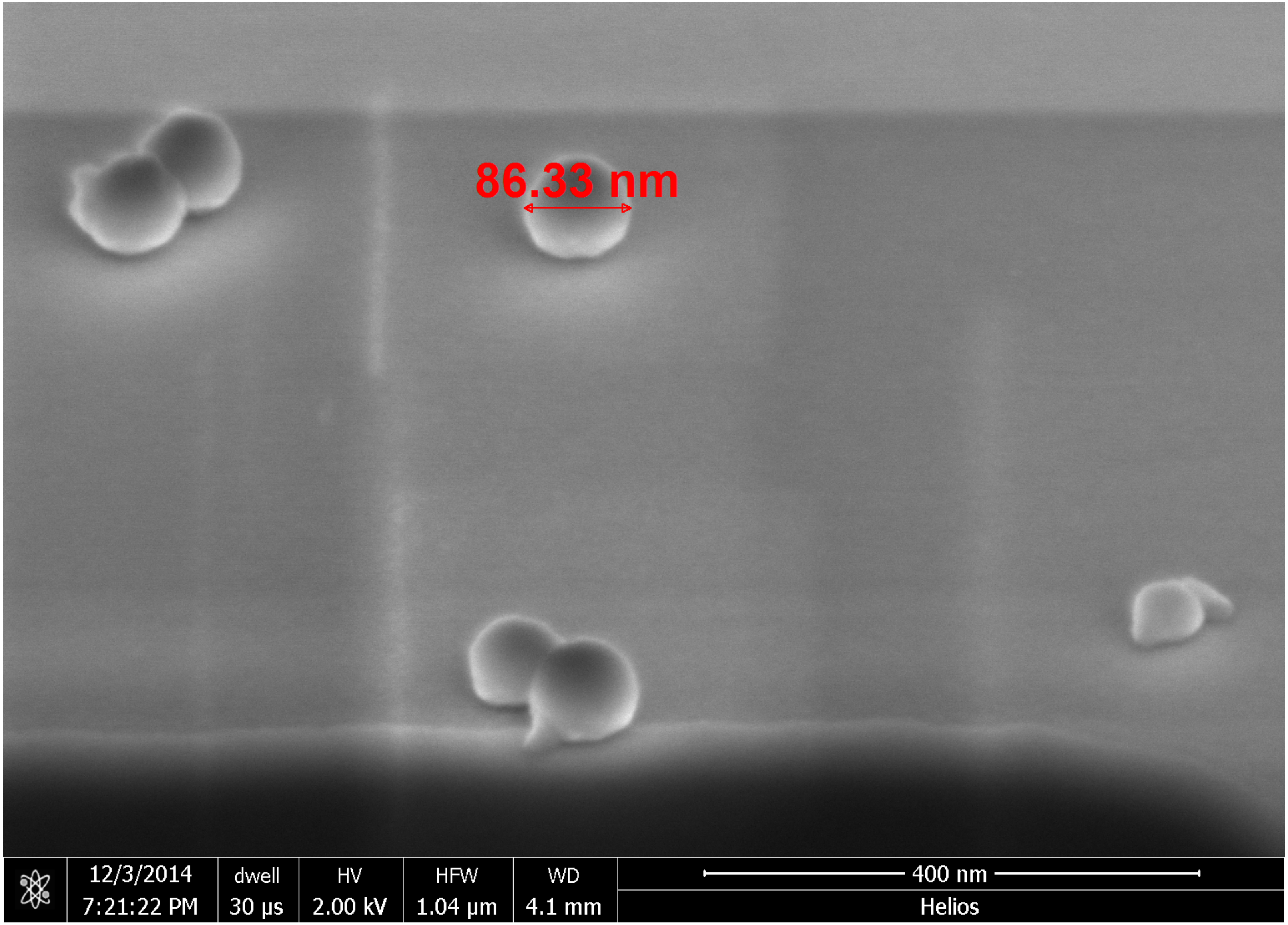
Investigate effects of
- size
- shape
- spacing
- array size
- dummy boxes

=> > 50 mask variations





Other CMP issues



ASML alignment marks & CMP

XPA mark depth	before CMP	after CMP
120 nm		
250 nm		
1 um		
4 um		

3. poly-Si LPCVD

4. CMP

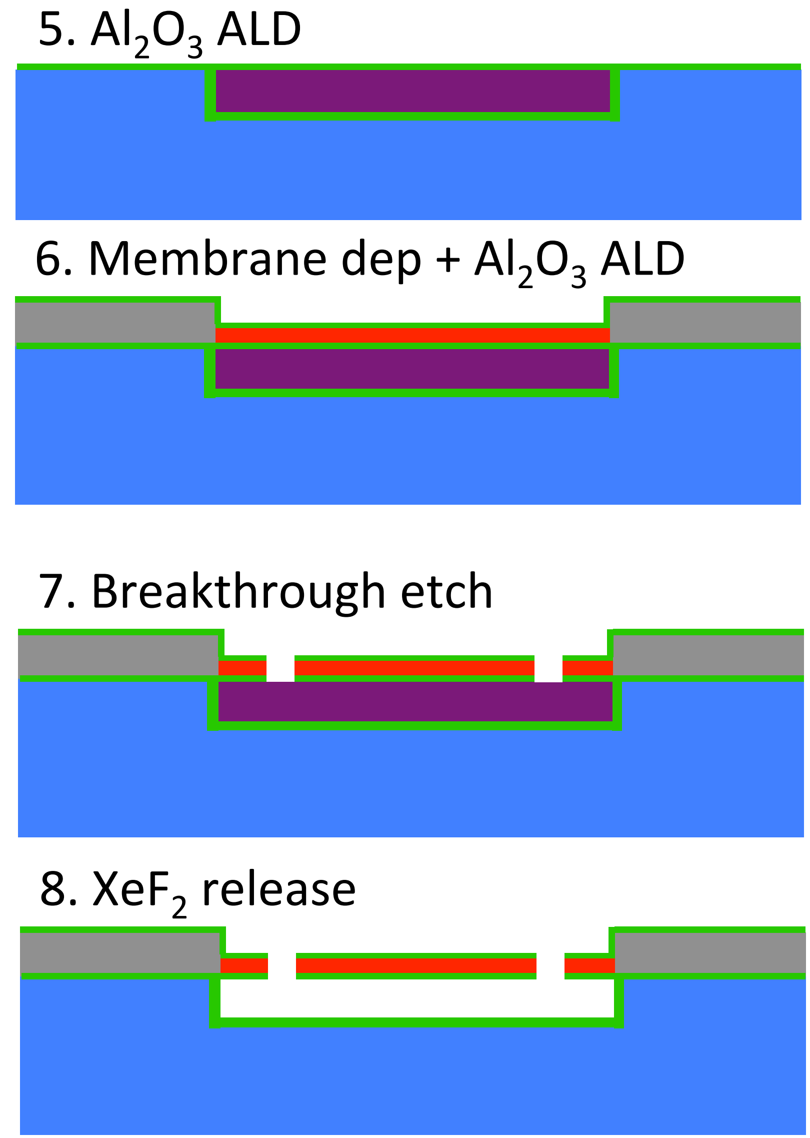
- backup marks further inside advisable due to CMP nonuniformity around edge
- possible issue later with reflective layer

2^{nd} and 3^{rd} ALD layer thickness

Determined by…

- Selectivity towards poly-Si in XeF_2
- Minimum pinhole-free cycle number

XeF_2 etch rate not measureable with woollam



ALD Al_2O_3 thickness vs. pinholes

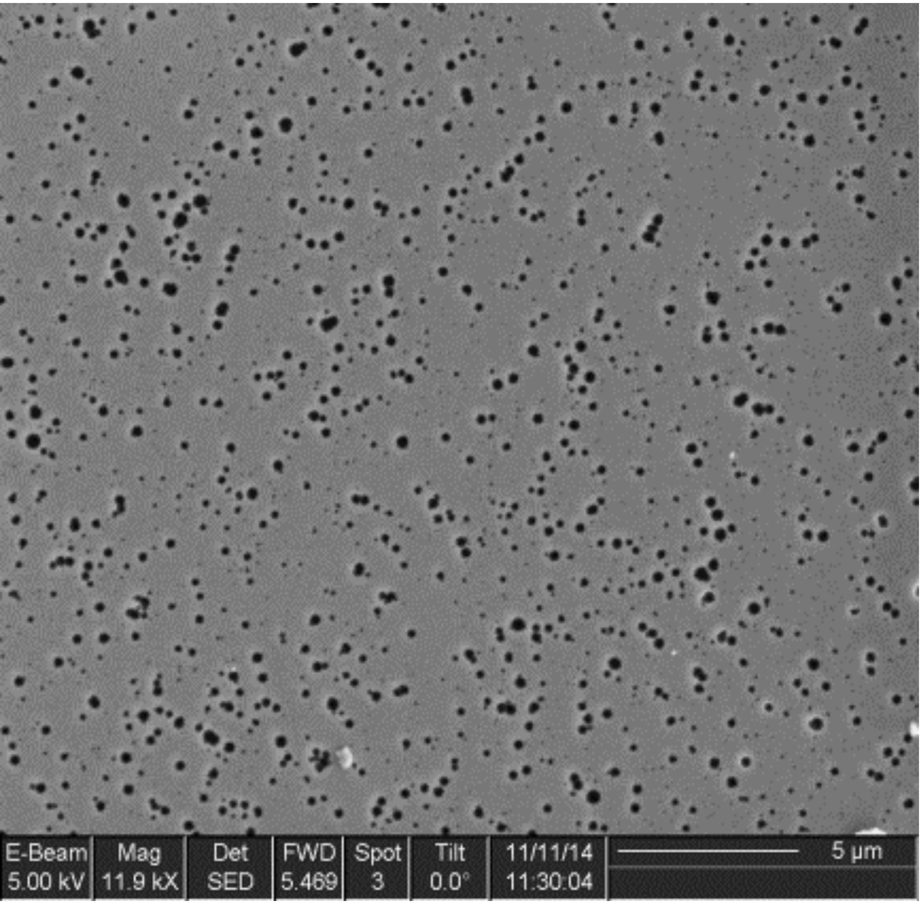
Previous EE412:

- test on savannah
- thermal ALD
- XeF_2 etch afterwards
- observed pinholes at 10 cycles (10 A), no pinholes at 20 cycles and above

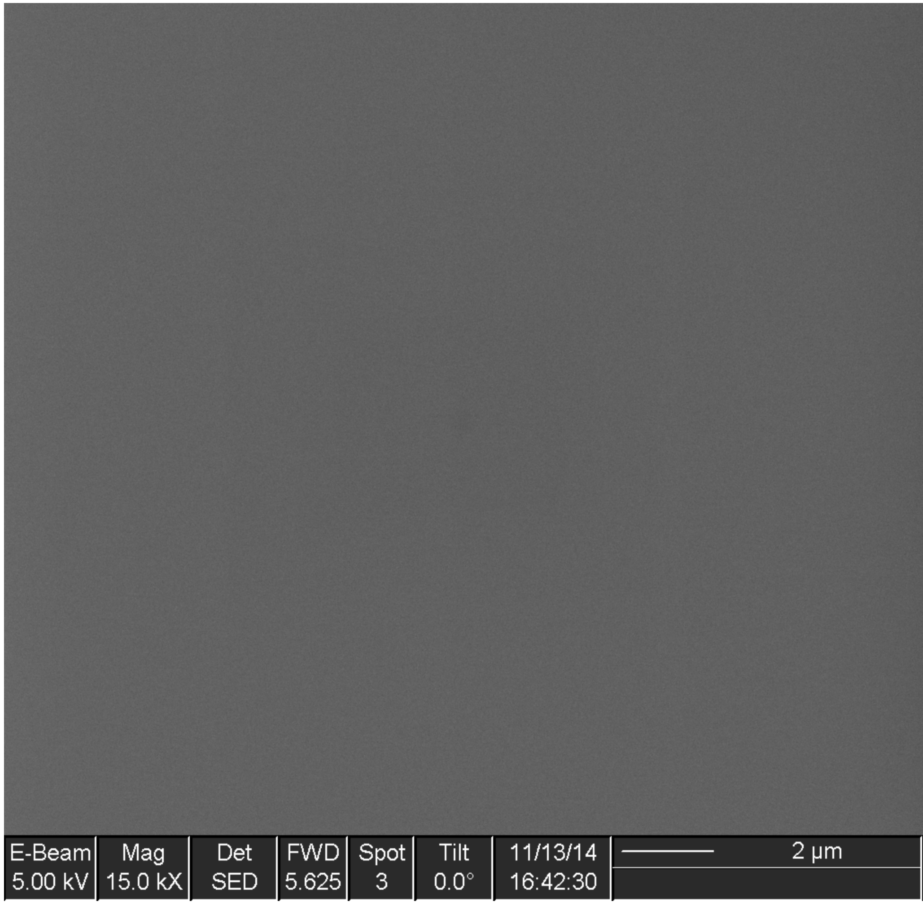
fiji2	10 (red)	11 (red)	12 (red)	13 (red)	14 (red)	15 (green)

fiji3	5 (red)	6 (red)	7 (red)	8 (red)	9 (green)	10 (green)	11 (green)	12 (green)	13 (green)	14 (green)	15 (green)

fiji2 Plasma Al_2O_3 ALD after 30 cycles XeF_2

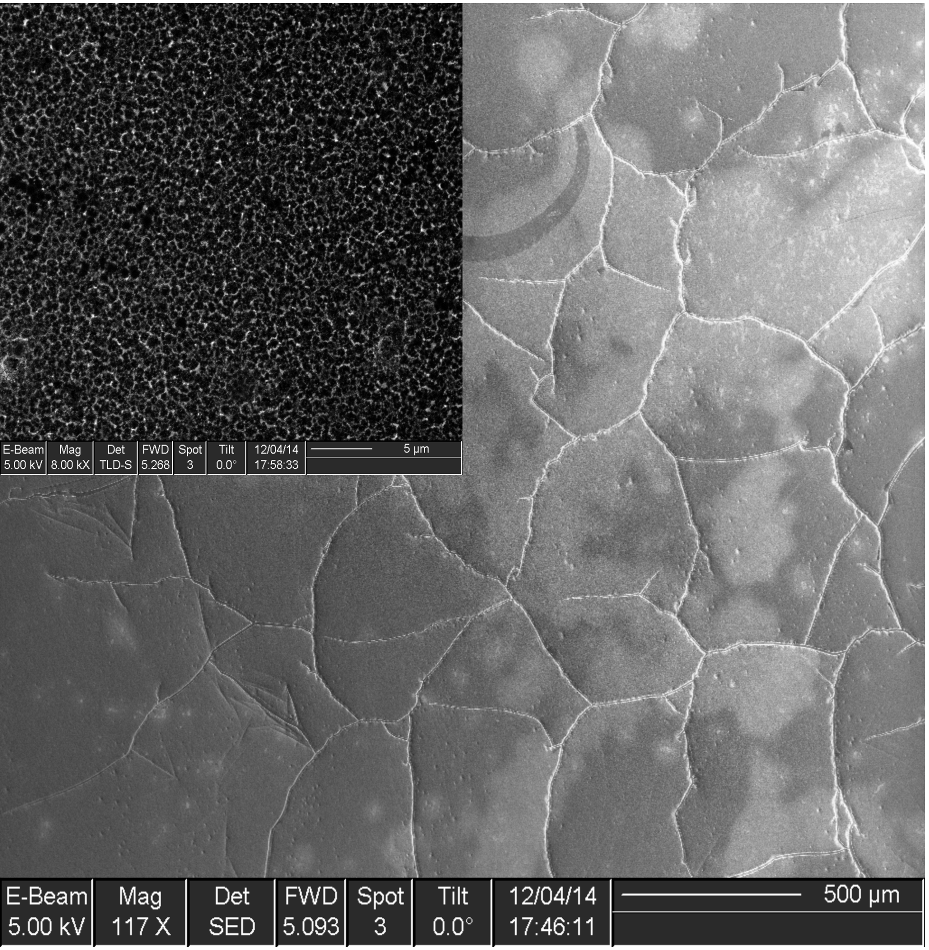


14 TMA cycles

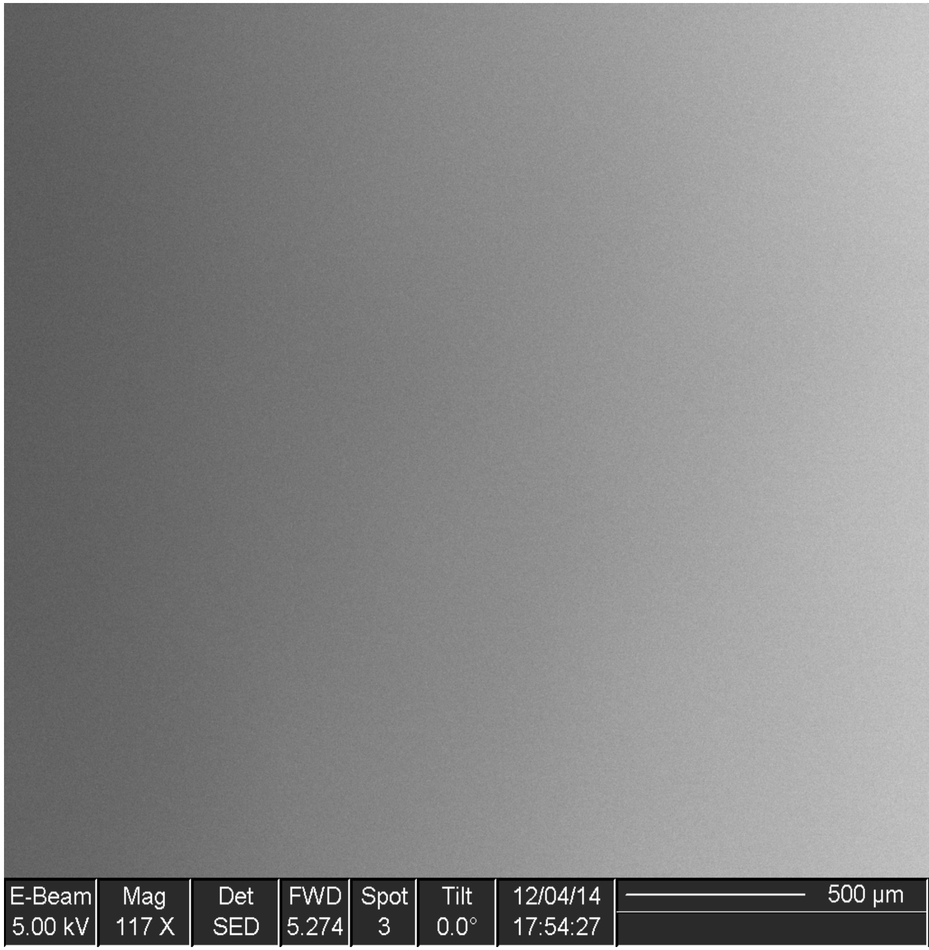


15 TMA cycles

fiji3 Plasma Al_2O_3 ALD after 30 cycles XeF_2

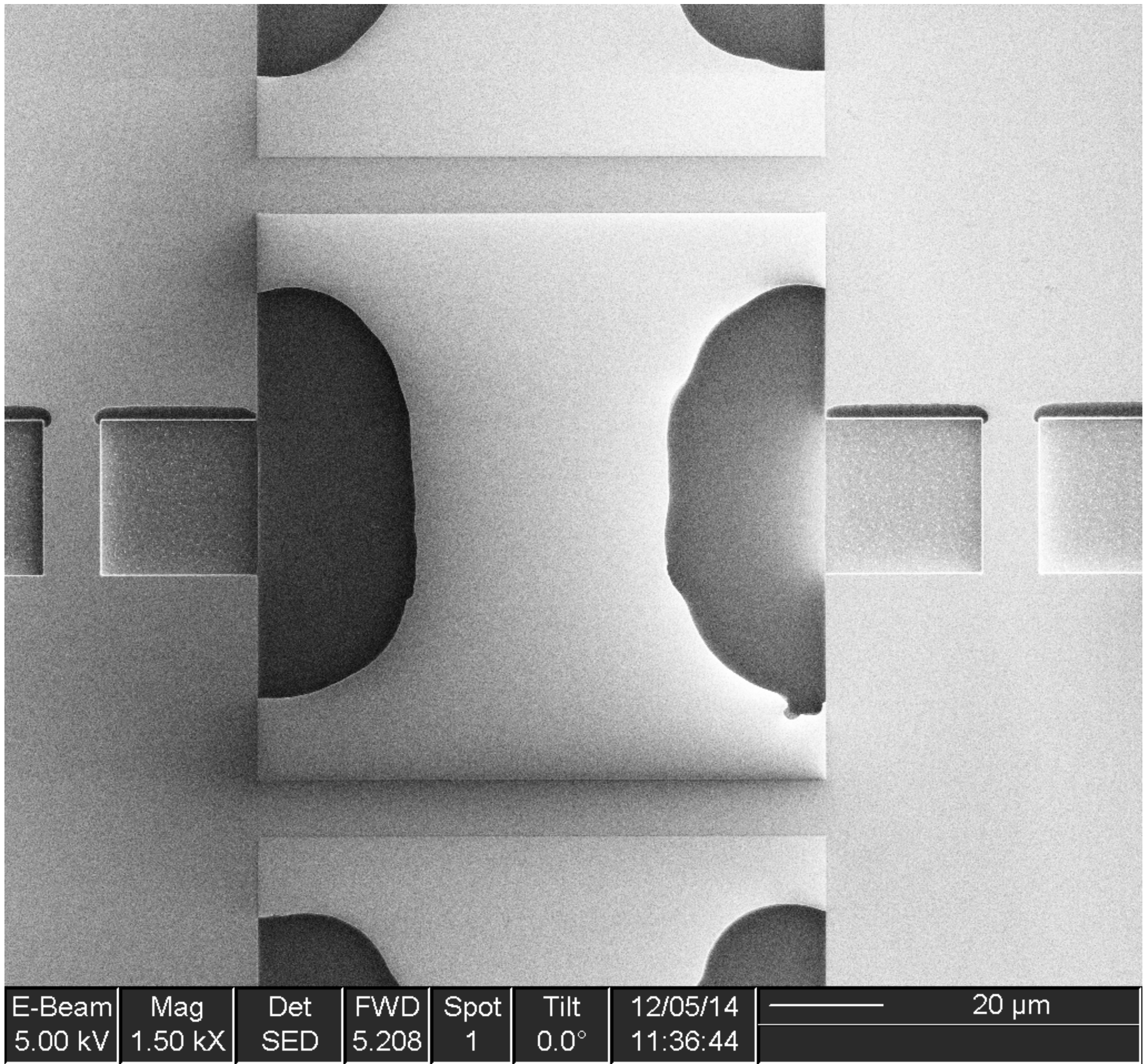


8 TMA cycles



9 TMA cycles

Fabrication results



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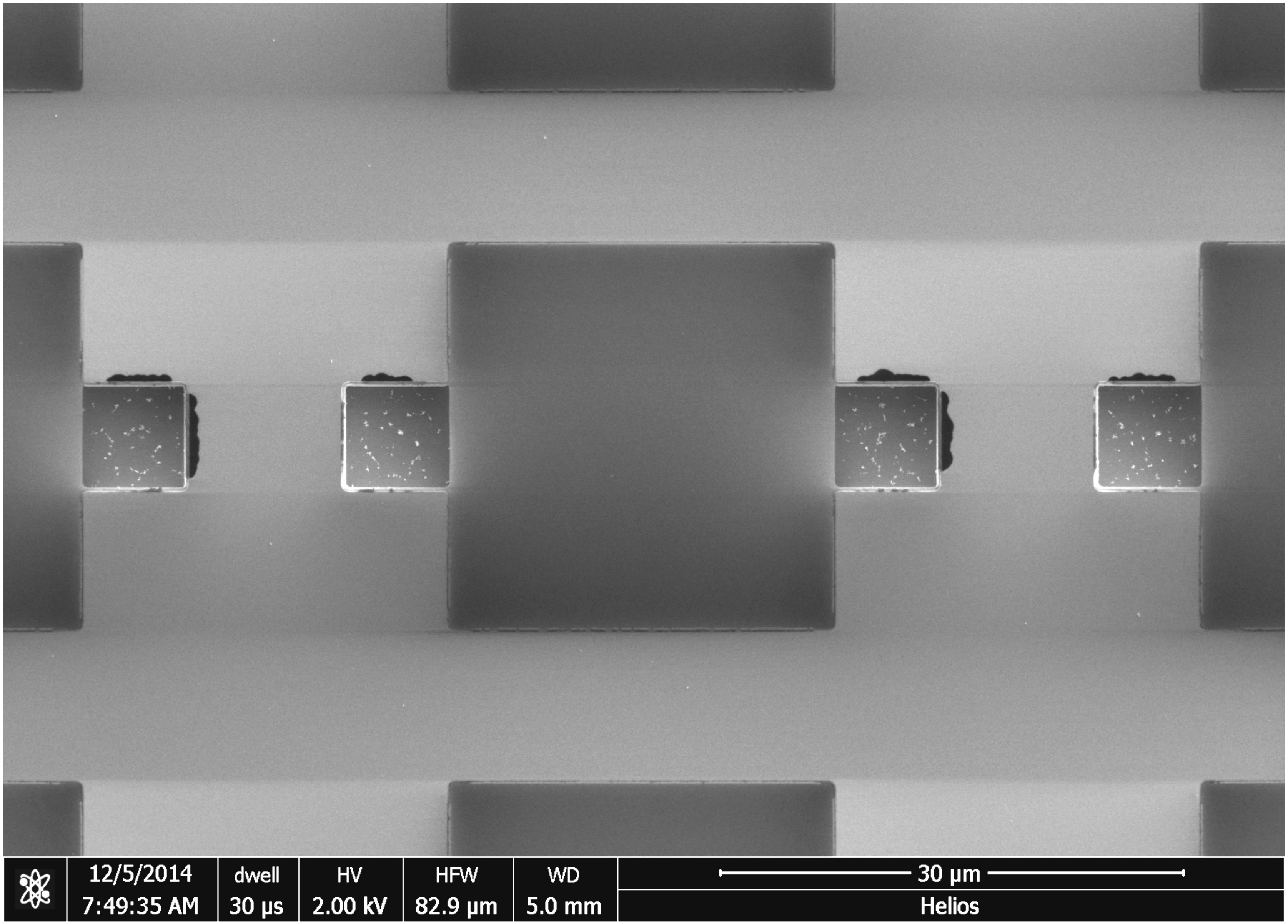

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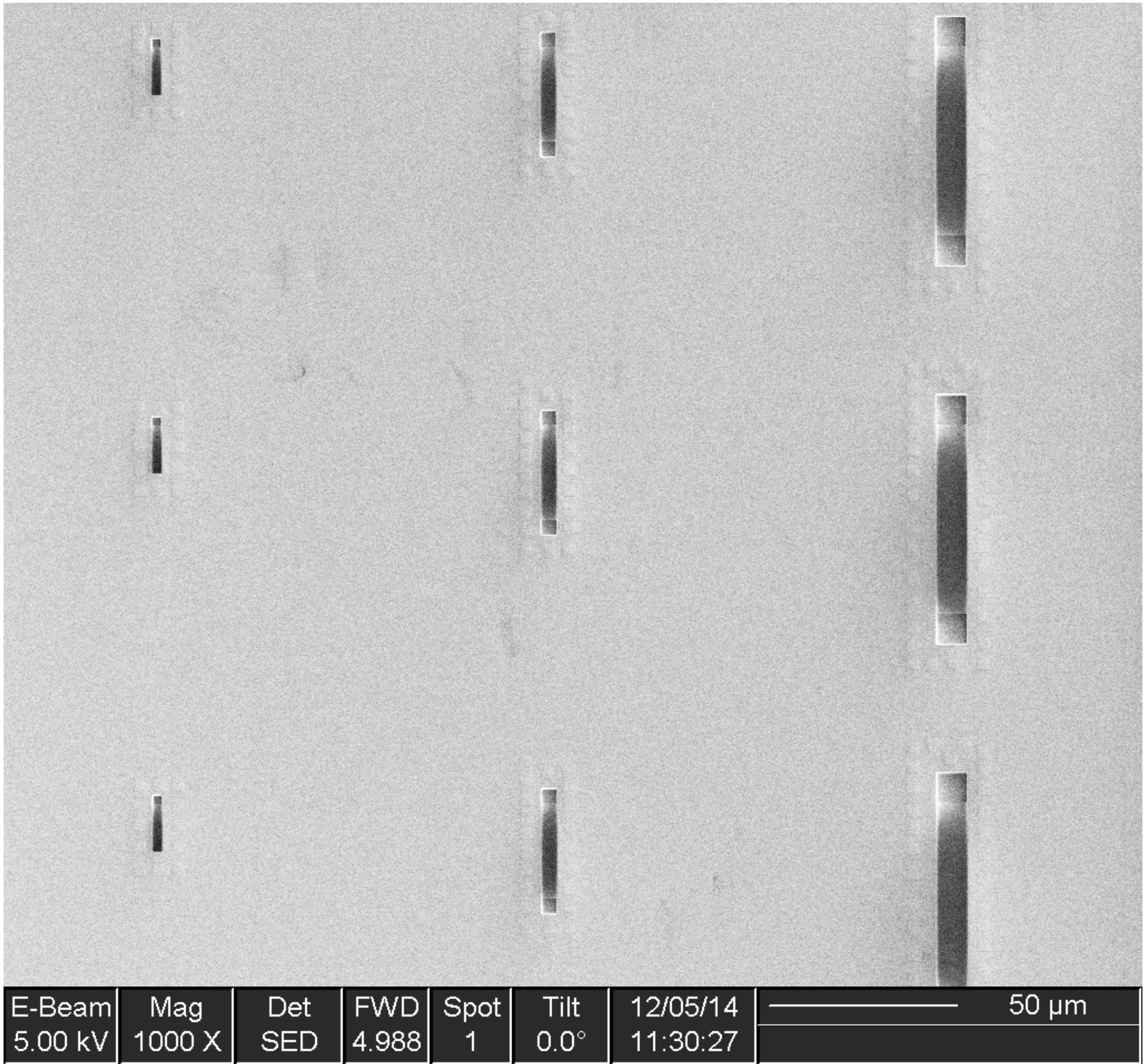

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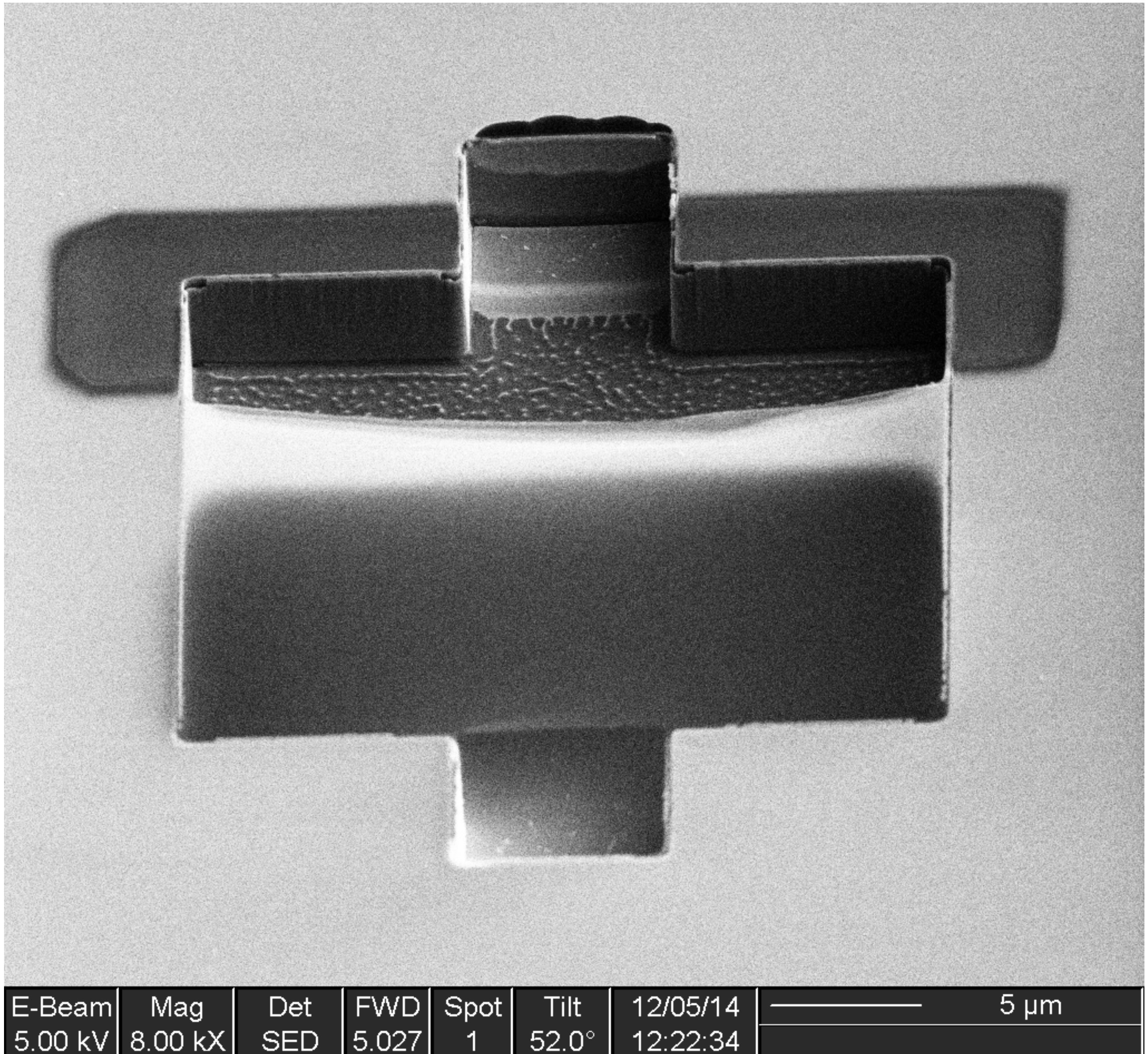
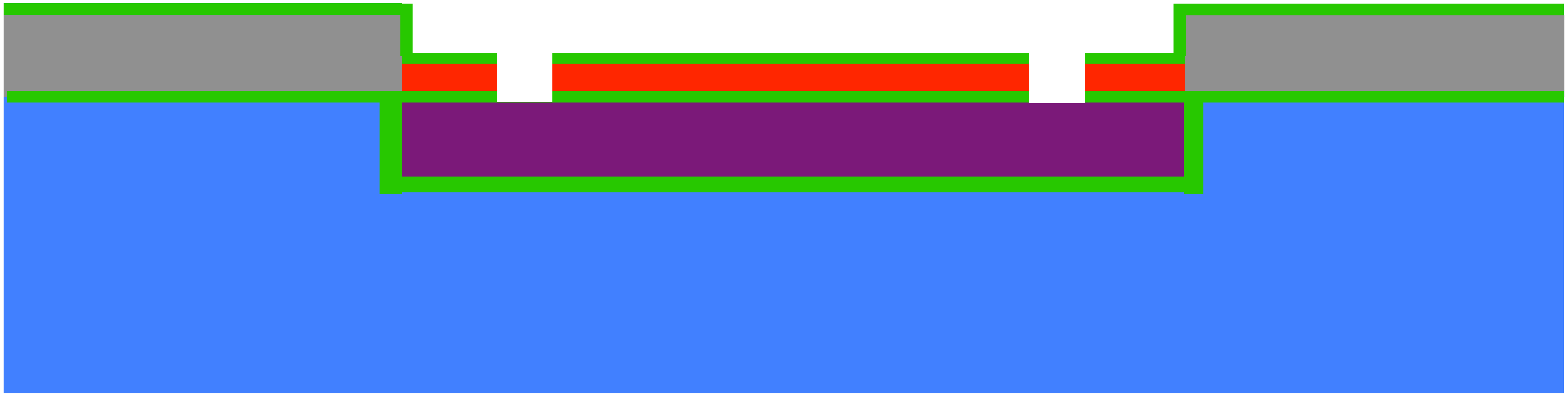
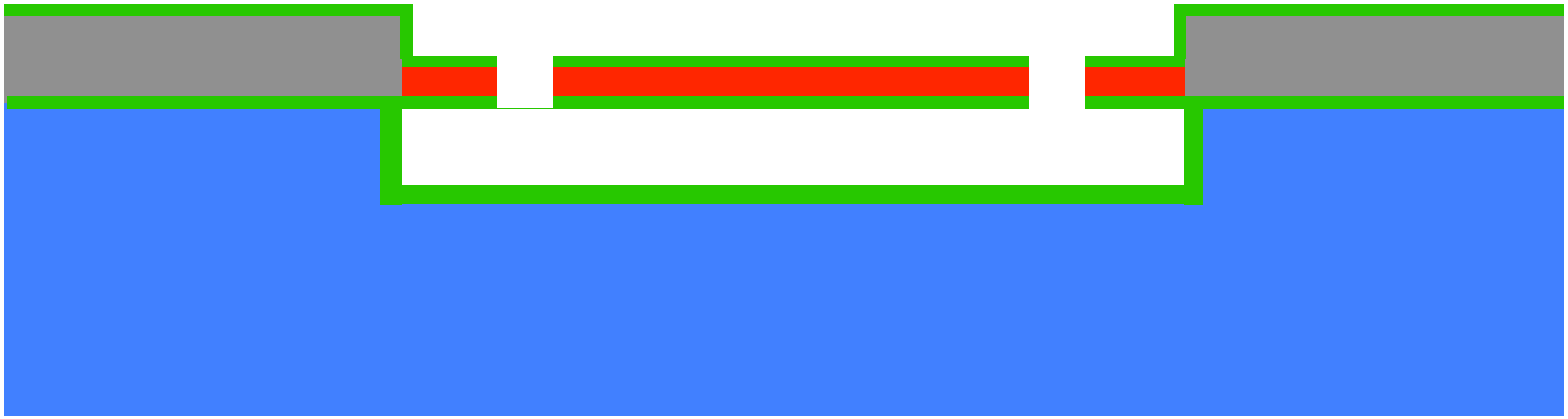


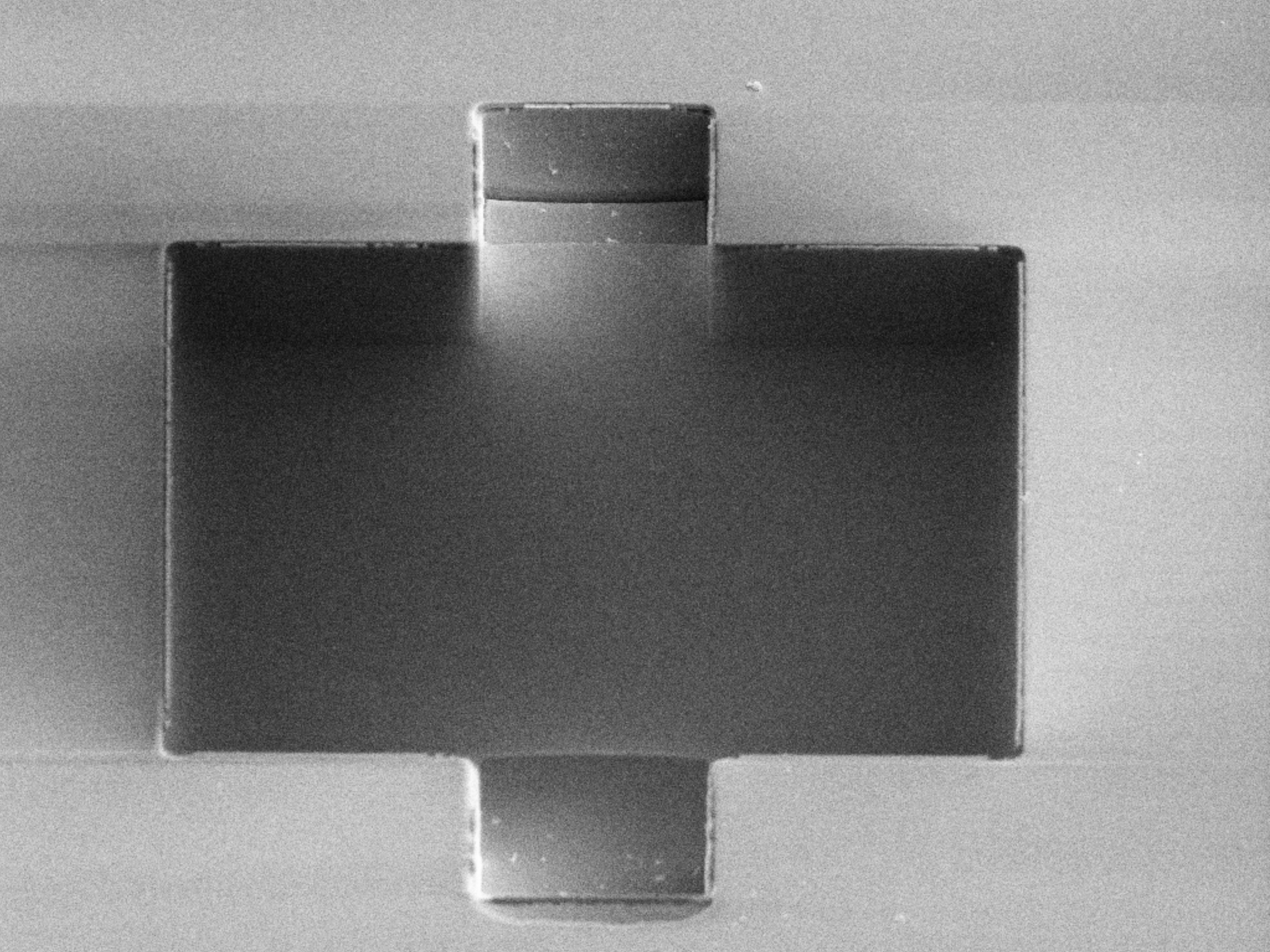
Self-alignment membrane passivation

7. Breakthrough etch



8. XeF_2 release





Thank you.