Released Lithium Niobate Structures on Silicon using the PT-DSE

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Introduction

Motivation

Lithium niobate (LN) has emerged as an ideal material for next-generation quantum devices owing to its strong optical nonlinearity and piezoelectricity. By simultaneously supporting long-lived gigahertz frequency mechanical oscillations and optical excitations, LN bridges the gap between the microwave and optical domains of quantum information processing [1,2].

Further, the combination of LN's strong piezoelectric coefficient and recent advances in fabricating thin film LN devices on silicon has allowed for novel studies of *quantum acoustics* [3,4]. Specifically, using electrodes patterned on nanomechanical LN resonators, one can couple to mechanical motion down to the single phonon level [3].

As an example, consider a piezoelectric nanomechanical resonator with an isolated resonance frequency of $\omega/2\pi$= 2.5 GHz cooled to the T = 5 mk baseplate temperature of a dilution refrigerator satisfies,

$$kT \ll \hbar\omega$$

where k is the Boltzmann constant and $\hbar$is the reduced Planck constant. Thus, the mechanical resonator is effectively cooled to its quantum ground state and it is best modeled with the following Hamiltonian,

$$H_r = \hbar\omega(a^\dagger a + \frac{1}{2})$$

where $a^\dagger$and a are the creation and annihilation operators for phonons in the nanomechanical resonator respectively. Now consider the Hamiltonian for a superconducting transmon qubit, which behaves as an artificial atom or two-level system,

$$H_q = \frac{\hbar}{2}\omega\sigma_z$$

The transmon superconducting circuit can be capacitively coupled to the mechanical resonance and described by an interaction term,

$$H_{int} = g(\sigma_+ + \sigma_-)(a + a^\dagger)$$

allowing for the exchange of quanta between the qubit and mechanical modes of the System. The sum of these three terms represents a quantum acoustic system that interfaces light and motion.

Quantum acoustic resonators have emerged as an attractive platform for quantum computing hardware owing to their long lifetimes, small size, and integration with superconducting circuits. Systems of mechanical resonators coupled to superconducting circuits, such as those shown in Fig. 1, are promising platforms for scalable quantum computing since arrays of long-lived nanomechanical resonances controlled by a single quantum processing element allows for the compact storage of quantum information with no additional instrumentation overhead. Hybrid acoustic-superconducting quantum circuit architectures are explicitly being pursued by AWS [6].

A crucial step for achieving long-lived excitations in quantum acoustic systems is decoupling the desired resonance from other mechanical loss channels. This is achieved by placing the desired resonance in a phononic bandgap and *releasing* the mechanical resonator from the substrate [4]. Developing a reliable technique for releasing LN structures from their silicon substrate is an important step towards reproducibly fabricating quantum acoustic devices.

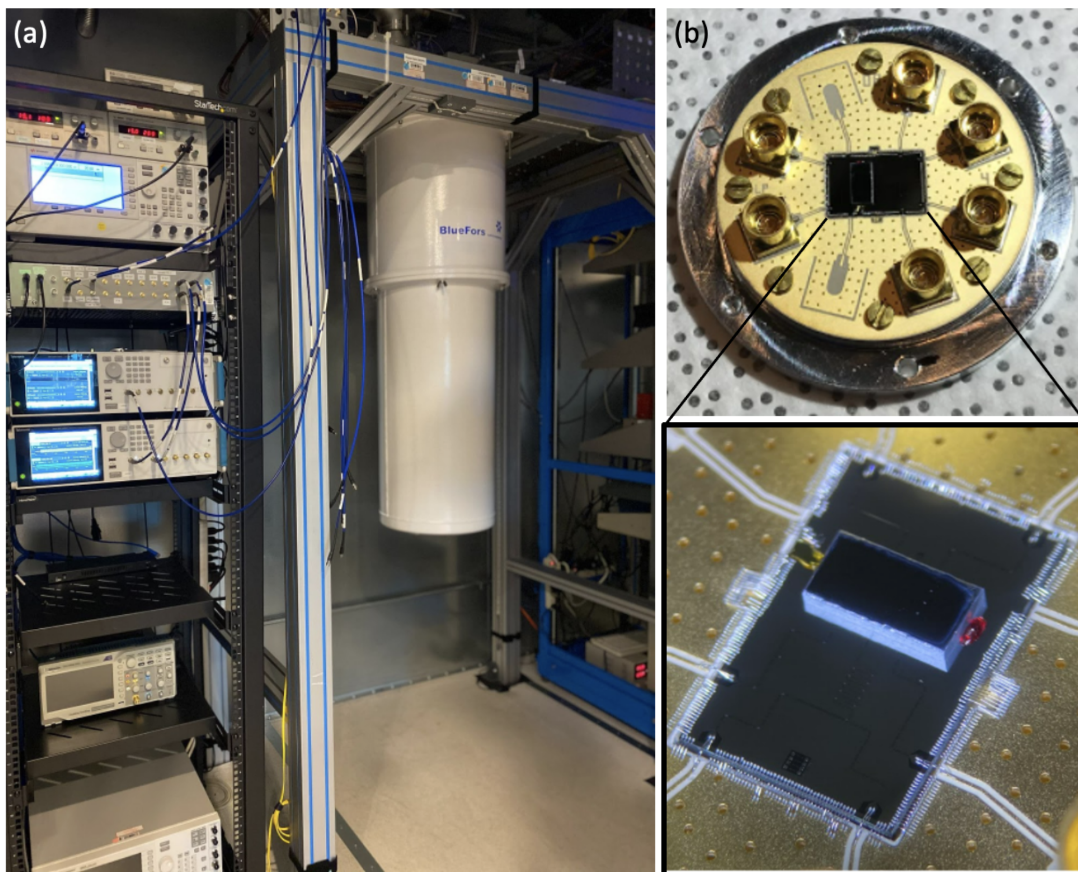


Fig. 1: (a) Dilution fridge in the Safavi-Naeini lab used to cool mechanical resonators into their quantum ground state. (b) Packaged quantum acoustic resonator coupled to a superconducting transmon qubit.

Partially releasing structures on silicon from their substrates extends beyond fabricating long lived LN nanomechanical resonators. Releasing thin film trampolines of silicon nitride has led to ultralow loss mechanical oscillators that reach a quantum coherent regime even at room temperature [7]. Suspended thin films of piezoelectric material increase the electromechanical coupling which enables small footprint piezoelectric transducers [8].

Project Goal

We propose to develop a robust process for undercutting Si from structures using SF_6 in the PT-DSE. Previous works have released LN nanomechanical resonators using XeF2 in the Xactix, but extreme sensitivity to chamber conditions and drastic differences in the silicon and silicon oxide etch rates led to unreliable etch rates and a low yield on final devices. Fig. 2a shows an example of irreproducible etch rates leading to collapsing structures, and Fig. 2b shows an example of sensitivity to chamber conditions leading to polymers growing on LN devices. However, previous work in ENGR 241 has demonstrated that the PT-DSE is a versatile Si etcher that is compatible with isotropic etching, which is crucial for undercuts.

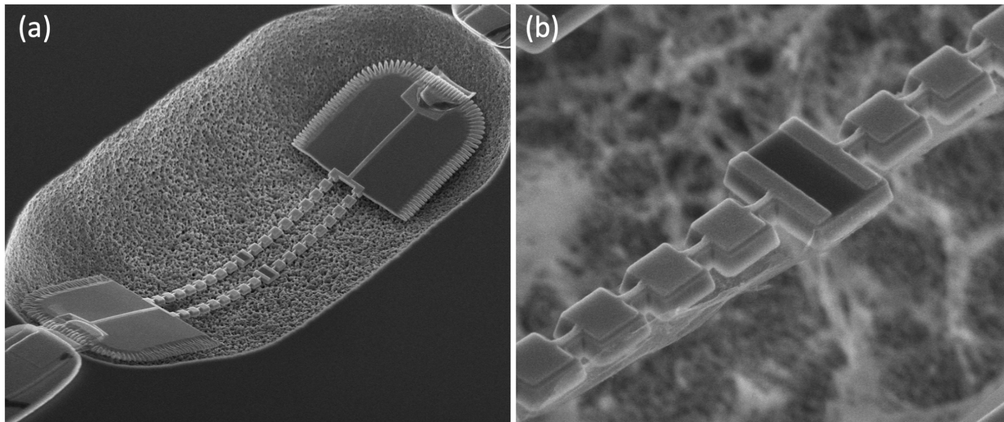


Fig. 2: (a) Released LN structures using XeF_2 in the Xactix, where irreproducible etch rates led to collapsing anchors. (b) Chamber memory from previous runs causing a polymer to grow on the LN structures.

Given that LN has never been placed in the PT-DSE, **we will also characterize how releasing LN structures affects standard etch rates in the PT-DSE, and will submit our findings for PROM committee approval to enable future projects.** Before attempting to release LN structures, we will first optimize our process using aluminum proxy structures. Given that fabricating aluminum structures is significantly easier than fabricating identical structures from LN, this will enable us to rapidly iterate on our process. This will also enable us to develop our process without contaminating the chamber. While our end goal is undercutting LN phononic crystals, **our work will also study the PT-DSE's ability to *shallow* etch under structures of various geometries and materials.**

A previous ENGR 241 project demonstrated the versatility of etching Si using SF_6 in the PT-DSE. Specifically, they used the PT-DSE to form micron-scale blades using a combination of isotropic and anisotropic etches. Their SOPs will provide a solid foundation for our project. However, our project represents a several key advances:

1. We hope to increase the versatility of the PT-DSE by investigating its compatibility with LN. Specifically, we will study the amount of lithium in the chamber after an etch by requesting VPD-ICPMS tests from Chem Trace.
2. We are explicitly interested in the released structures above the etched Si, and will

investigate different materials/geometries that can be undercut.

3. Given our end goal is releasing nanoscale LN structures, we are interested in adapting their deep (~100 um) etch process to a shallow (~3 um) etch process.

Benefits to SNF

Nonlinear optics in LN was pioneered by Stanford researchers [9,10], and Stanford continues to be a leader in the study of LN [3,11]. These efforts rely heavily on the community's shared expertise in LN fabrication. Understanding how SNF tools can be used to support LN fabrication is crucial for the success of our research and benefits the broader SNF community. Therefore, important aspects of our project are:

1. Characterizing the PT-DSE's compatibility with LN fabrication through etching followed by VPD-ICPMS tests from Chem Trace to determine the amount of lithium in the chamber.

2. Develop a process for undercutting a variety of geometric structures made from LN and other materials, such as aluminum.

3. Study limits on the geometries that can be released, as well as post-etch residual stresses.

4. Develop a process for *shallow* (~ 3 um) isotropic etching the PT-DSE as opposed to the traditional deep etch (~100 um).

Fabrication Process Development

Process Flow

In order to develop a new process for releasing lithium niobate devices in the PT-DSE in 10 weeks, we adopted a streamlined process flow that simplifies aspects of the fabrication process while maintaining the validity of the process when applied to actual nanomechanical piezoelectric devices of interest.

In essence, our process development involved 3 major steps: the fabrication of aluminum proxy structures, a design of experiments for releasing structures in the PT-DSE, and the fabrication and release of lithium niobate structures in the PT-DSE. A summary of this process is depicted in Fig. 3.

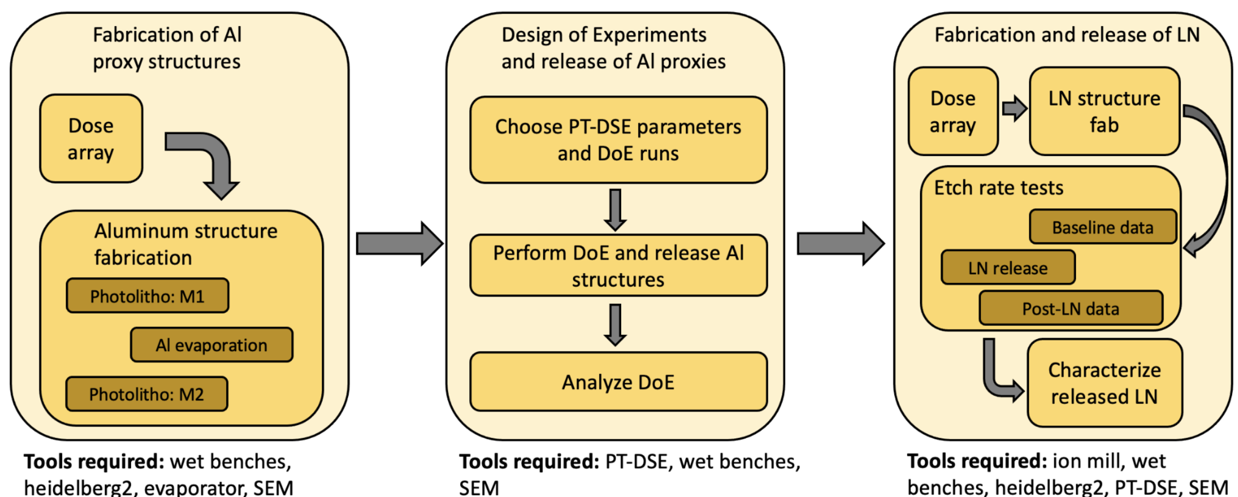


Fig. 3: Overview of PT-DSE release process development. We begin by fabricating Al proxy structures using a combination of photolithography and evaporation, then use these structures to develop a process for shallow and isotropic etch in the PT-DSE. Finally, we apply this process to releasing LN structures, and we characterize etch rates before and after the release to assess chamber contamination.

Fabrication of aluminum proxy structures was necessary to obtain a multitude of nearly identical chips which we could use to practice releasing and honing our release recipe in the PT-DSE without introducing contamination into the chamber

The design of experiments offered a statistics based approach to exploring the parameter space of etching in the PT-DSE. By utilizing a fractional factorial design of experiments, we investigated the main effects of four parameters: electrode temperature, bias voltage, forward ICP power, and $SF_6:O_2$ gas ratio, on etch rates and etch isotropicity, and used these results to pick an optimal etch recipe.

Finally, the culmination of the project was the fabrication and release of LN structures in the PT-DSE. Since LN is not on the list of approved materials for the PT-DSE, we were required to perform contamination and etch rate tests. This data was then used to draw conclusions about potential impacts of the presence of lithium on the tool's etch rates which have implications to user processes.

Structure design

In designing devices to release, we anticipate failure modes to include devices collapsing under their own weight, devices breaking due to residual stresses, and polymer growth around the device's edges. We identified the last failure mode based on previous experience releasing phononic crystals (PNCs) using XeF_2 in the Xactix, which resulted in polymers growing inside sharp edges, as shown in Fig. 2b.

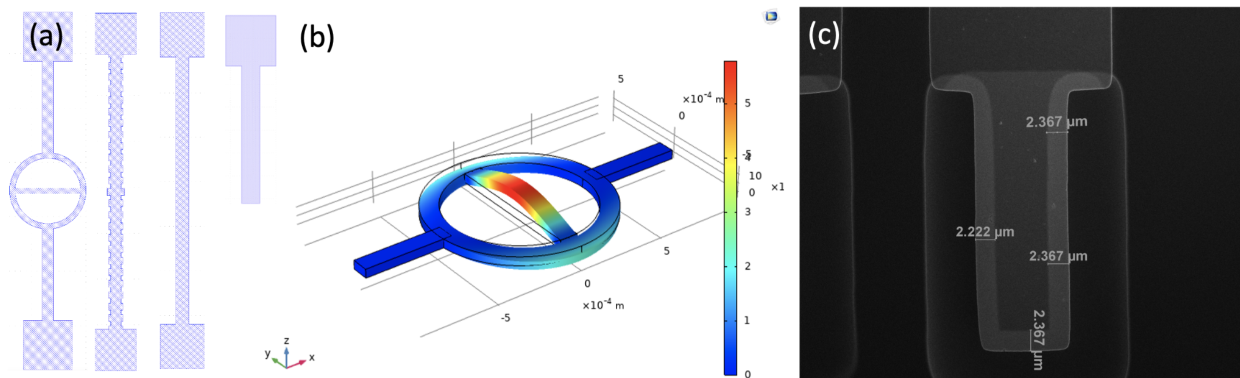


Fig. 4: (a) Structures to be released in the PT-DSE. (b) Finite element method simulations of the so-called theta structures under stress from the two anchors showing clear buckling in the middle beam. (c) Example overhead SEM of an unreleased aluminum beam showing easy characterization of horizontal etches.

To speed process development, we designed release structures to identify each of the preceding failure modes. The four release structures we designed are shown in Fig. 4a. To study how devices can collapse under their own weight, we designed *planks* that are only anchored at one end, and we varied the lengths of these planks from 5 um to 30 um. To study how residual stresses might affect the devices, we designed *thetas*. Buckling of the theta's middle beam should clearly show any residual stresses coming from the anchors, as shown in Fig. 4b. To study whether high aspect ratio geometries lead to polymer growth, we designed PNCs. Finally, we fabricate a series of *beams*, which are simply rectangles that are anchored on either end. SEMs of wide beams that are not released by the etch provide precise information about the horizontal etch rate of our etch, as shown in Fig. 4c.

Fabrication of Aluminum Proxy Structures

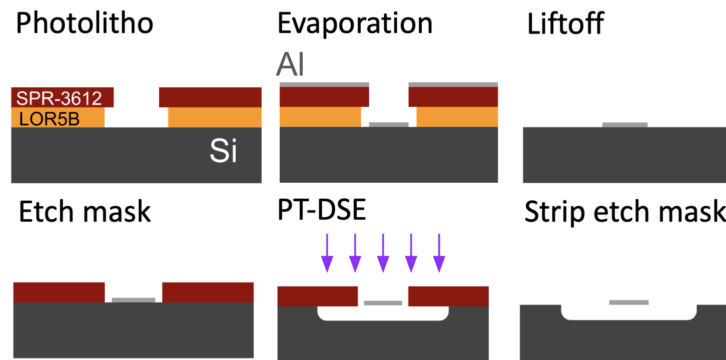


Fig. 5: Overview of LN release structures fabrication.

Fabrication of our aluminum proxy structures involves a relatively simple photolithography process, the steps for which are depicted in Fig. 5.

We begin by cleaning our 5x10 mm silicon substrates by sonication in acetone for 5 minutes followed by sonication in isopropanol for 5 minutes. A dehydration bake on a 180 C hotplate drives off moisture and improves adhesion of the spin stack. We then spin a ~550 nm layer of LOR5B (lift off resist) and partially harden at 180 C for 5 minutes. It is important to note that LOR5B is very viscous and does not spread easily and so one must cover the vast majority of a chip to obtain adequate coverage, for a 5x10mm sample this was equivalent to two large drops from a glass pipette. After the LOR5B, we spin a layer of SPR-3612, a positive resist, to a thickness of ~1um and bake for 1 minute at 90 C.

From here, we proceed to Heidelberg MLA 150 - 2 maskless aligner for direct write photolithography. We expose our patterns in optical autofocus mode due to small substrate sizes with an optimal dose value of 95mJ/cm^2 and defocus value of -6, which were determined via a dose defocus matrix using series mode.

With exposure completed we develop the resist in MF-26A for 20 seconds, followed by DI water rinses. In addition to removing the exposed SPR-3612 regions, the MF-26A also removes the underlying LOR5B layer, thus the timing of the development allows one to undercut the top layer of SPR-3612. This undercut is crucial for the deposition of aluminum and subsequent liftoff. For our process we aimed for ~1um of undercut, which can be verified under optical microscope as seen in Fig. 6.

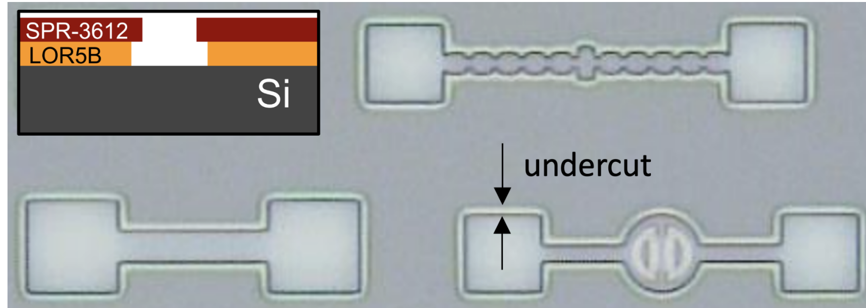


Fig. 6: Photoresist spin stack after development showing undercut of SPR-3612, as illustrated in the inset.

At this stage, we perform a descum in the march instruments PX-250 plasma asher in the SNSF flexible cleanroom (FCR) to remove the top ~25 nm of SPR in preparation for aluminum evaporation. Evaporation of the aluminum is performed in a Plassys Electron Beam Evaporator MEB550S housed in the Safavi-Naeini Lab. This state of the art tool uses a focused beam of electrons to bombard and evaporate metals in a high vacuum environment. The metals are deposited on samples and the deposition rates can be precisely tuned via source current and measured with a crystal monitor. For our process, we evaporated 250 nm of aluminum at a rate of 1 nm/s.

We now performed a liftoff procedure to remove the aluminum that was not deposited on the silicon. This involves submerging the samples in Remover PG, which dissolves the walls of LOR5B that are exposed due to the undercut. Gentle agitation then removes the thin film of aluminum. After the film is removed we rinse with IPA and are left with our aluminum proxy structures on our silicon substrate, as shown in Fig. 7.

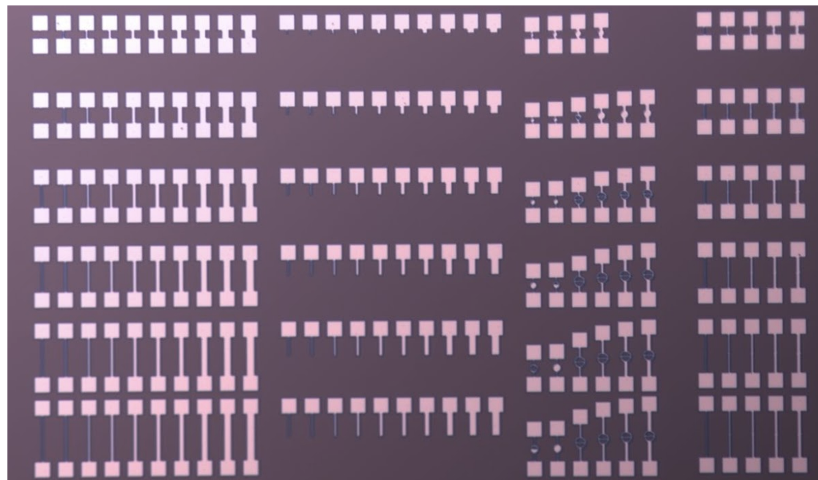


Fig. 7: Aluminum proxy structures on Si after liftoff.

The last step before the etch and release of the aluminum proxy structures in the PT-DSE is the patterning of the etch windows. These windows can be written in either a single or double layer spin stack and with the same procedure/parameters as the first mask. The purpose of these etch windows is to localize the etching to the structures we want to release. The extent of these windows is visible under optical microscope, seen in Fig. 8.

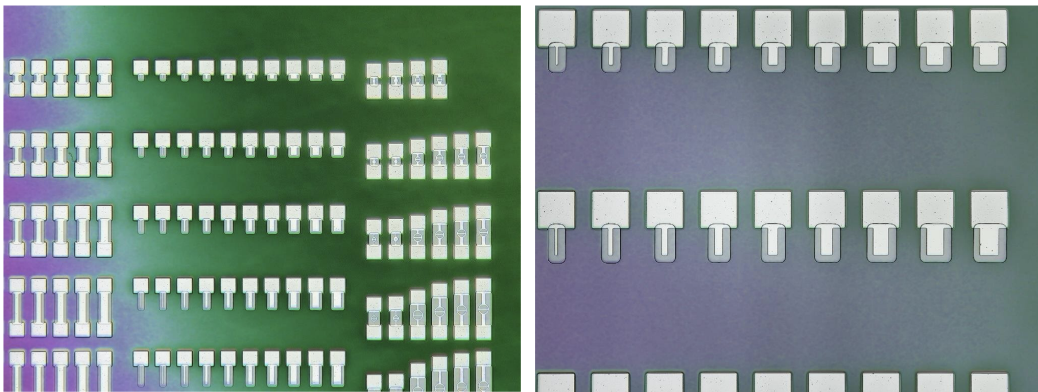


Fig. 8: Aluminum proxy structures on Si after the etch windows were patterned around the portions of the structures to be released.

Finally, we cleaved our samples in half to double our number of samples and mounted the 5x5mm chips to a silicon carrier wafer using a small amount of PMMA 9550k as a glue which can later be easily removed in acetone.

Design of Experiments

The Plasma Therm Versaline LL ICP Deep Silicon Etcher (PT-DSE) uses an inductively coupled plasma and SF_6 fluorine chemistry to etch silicon. For a given PT-DSE recipe, there are many parameters that can be modified.

The most important parameters to consider when studying etch rates in the PT-DSE are electrode temperature, ICP power, bias voltage, and SF_6:O_2 ratio. The electrode temperature could affect the kinetics of the chemical reaction. The ICP power affects how energetic the plasma and its free radicals are. The bias voltage affects the directionality of the plasma. The SF_6:O_2 ratio is known to affect the selectivity of the etch [12], although here we are only doing shallow etches. We are optimizing our process while holding the etch time fixed at 150 seconds, since the later adjustment of time can be done to undercut structures of arbitrary dimensions.

Another important parameter for the PT-DSE is the number of *Bosch* loops. The PT-DSE is unique in its capability to execute the *Bosch process*, which yields anisotropic Si etches by cycling between short isotropic etches and passivation of sidewalls with a C_4F_8 polymer and produces high aspect ratio features. Given that our goal is to develop a process for shallow, isotropic etches, we are not executing any Bosch loops. A previous E241 project developed a process for implementing the Bosch process in the PT-DSE to develop blades for microdissection of biological samples.

We ran a *half fractional factorial* DoE [13] on our four parameters, leading to eight DoE runs. In addition, we conducted two center runs where the PT-DSE parameters were set in between their high and low values for the DoE runs. These repeated runs were also used to characterize the variation between runs in the DoE [13]. The parameters of the PT-DSE and their

high/low/center values for our DoE runs are shown in Table 1, and the DoE runs are shown in Table 2.

Factors:	Low	High	Center
Electrode Temp	5	25	15
Bias Voltage	10	100	20
ICP Power	1200	2000	1600
SF6:O2	150 : 0	150 : 10	150 : 5

Table. 1: DoE Table showings studied PT-DSE parameters and their low, high, and center values.

Run	Temperature	Bias Voltage	SF6 : O2	ICP Power
1	-1	-1	-1	-1
2	+1	-1	-1	+1
3	-1	+1	-1	+1
4	+1	+1	-1	-1
5	-1	-1	+1	+1
6	+1	-1	+1	-1
7	-1	+1	+1	-1
8	+1	+1	+1	+1
9	0	0	0	0
10	0	0	0	0

Table 2: Design of Experiments table.

DOE Results

We found that every run of our DoE etched between 2-3 um horizontally and thus all structures that were under 4 um wide were released, increasing our confidence that the process we have developed is robust.

We characterized the vertical etch rates from our DoE using the Keyence laser microscope, as shown in Fig. 9a. The main effects of the studied parameters on the vertical etch rates are summarized in Fig. 9c. In the future, we hope to pattern trenches on our chip that will allow us to characterize the vertical etch rate using profilometry. Error bars correspond to the variance of the measured etch rates from the two repeated center runs.

We characterized the horizontal etch rates from our DoE using overhead SEMs, as shown in Fig. 9b. The *main effects* of the studied parameters on the horizontal etch rates are summarized in Table 9c. Error bars correspond to the variance of the measured etch rates from the two repeated center runs.

From our measured horizontal and vertical etch rates, we also studied the main effects of the PT-DSE parameters on the so-called *isotropicity* of the etch, which is defined as the ratio of horizontal to vertical etch rates. The main effects are summarized in Fig. 9d. We found that increases in electrode temp, bias voltage, O2 flow, and ICP forward power all contributed to increased horizontal and vertical etch rates. However, when studying etch isotropicity we find that increases to electrode temperature and O2 make the etch more isotropic, while increasing bias voltage makes an etch less isotropic (higher aspect ratio). Increases to the ICP forward power had a statistically insignificant effect on the etch isotropicity.

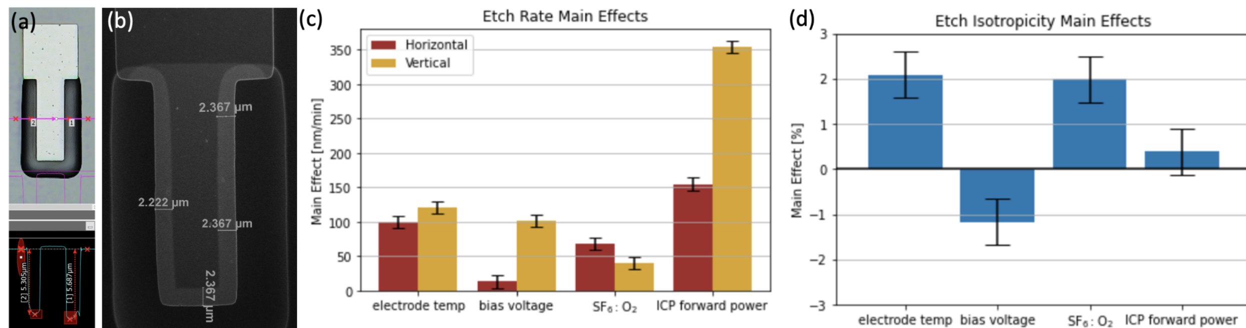


Fig. 9: (a) Example Keyence image used to characterize vertical etch rates. (b) Example SEM image used to characterize horizontal etch rates. (c) DoE main effects for vertical and horizontal etch rates. (d) Isotropicity main effects.

Given that all structures narrower than 4 um were released, we chose the PT-DSE parameters largely based on convenience. We chose 15 C for the electrode temperature because most recipes in the PT-DSE etch at this temperature and therefore we do not need to wait for the electrode temperature to stabilize when starting our process. We chose 1600 W for the forward ICP power because we observed high reflected ICP powers when the forward ICP power was set too low, causing the recipe to fail. We chose 10 V bias voltage because higher bias voltages will increase the risk of sputtering more Li ions into the chamber, which may cause chamber memory effects that affect other users' processes. We chose 150:0 for the SF_6:O_2 ratio because O_2 is known to increase the Si etch rate and the photoresist etch rate. However, we are only interested in shallow etches.

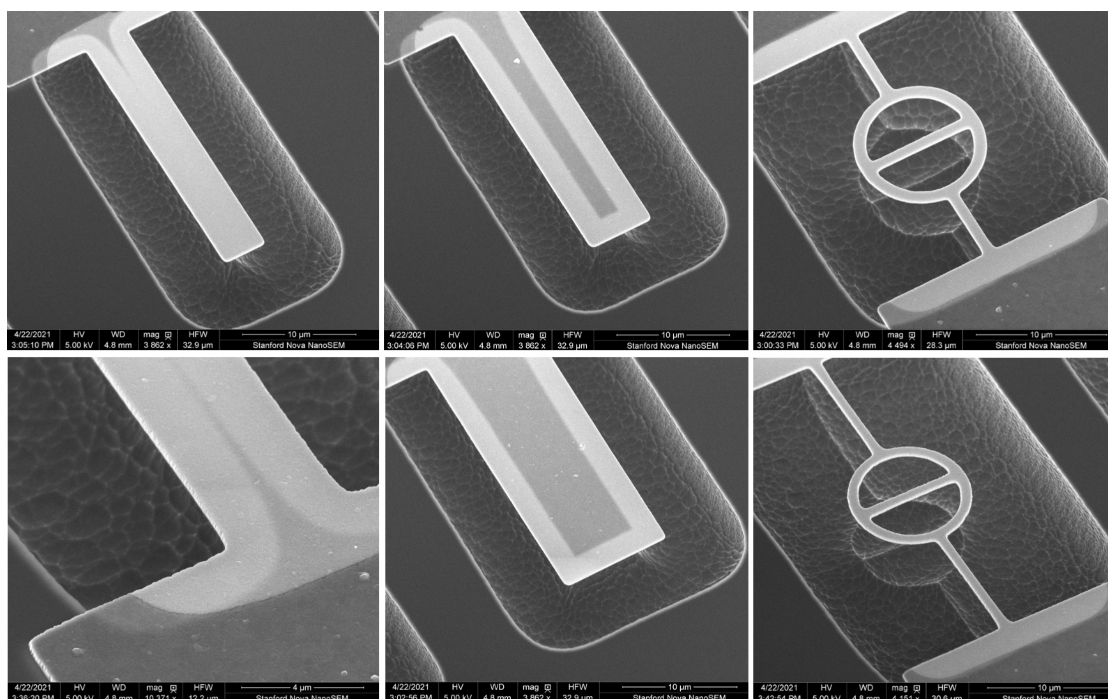


Fig. 10: SEMs of released and partially release aluminum proxy structures.

Fig. 10 shows a variety of released and partially released aluminum structures. The contrast between bright and dark regions of aluminum mark the boundary between undercut aluminum and aluminum still in contact with the silicon substrate. Below the theta structures one sees a raised silicon feature or 'shadow' due to the aluminum structure masking the anisotropic etch.

Common failure modes we observed in our etched samples include collapsed planks and photoresist residues on the structures, as shown in Fig. 11. We believe that the photoresist residues seen are SPR-3612 that became crosslinked.

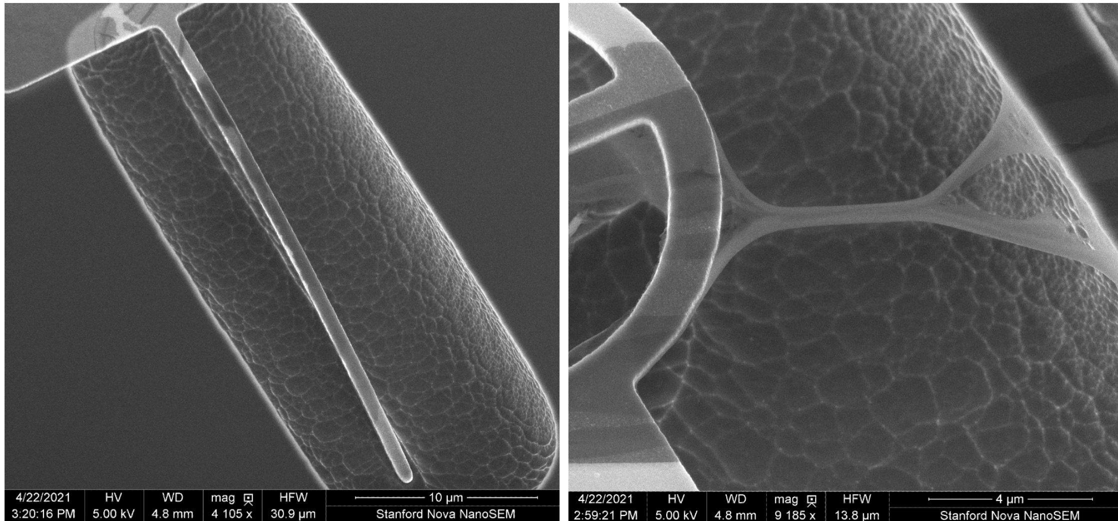


Fig. 11: SEMs of released structures showing collapsing (left) and photoresist residues on structures (right).

Fabrication of Lithium Niobate Structures

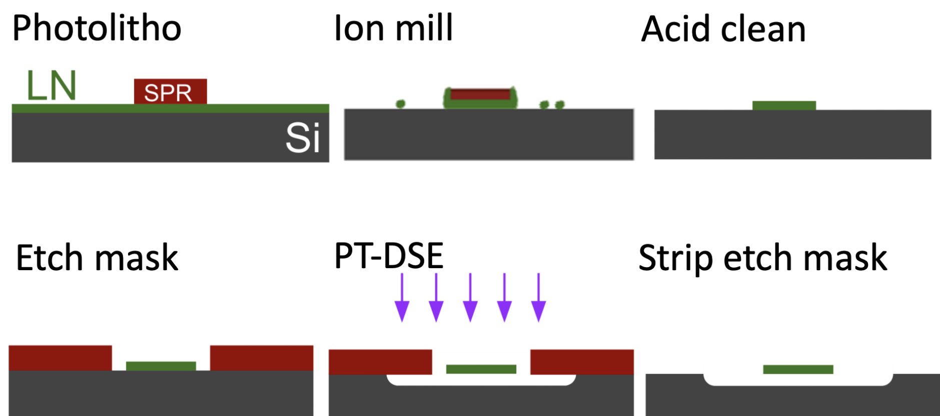


Fig. 12: Overview of LN release structures fabrication.

Fabrication of lithium niobate structures, in contrast to aluminum, is a subtractive rather than additive process. This is because the unique properties of lithium niobate are derived from its single crystal nature and so it cannot be sputtered or deposited like metals. The lithium niobate

samples we began with for this fabrication are 5x10mm chips with 500 nm of X-cut lithium niobate on silicon. Fig. 12 shows a simplified process of the $LiNbO_3$ fabrication process, the main steps being lithographic patterning, ion mill physical etching, acid cleaning, and release.

The first step in our fabrication is to thin the 500 nm layer of LN to a target thickness of ~250nm, equivalent to the thickness of the phononic nanomechanical crystal resonators [3]. This is achieved by first measuring the thickness of our LN in the Woollam ellipsometer. For the two chips we are working with, we measured,

Pre-Thinning	Chip 1	Chip 2
Thickness	4976 Å	5100 Å

These chips were then mounted on a carrier wafer and placed in the Intlvac Ion Beam Mill Etcher in SNSF. After a total of 23 minutes of etching in the ion mill, the chips were removed and the LN thickness was measured again with the Woollam.

Post-Thinning	Chip 1	Chip 2
Thickness	2400 Å	2515Å

This amounts to an etch rate of LN in the ion mill of 11.13 nm/min.

Next, we spun SPR-3612 to a thickness of ~1um on the thinned layer of LN for both chips. The resist was then baked for 1 minute at 90 C to harden. After this, the samples were taken to Heidelberg2 and our patterns were exposed with a dose of 100mJ/cm^2 and a defocus of 0, values that were determined from a dose array. Note that there is no LOR5B for this spin stack because there is no liftoff process in the LN fabrication. These exposed resist patterns were then developed in MF-26A.

With the substrates now patterned with photoresist, we return to the ion mill and perform a 26 minute etch, which was calculated so as to overetch Chip 1 by 60 nm and Chip 2 by 50 nm. This safely avoids the potential for thin films of LN remaining on the chips. Fig. 13a shows the LN release structures after ion milling. Removal of the photoresist after ion milling is a challenge as it becomes heavily crosslinked, as shown in Fig. 13b. Further, the LN that is sputtered and redeposited during the ion milling process must be removed, as shown in Fig. 13c.

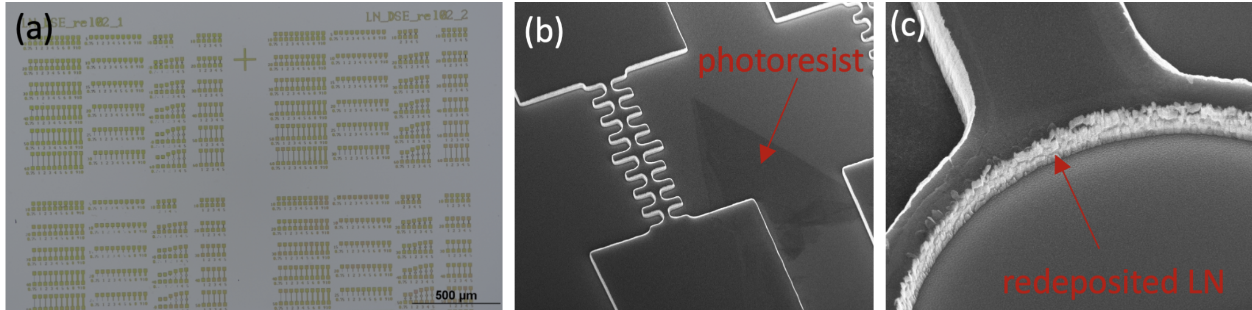


Fig. 13: (a) LN release structures on Si after ion milling. (b) SEM of LN structures showing photoresist films, and (c) redeposited LN after ion milling.

In order to remove the crosslinked photoresist, and reduce the sidewall roughness due to re-deposited lithium niobate, we performed a series of acid cleans. Each acid clean involves two steps, first is a 5 minute piranha clean comprising a solution of 3 parts concentrated sulfuric acid, 1 part hydrogen peroxide with a stir bar for agitation. After this a solution of 2% hydrofluoric acid is prepared at 42 C and our samples are gently agitated in the solution for two cycles of 3 minutes, with DI water rinses between cycles. Then the samples are thoroughly rinsed with water to ensure no acid remains.

We then view the samples under SEM to check the effect of the acid cleaning process on the crosslinked photoresist and amorphous LN.

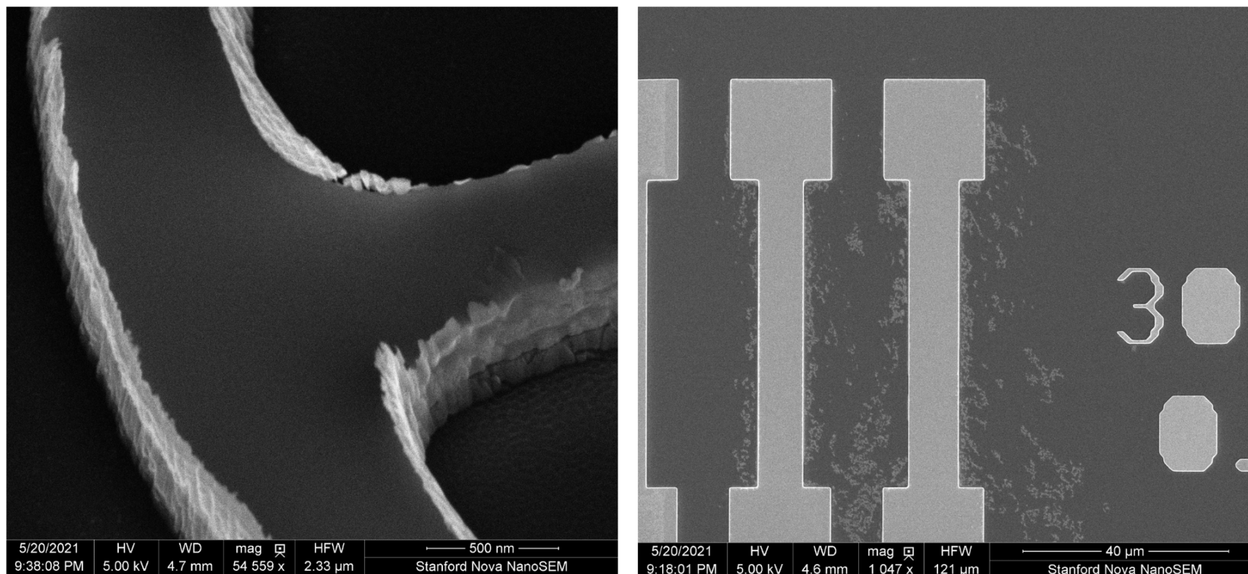


Fig. 14: Remaining redeposited LN and photoresist films after one round of acid cleaning. Note that these structures were released in the PT-DSE without further cleaning.

Fig. 14 shows inspection of the cleaned LN release structures under the SEM. We see that amorphous LN sidewalls were reduced but not completely eliminated, and that the crosslinked photoresist was partially removed after 5 minutes in piranha. We proceeded with one chip to the

PT-DSE after a single acid clean and repeated the acid clean on our second chip. This second chip was subjected to another round of acid cleaning, again 5 minutes in a 3:1 piranha solution followed by a total of 9 minutes in hot HF (3min + 3min + 3min). After a thorough DI water rinse we inspected the results of the second round of acid cleaning under the SEM.

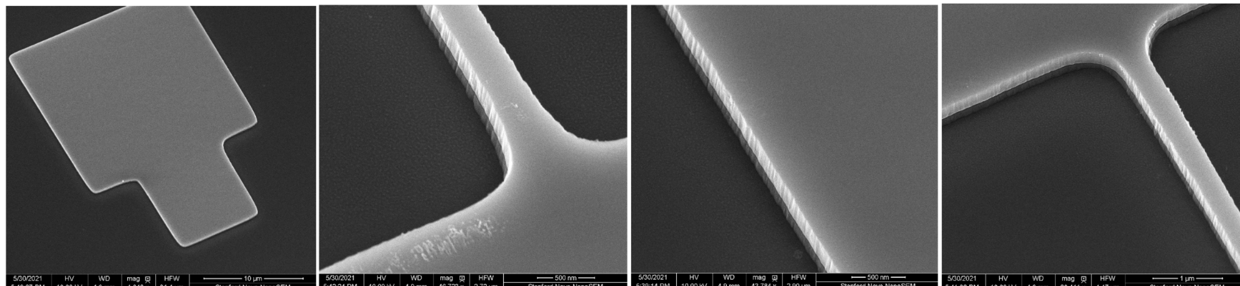


Fig. 15: SEMs of LN release structures after a second round of acid cleaning showing significant removal of photoresist films and redeposited LN.

We observe a dramatic improvement for most structures after a second round of acid cleaning. As seen in Fig. 15, we found no crosslinked photoresist residues on the chip and the amorphous LN sidewalls were markedly smoother. Some amorphous LN residues were still observed on some structures such as that seen in the second panel of Fig. 15, and it is believed that additional time/cycles in hot HF would eliminate it completely. Smoother sidewalls and increased feature resolution can be achieved using electron-beam lithography techniques.

It is important to note that the exact details and timing of an acid cleaning procedure such as the one employed above can be very sensitive to structure geometry and substrate size. Delamination of the LN from the silicon handle has been observed in larger substrates, e.g. 30x40mm, though no delamination was observed in the 5x10mm samples used in this project.

The last step in preparation for release was to pattern and expose SPR-3612 to define the etch windows for our release, as described in the section on aluminum proxy structure fabrication.

Etch Rate Tests

The PT-DSE is a flexible tool, meaning that the chamber becoming contaminated with lithium is not a primary concern. However, it is problematic if the degree of contamination is so large such that etch rates of standard recipes are altered. In accordance with our PROM request, we measured the etch rate using a standard recipe (DSE FAT EBTr for 40 loops) before our release, after our release, and after a standard plasma clean that all users run before their process (DSE Clean for 1800 seconds).

We measured both the photoresist etch rate and silicon etch rate. We used standard SUMO wafer provided by SNF staff, which have patterns written in SPR-3612 on Si. The photoresist etch rate was characterized by reflectometry using the Nanospec, and the Si etch rate was measured using profilometry using the Alphastep. For each measurement session,

measurements were taken in the top, middle, bottom, left and right of each SUMO wafer. In between the reflectometry measurement and the profilometry measurement, the photoresist is stripped using an O2 plasma etch in the Matrix plasma asher. The process for measurement and characterization of etch rates is depicted in Fig. 16.

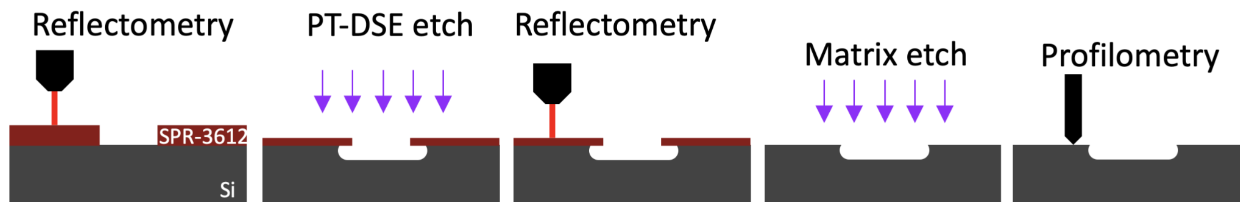


Fig. 16: Etch rate characterization process begins with reflectometry (using the Nanospec) to characterize the photoresist thickness, followed by a standard etching recipe in the PT-DSE (DSE FAT EBTr for 40 loops). The photoresist etch rate is characterized using reflectometry again and is then stripped using another plasma etch in the Matrix. Finally, the Si etch rate is characterized using profilometry (Alphastep).

During profilometry, special attention was paid to measuring the step height of identical structures across the wafer, as variation in etch rates dependent on the structure geometry was observed during our aluminum proxy structure DoE.

VPD-ICPMS Tests

To determine whether any changes in photoresist/Si etch rates is due to releasing LN structures, we also studied the contamination of the PT-DSE. Specifically, we requested vapor phase decomposition inductively coupled plasma mass spectroscopy (VPD ICPMS) tests on wafers that were run through the PT-DSE before we released LN structures, after we released LN structures, and after running a standard plasma clean (DSE Clean for 1800 seconds) that all users should run before starting their process. VPD ICPMS tests provide the surface concentration of different elements (such as lithium) present on a wafer. Therefore, these tests allow us to determine whether releasing LN structures sputters lithium into the chamber.

Importantly, the wafers used for VPD ICPMS tests must be very clean. Therefore, before these wafers were placed in the PT-DSE, we cleaned them with a piranha, followed by *Standard Clean 1* (SC1) and *Standard Clean 2* (SC2). SC1 and SC2, sometimes referred to as RCA cleans, are standard cleaning procedures for preparing wafers in semiconductor manufacturing. The piranha and SC1 remove any organics (such as photoresist) from the wafers, and SC2 removes any metal. These cleans were performed on new wafers at SNF wet benches in the “clean” category. Once cleaned, wafers were only handled with “clean non-metal” tweezers until after processing in the PT-DSE. Further, wafers were stored in teflon cassettes, which do not outgas and therefore do not contaminate housed wafers, between cleans and processing in the PT-DSE.

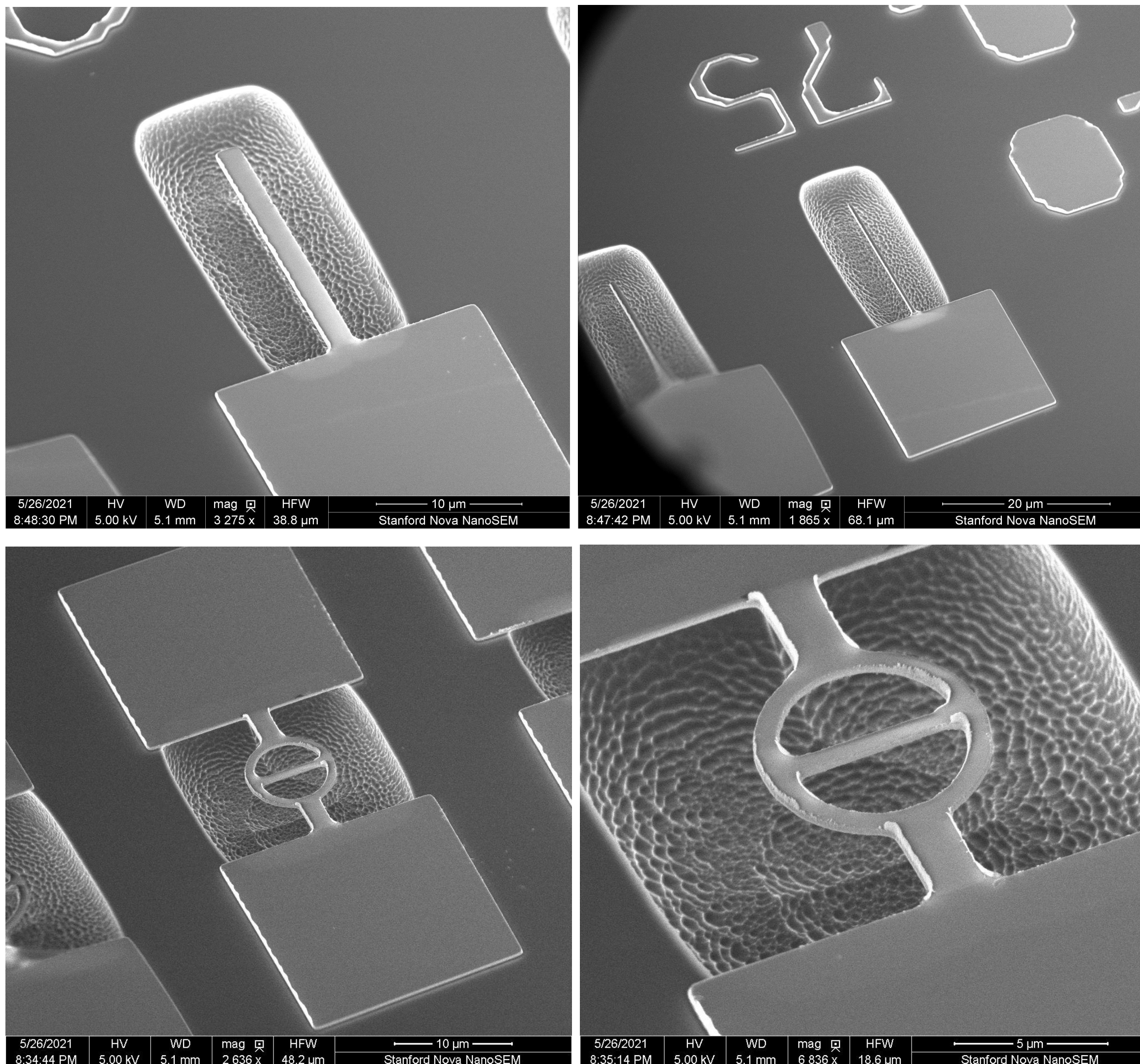
Although we collected the wafers for the VPC ICPMS tests and mailed them to ChemTrace, where they will be analyzed, we have not received the results yet.

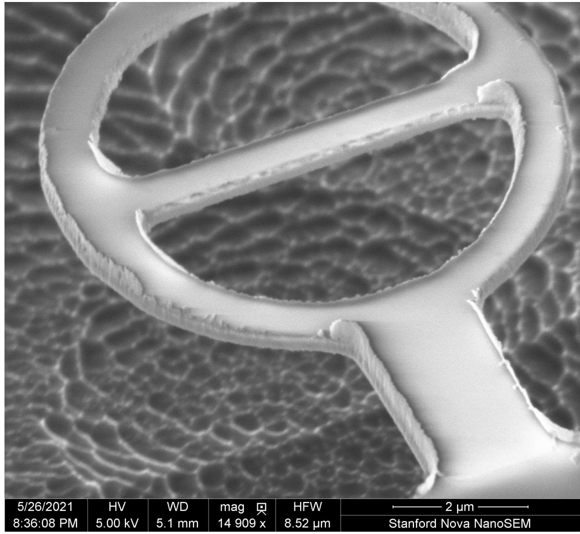
Results and Discussion

Characterization of Released Structures

Application of the process developed with aluminum proxy structures to LN fabrication (Chip 2) demonstrated the capability of successfully releasing the predicted structures (< 4 um wide). SEM images of the released structures are shown in Fig. 17.

Amorphous redeposited LN sidewalls were expected as this sample only underwent the first round of piranha and HF acid cleaning and the sidewalls.

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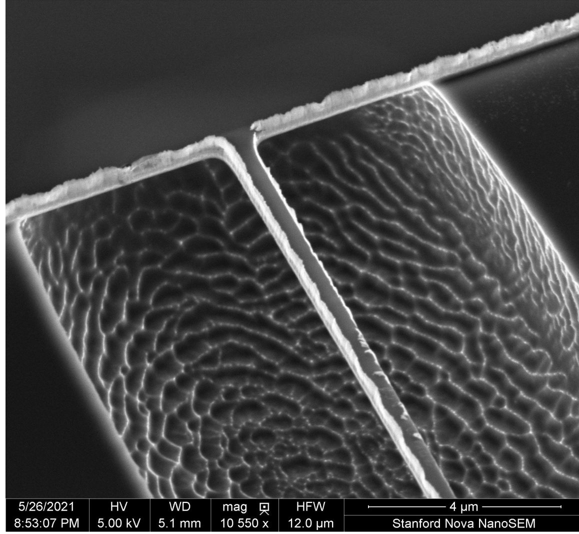
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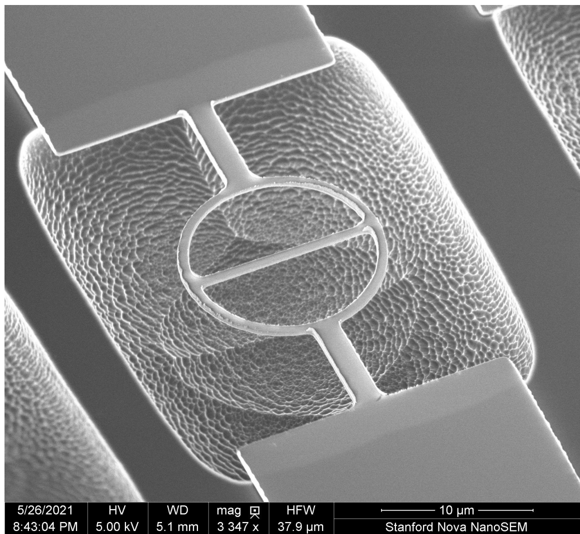
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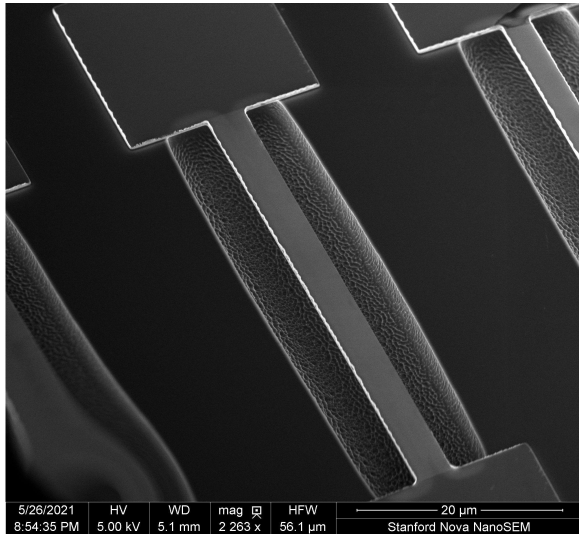
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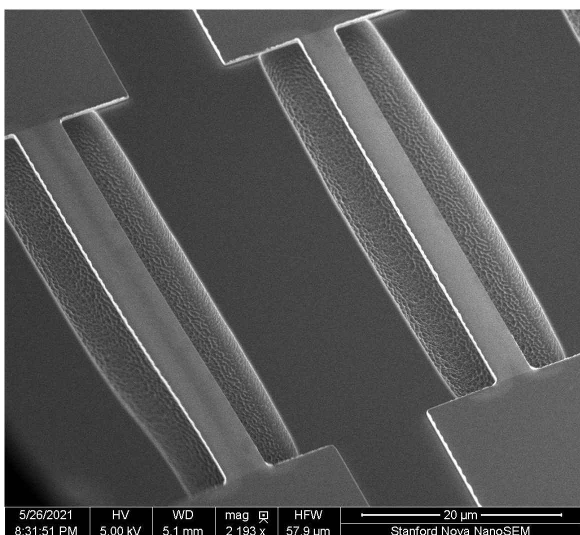
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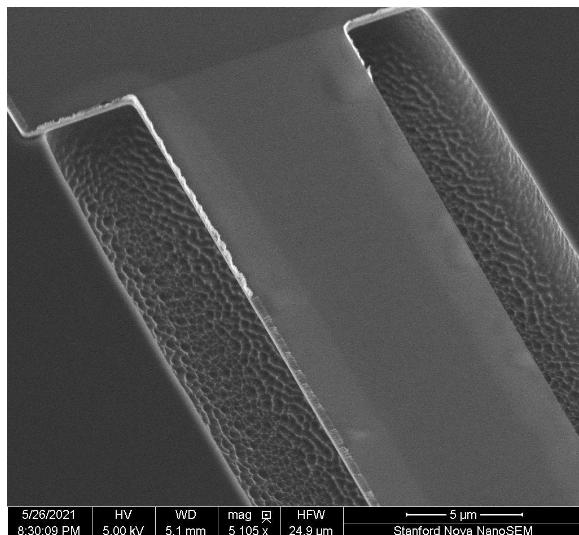
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HFW
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5 μm
Stanford Nova NanoSEM

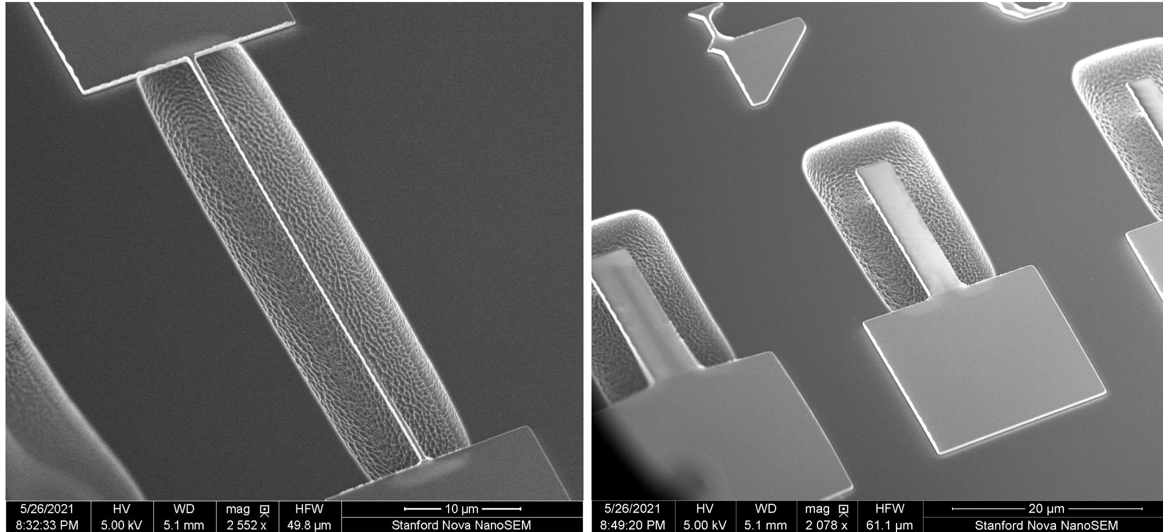

Fig. 17: SEMs of released LN structures.

In addition, we observed films approximately 50nm thick comprising crosslinked SPR-3612 photoresist from our etch window mask. These films were found draped across several structures on our chip such as those in Fig. 18.

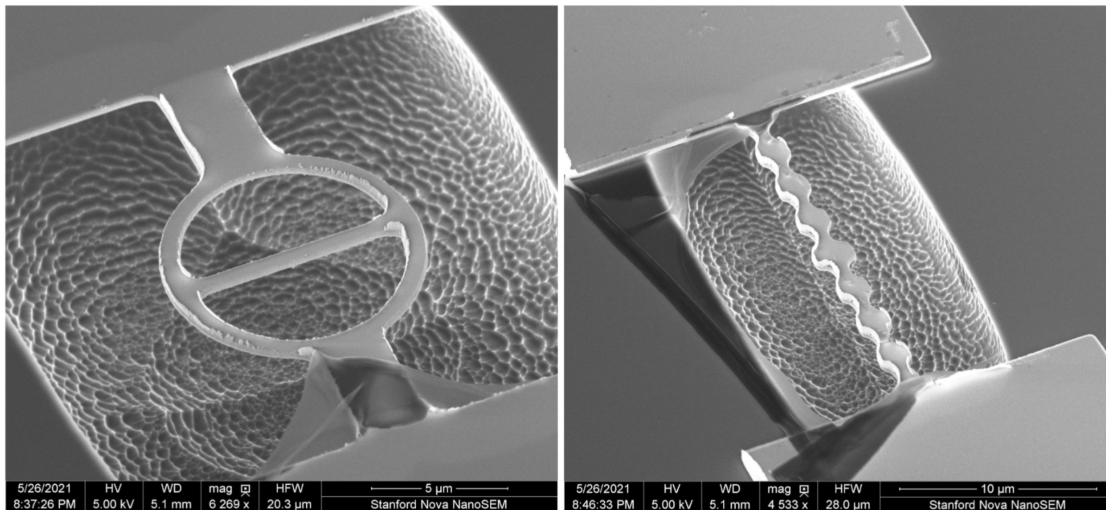

Fig. 18: SEM of released LN structure showing redeposited photoresist films.

We believe that the primary cause of these persistent photoresist films is our post-release cleaning process, which uses only a solvent clean consisting of acetone and Remover PG, both of which are notoriously poor for removing crosslinked photoresist. An additional factor we believe is contributing to this issue is the amorphous LN sidewalls, which effectively snag the lifted-off crosslinked films of SPR. Both of these effects should be mitigated by minor changes to our process.

Finally, we will comment on a notable advantage of this new process with the PT-DSE in comparison to the Xactix. The Xactix was found to be sensitive to loading effects --the amount

of silicon exposed to the XeF_2 etch chemistry, which depends on the substrate size and pattern--which posed a challenge for obtaining reproducible etch results. The PT-DSE however requires a Si carrier wafer for smaller substrates, this large exposed area of silicon effectively buffers against loading effects.

Etch Rates

The characterization of photoresist and silicon etch rates were performed with the Nanospec and Alphastep respectively, and correspond to running the standard recipe DSE FAT EBTr for 40 loops. Measurements were taken at 5 locations per wafer, at three distinct stages. The first stage, standard etch 1, measured baseline etch rates before the PT-DSE was exposed to LN, and was performed twice to allow us to estimate the normal variation in the tool etch rate. The second stage, standard etch 2, measured etch rates after the PT-DSE was exposed to LN. The third stage, standard etch 3, measured etch rates after we cleaned the chamber via DSE Clean for 30 minutes. The fourth stage, standard etch 4, would have been performed after a chamber wet clean if significant variation in etch rates were observed between the first three stages. The results for resist thickness and etch rates are contained in Table 3. The results for silicon etch depth and etch rates are contained in Table 4.

Reflectometry [nanospec2]							
wafer	measurement	top [Å]	middle [Å]	bottom [Å]	left [Å]	right [Å]	Average [Å]
standard etch 1	pre-etch	9793 / 9802	9757 / 9725	9768 / 9760	9845 / 9938	9792 / 9820	-
	post-etch	6134 / 5506	5149 / 5006	5775 / 5123	5217 / 5083	5358 / 5427	-
	difference	3659 / 4296	4608 / 4719	3993 / 4645	4628 / 4855	4434 / 4393	4264 / 4582
	rate [per loop]	91.5 / 107.4	115.2 / 118.0	99.8 / 116.1	115.7 / 121.4	110.9 / 109.8	107 / 115
standard etch 2	pre-etch	9802	9758	9792	9836	9790	-
	post-etch	5967	4975	5421	5195	5467	-
	difference	3835	4783	4371	4641	4323	4390.6
	rate [per loop]	95.875	119.575	109.275	116.025	108.075	109.765
standard etch 3	pre-etch	9821	9775	9798	9889	9797	-
	post-etch	5662	4926	4944	5231	5613	-
	difference	4159	4849	4854	4658	4184	4540.8
	rate [per loop]	103.975	121.225	121.35	116.45	104.6	113.52
standard etch 4	pre-etch	9816	9757	9797	9838	9791	-
	post-etch	-	-	-	-	-	-
	difference	-	-	-	-	-	-
	rate [per loop]	-	-	-	-	-	-

Table 3: detail of resist thickness reflectometry measurements and photoresist etch rate

Profilometry [alphastep]							
wafer	measurement	top [um]	middle [um]	bottom [um]	left [um]	right [um]	average [um]
standard etch 1	pre-etch	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	-
	post-etch	31.55 / 29.47	25.14 / 24.75	28.91 / 29.74	31.36 / 27.33	31.85 / 31.39	-
	difference	31.55 / 29.47	25.14 / 24.75	28.91 / 29.74	31.36 / 27.33	31.85 / 31.39	29.76 / 28.54
	rate [per loop]	0.7888 / 0.7368	0.6285 / 0.6188	0.7228 / 0.7435	0.784 / 0.6833	0.7963 / 0.7848	0.7441 / 0.7134
standard etch 2	pre-etch	0	0	0	0	0	-
	post-etch	30.39	24.25	27.7	29.83	30.34	-
	difference	30.39	24.25	27.7	29.83	30.34	28.502
	rate [per loop]	0.75975	0.60625	0.6925	0.74575	0.7585	0.7126
standard etch 3	pre-etch	0	0	0	0	0	-
	post-etch	29.8	24.19	27.71	29.59	30.38	-
	difference	29.8	24.19	27.71	29.59	30.38	28.334
	rate [per loop]	0.745	0.60475	0.69275	0.73975	0.7595	0.7084
standard etch 4	pre-etch	0	0	0	0	0	-
	post-etch	-	-	-	-	-	-
	difference	-	-	-	-	-	-
	rate [per loop]	-	-	-	-	-	-

Table 4: detail of resist thickness reflectometry measurements and photoresist etch rate

If we average over the set of measurements for each run, the measurements of photoresist and silicon etch rates can be summarized by Table 5. The final etch rate numbers were obtained from Tables 3 and 4, and used the fact that each loop of DSE FAT EBTr takes 8 seconds.

Run	PR etch rate [um/min]	Si etch rate [um/min]	PR selectivity
Baseline	0.0803 (0.0863)	5.581 (5.351)	69.5 (62.0)
Post-LN	0.0823	5.344	64.9
Post-DSE Clean	0.0851	5.313	62.4
Post-wet clean	N/A	N/A	N/A

Table 5: summary of etch rates across runs

These results suggest that the silicon etch rate varied by at most 5%, the photoresist etch rate varied by up to 6%. Repetition of the baseline etch rate test twice suggests a typical variation of Si etch rate between runs of 0.23um/min, which amounts to a 4% difference in etch rate between nearly identical chamber conditions.

It is important to note, the measurements for SE1 --baseline-- was done with the electrode placed at the wrong temperature. As such, further testing may be required to verify stable etch rates conclusively.

Summary

In summary, we have developed a process for performing shallow etches in the PT-DSE to undercut both LN and aluminum structures that are roughly 4 um wide. We characterized how changing the PT-DSE's electrode temperature, bias voltage, ICP power, and SF_6:O_2 ratio affects the horizontal/vertical etch rates and isotropicity through a half-fractional DoE. The results demonstrate that our isotropic etch process is robust and capable of releasing a variety of structure geometries from Si substrates in the PT-DSE, provided that they are fabricated from materials that are not etched by SF_6.

Future Work

In the future, near term goals involve receiving the results for the VPD-ICPMS contamination tests and submitting our data and analysis to the PROM committee. We also intend to refine our cleaning procedure post-release to eliminate the presence of crosslinked photoresist. We believe that placing samples into the Matrix plasma asher directly after etching in the PT-DSE may alleviate the issue.

Intermediate term goals require us to validate that the PT-DSE release process is compatible with quantum acoustic devices. For this, we will fabricate full phononic nanomechanical resonators and measure the corresponding quality factors. We will compare these quality factors to similar devices etched with the previously used Xactix XeF2 etch process. One potential concern is that subjecting the lithium niobate to an energetic plasma could modify the material properties such that it compromises the device performance, namely, long coherence times. We also intend to check if niobium structures are compatible with the SF_6 etch chemistry.

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Acknowledgements

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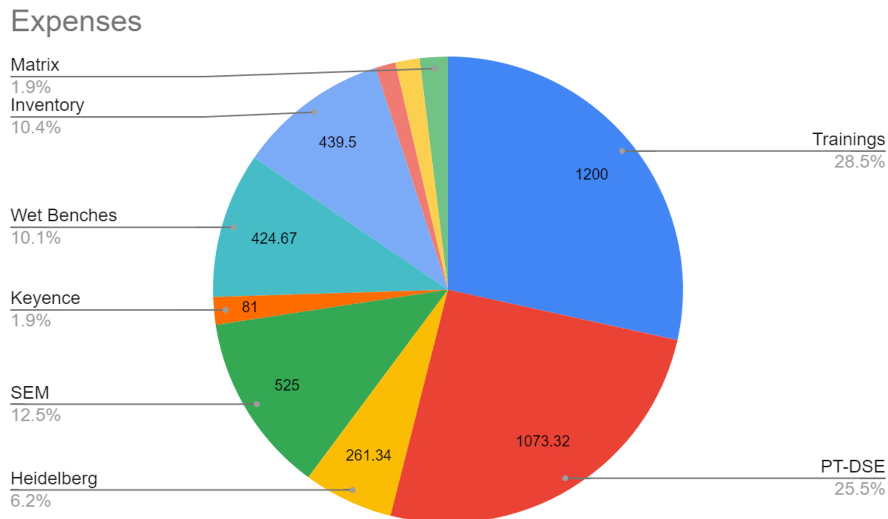
Expenses

Our cleanroom expenses over the course of the 10 week quarter were as follows,



Total ($)	**4215.41**
Trainings	1200
PT-DSE	1073.32
Heidelberg	261.34
SEM	525
Keyence	81
Wet Benches	424.67
Inventory	439.5
Woollam	58.33
Ion Mill	70.58
Matrix	81.67