Si and Glass Flip Chip Bonding with Solder Paste and Laser Cut Tape Stencils

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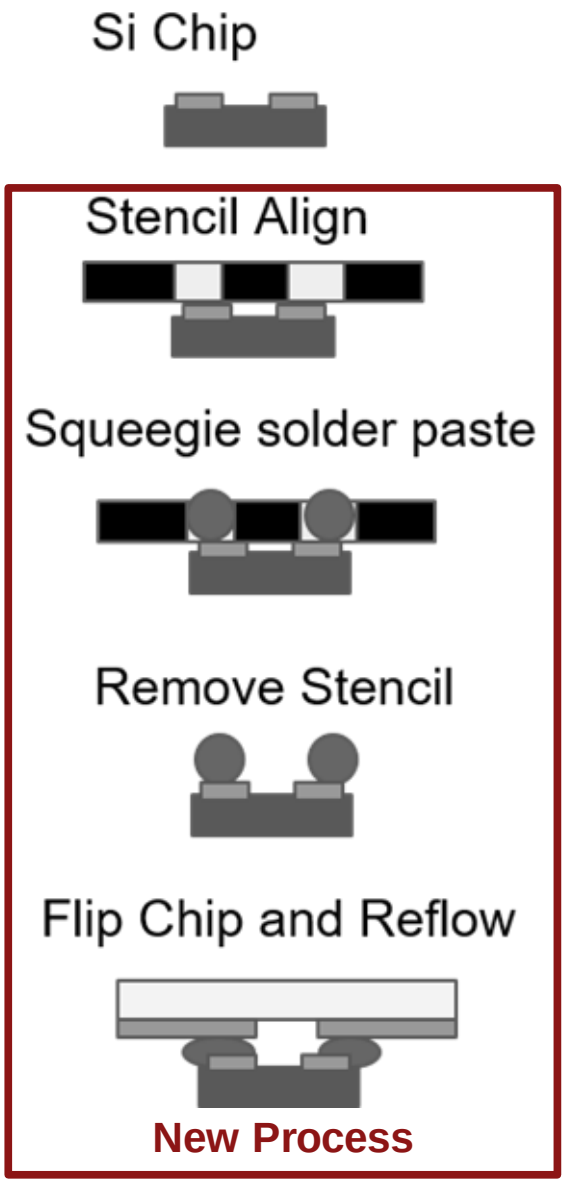
12/07/16

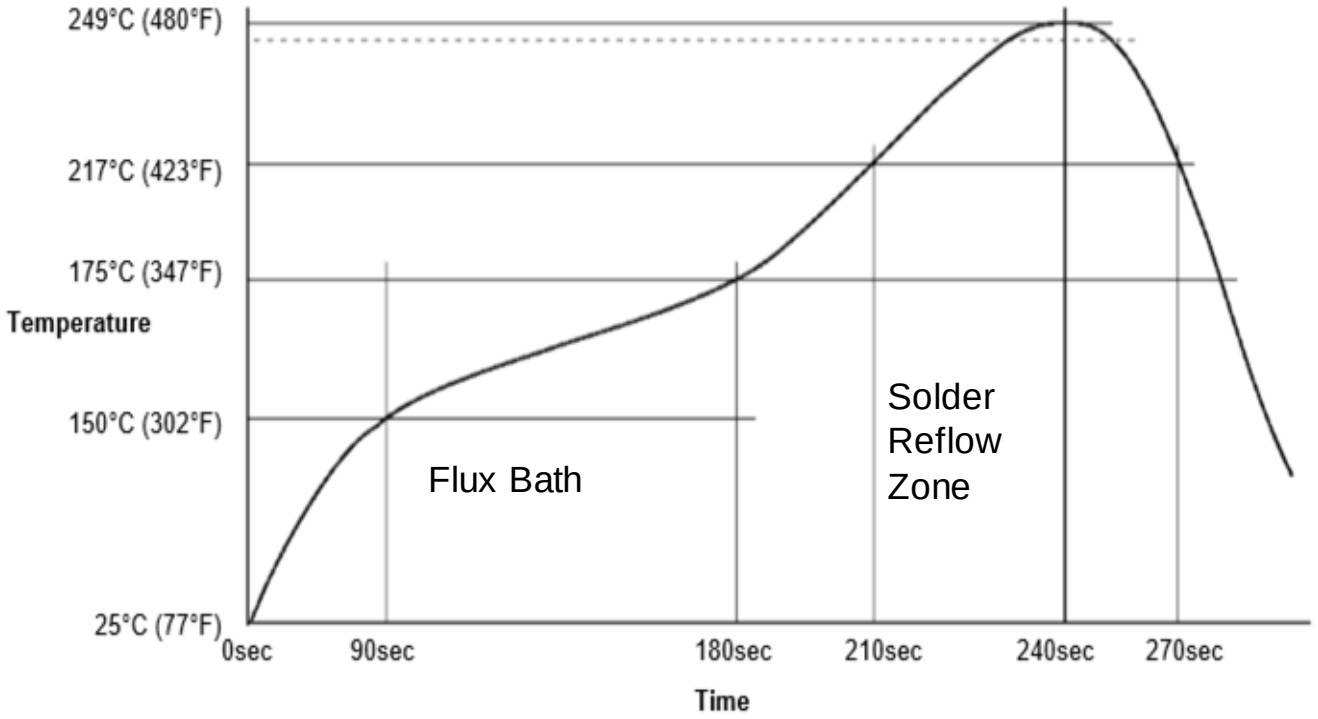
Motivation / Goals

- Evaluate Finetech flip chip bonding capabilities
- Develop a process for solder paste bonding
- Electrically quantify solder joint resistance

Variables in the Process



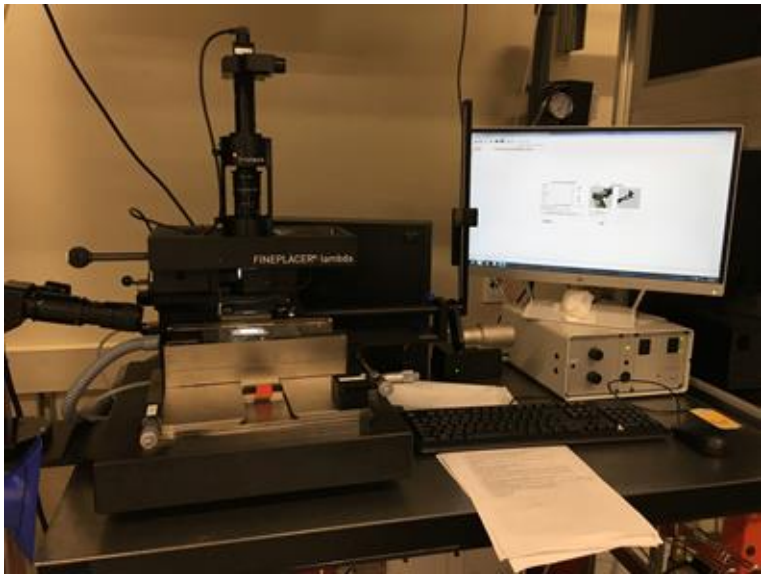
- Choosing a cheap and lead-free paste (Tin/Silver/Copper Solder (SAC 305))
- Determining reflow temperature parameters



- Determine mechanisms for a new process on a new machine

Overview

1. Device Preparation
2. Stencils
3. Solder Reflow Curves
4. Electrical Results
5. Design Considerations
6. Future Project Suggestions



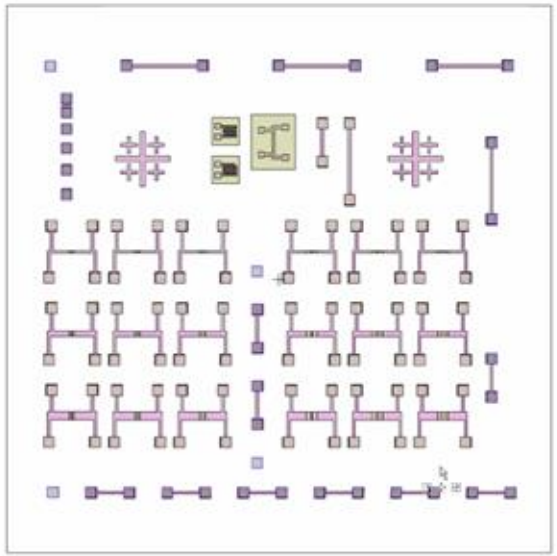
FINEPLACER® lambda

Devices Under Test

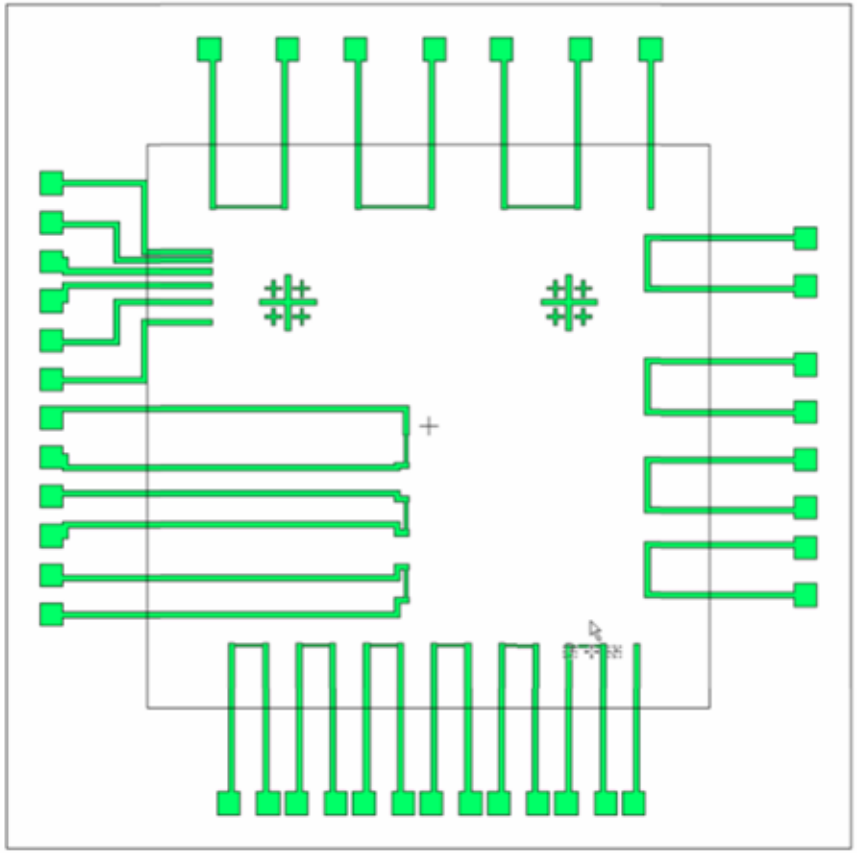
- Silicon die
- Glass Substrate
- Tin/Silver/Copper Solder
- 150 nm Nickel pads

- Daisy chains (2 sizes)
- Kelvin test structures
- Open face reflow structures

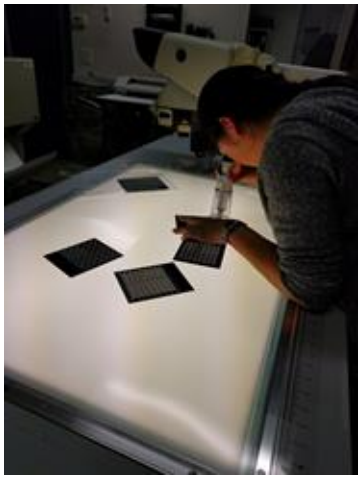
Device Die

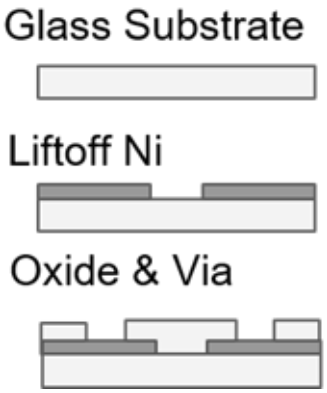


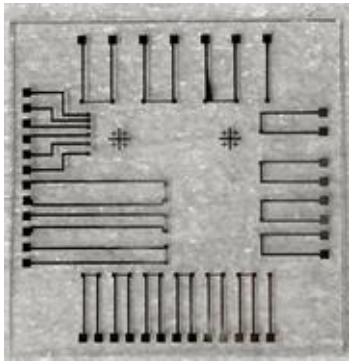
Substrate Die

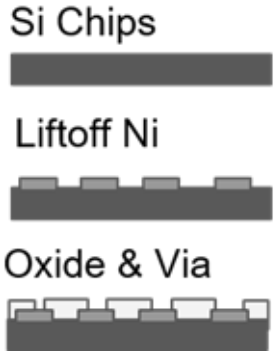


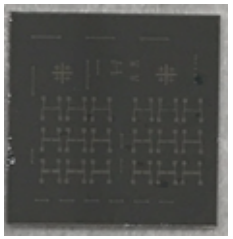
Device Preparation - the SNF Weeks



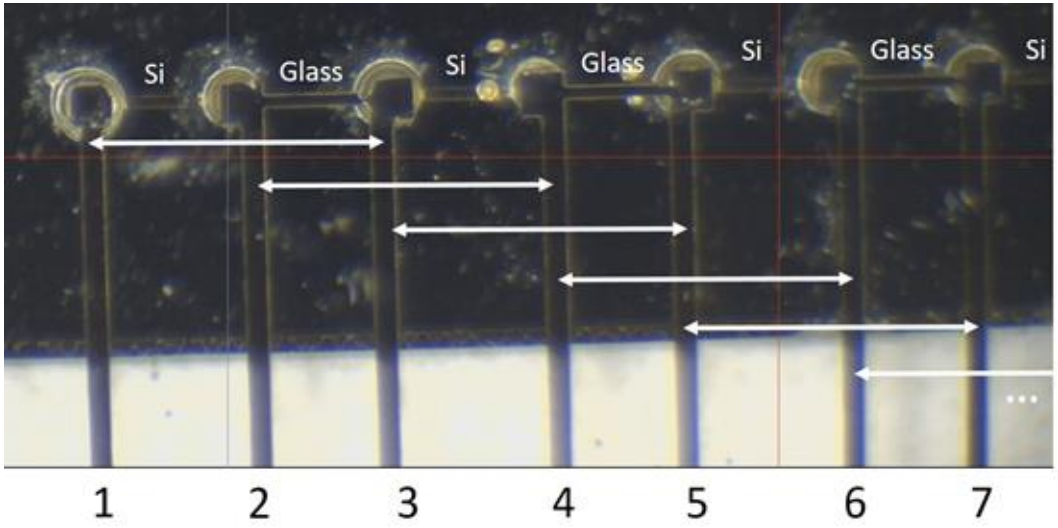


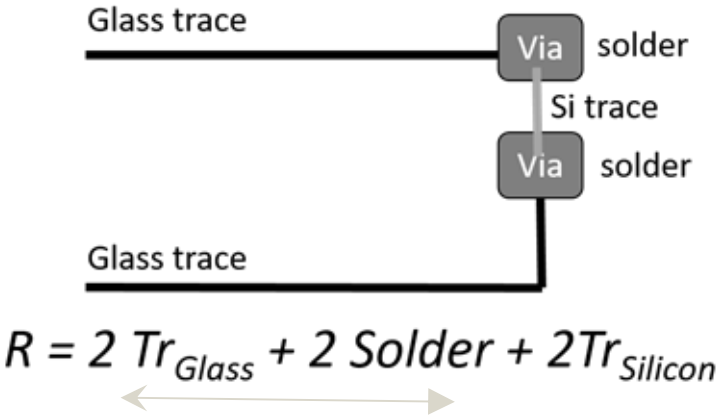




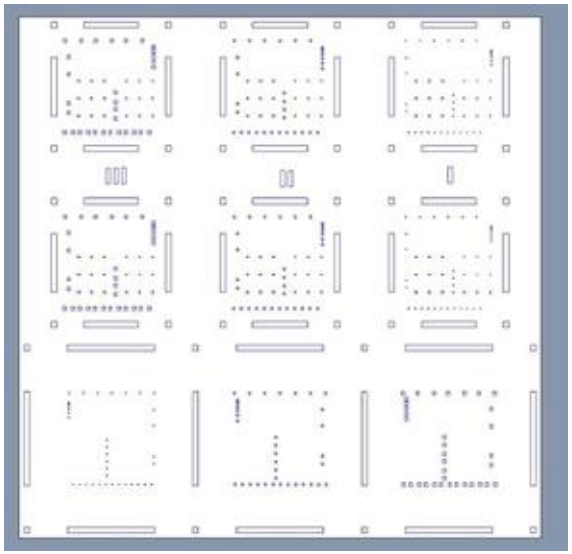


Transparency Masks





Stencil Design



Quick-Turn Rework Stencils

These laser cut stencils are typically used to manually print a single component on a printed circuit bo

- Maximum Size 2" x 2"
- Available with or without flaps (Flaps facilitate handling)
- Mainly used for PCB rework but can used for prototype PCB assembly of simple boards

Squeegee Kit 1

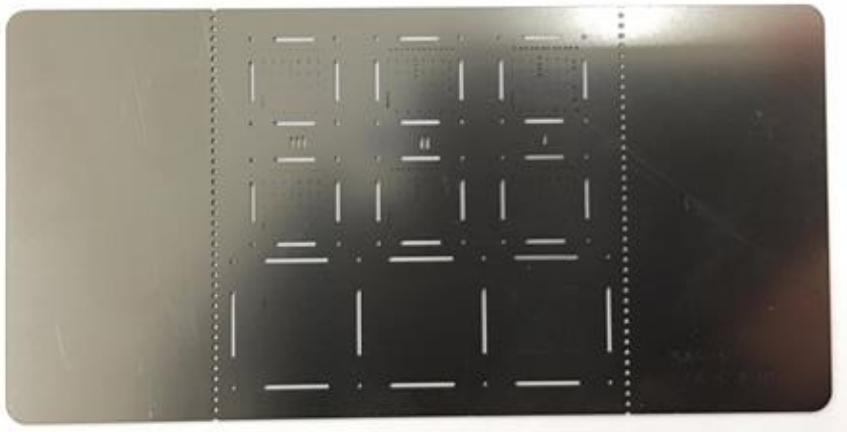
Each mini squegee kit contains 1 squeegee blade positive grip handle and the following stainless steel squeegee blades:

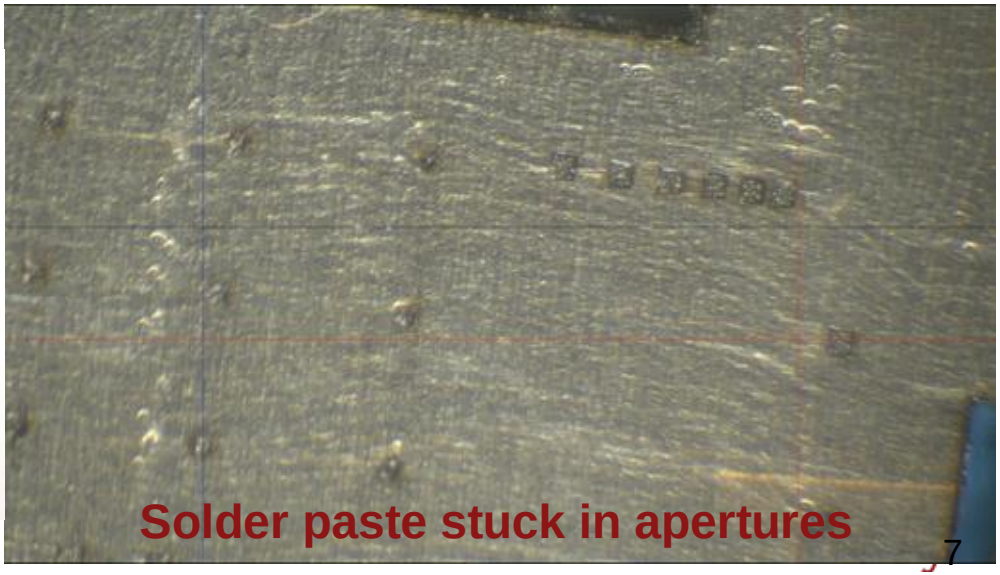
SQBLADE040 10.2mm/0.4" width Qty 2

SQBLADE060 15.2mm/0.6" width Qty 2

SQBLADE080 20.3mm/0.8" width Qty 2

Lead Time: In stock and ready for shipment **Price:** $35.00 Learn more





Metal Stencil Guidelines for the Future

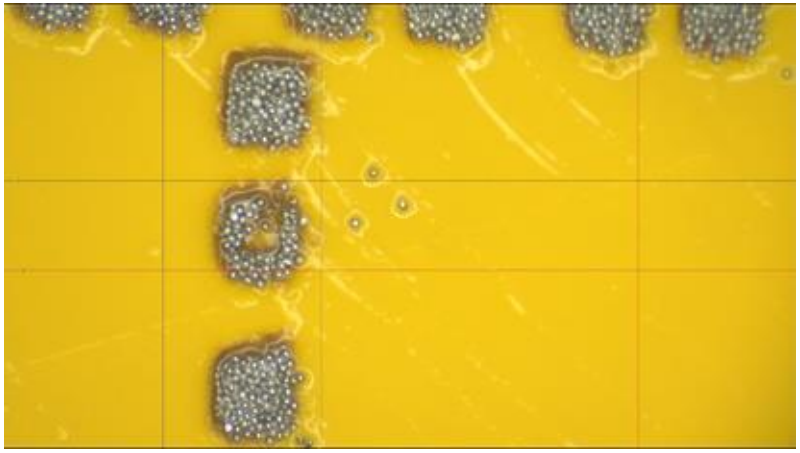
- Should be flush against surface
- Must be thin so surface tension of solder paste on substrate is greater than tension on stencil sidewalls
- $80 is cheap for a stencil … :((pay for material and laser time)
- Finetech has attachments for single die stencils, which are cheaper
- Type 3 solder paste particle size was too large (25-40 um) for our apertures (100 um). Need to obtain type 5 or 6 solder paste
- Design to include windows and large and easy alignment features

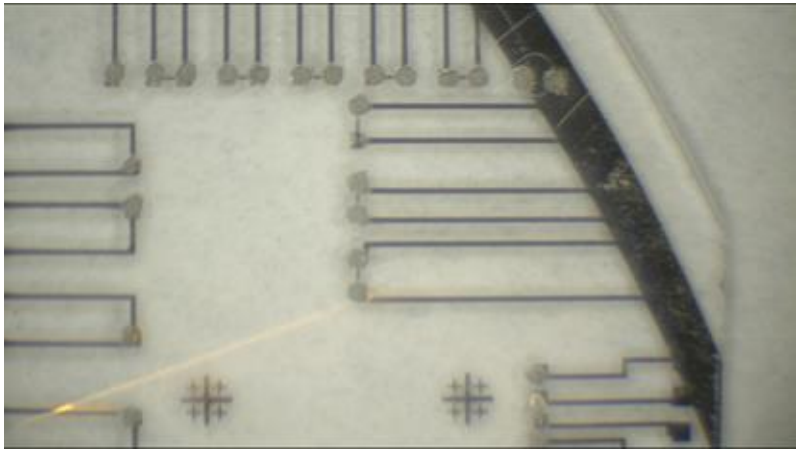
STANDARD POWDER RECOMMENDATIONS

Rule-of-thumb: **A minimum of four to five powder spheres should span the width of a stencil aperture.**

0.050 inch pitch -- Type 2
0.025 inch pitch -- Type 3
0.016 inch pitch -- Type 3
0.012 inch pitch -- Type 4 or 5
0.008 inch pitch -- Type 6

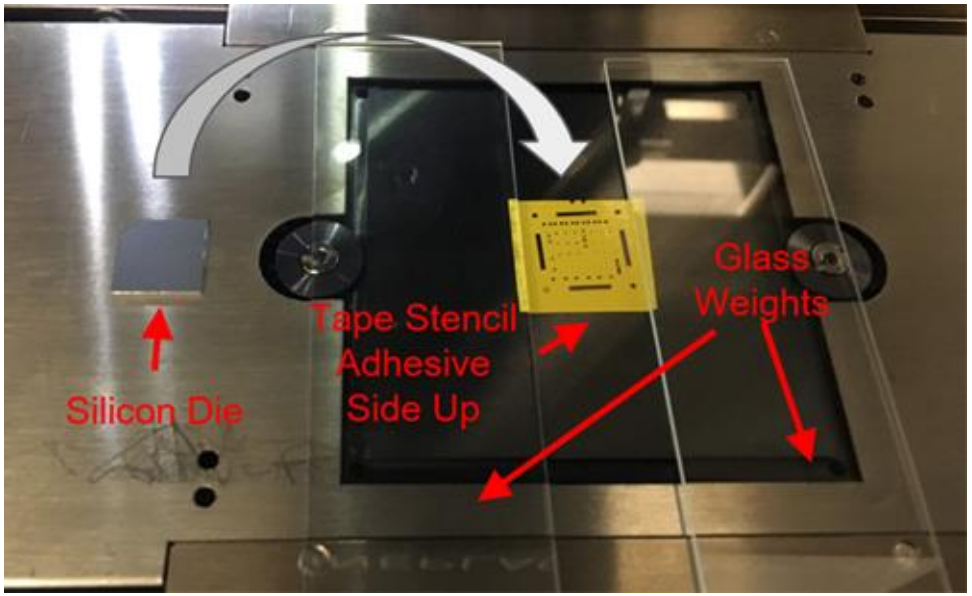
BUT We Figured out Tape Could Work!





Stencil(s) - Tape

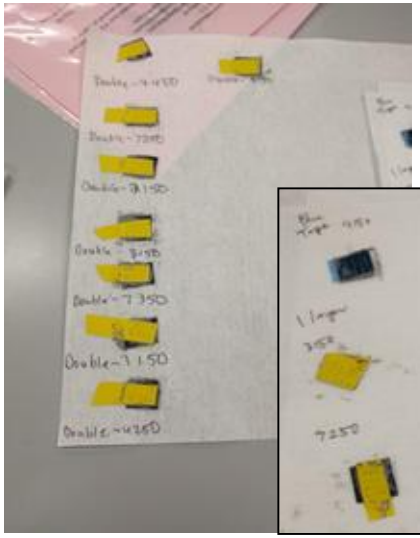
Laser Cut

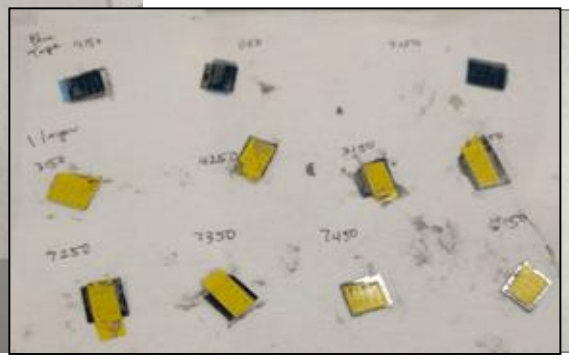


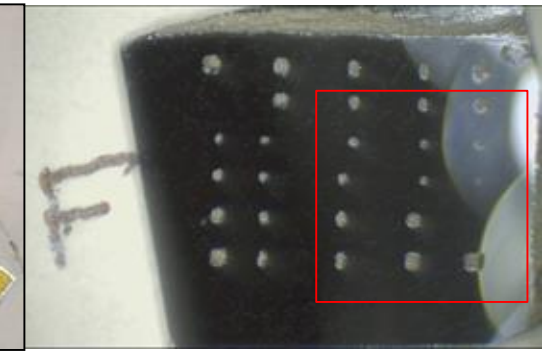
And We Characterized It

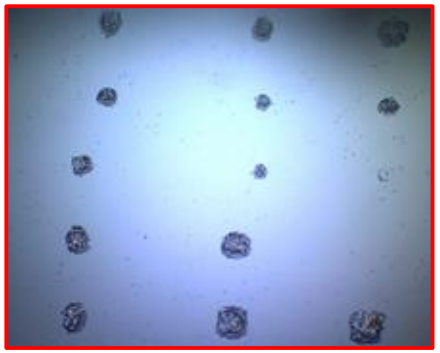
Label	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S
Speed (%)	7	7	2	3	7	1	4	4	4	1	7	3	4	2	1	7	7	7	4
Power (%)	4	2	1	1	3	1	2	1	1	1	2	1	2	1	1	2	3	4	1
Tape	2 Yellow Dots								Blue Tape			1 Yellow Dot							

Epilog Fusion M2 Laser
Laser Constants (50 W CO2 Laser):
Frequency (50%), Hairline width, Vector Cut



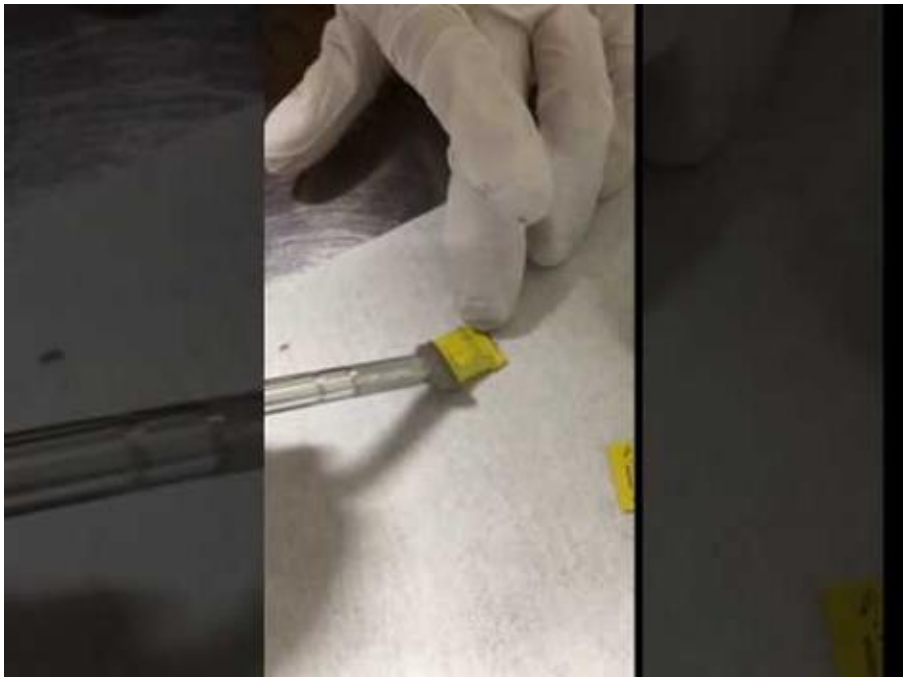


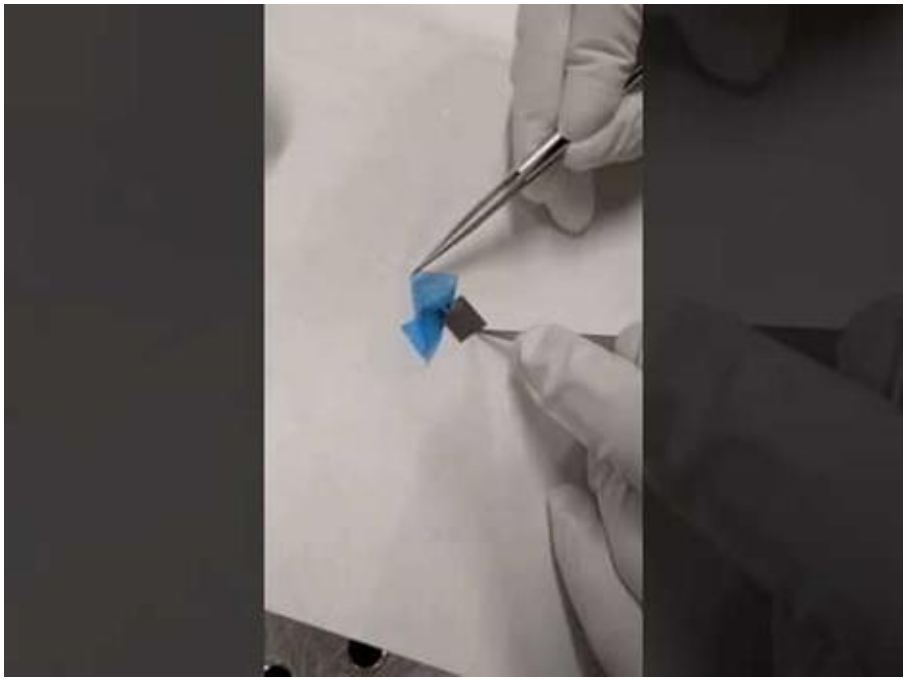




But How Does One Apply Solder Paste?

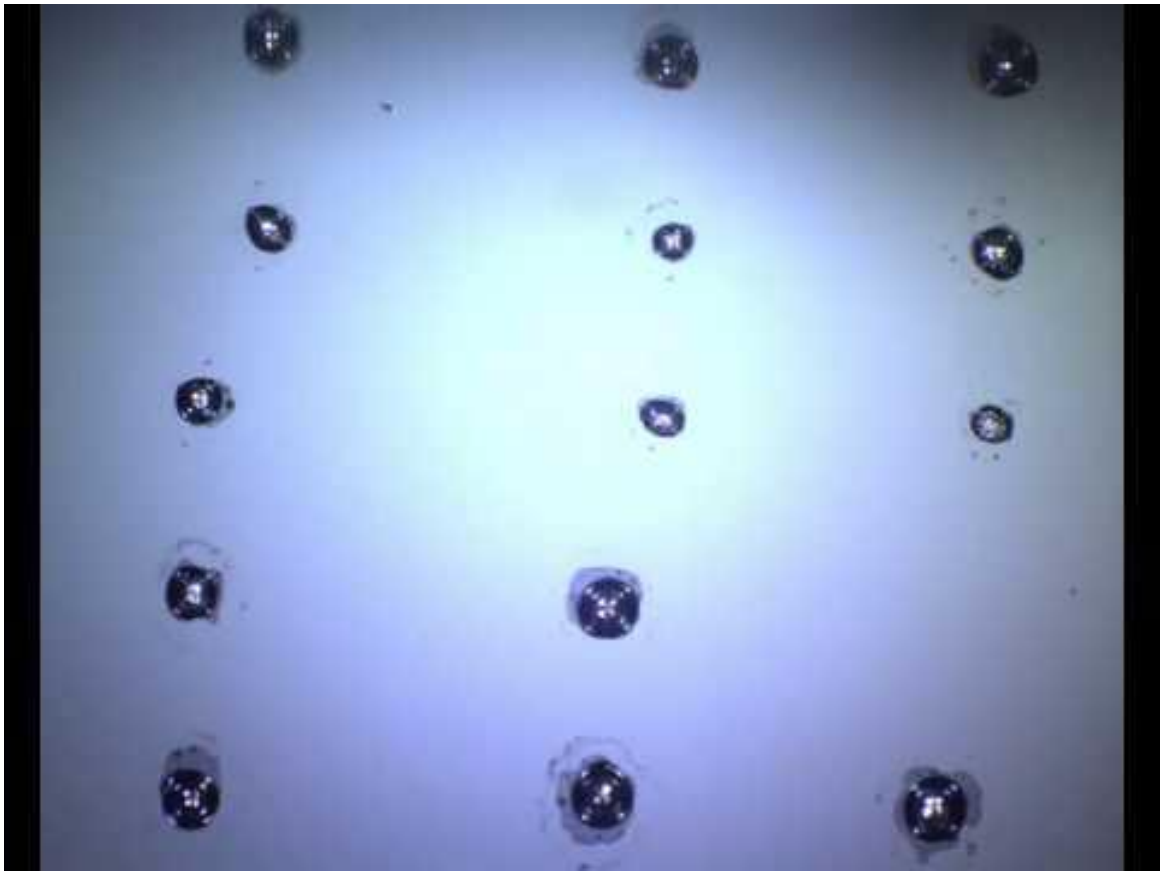
Click me! I'm a video!





Video!

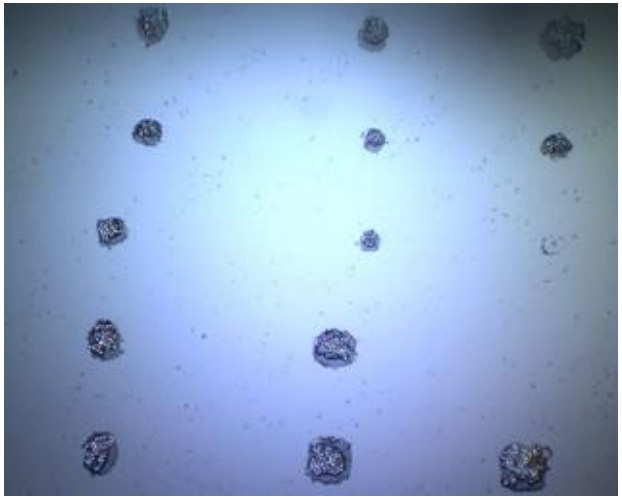
Click me! I'm a video!



Reflow Results - Laser Cut Tape on Blank Si

Good Melting Sample (F)

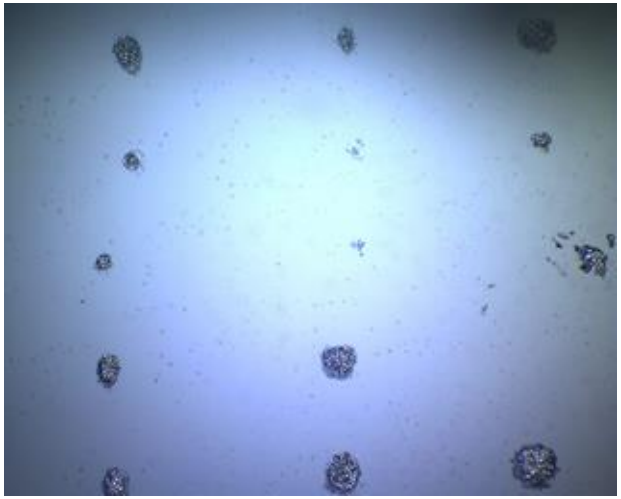
Before



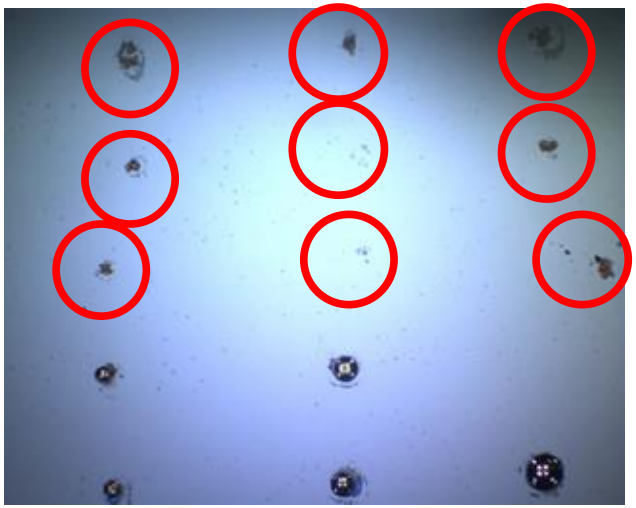
After

Bad Melting Sample (H)

Before

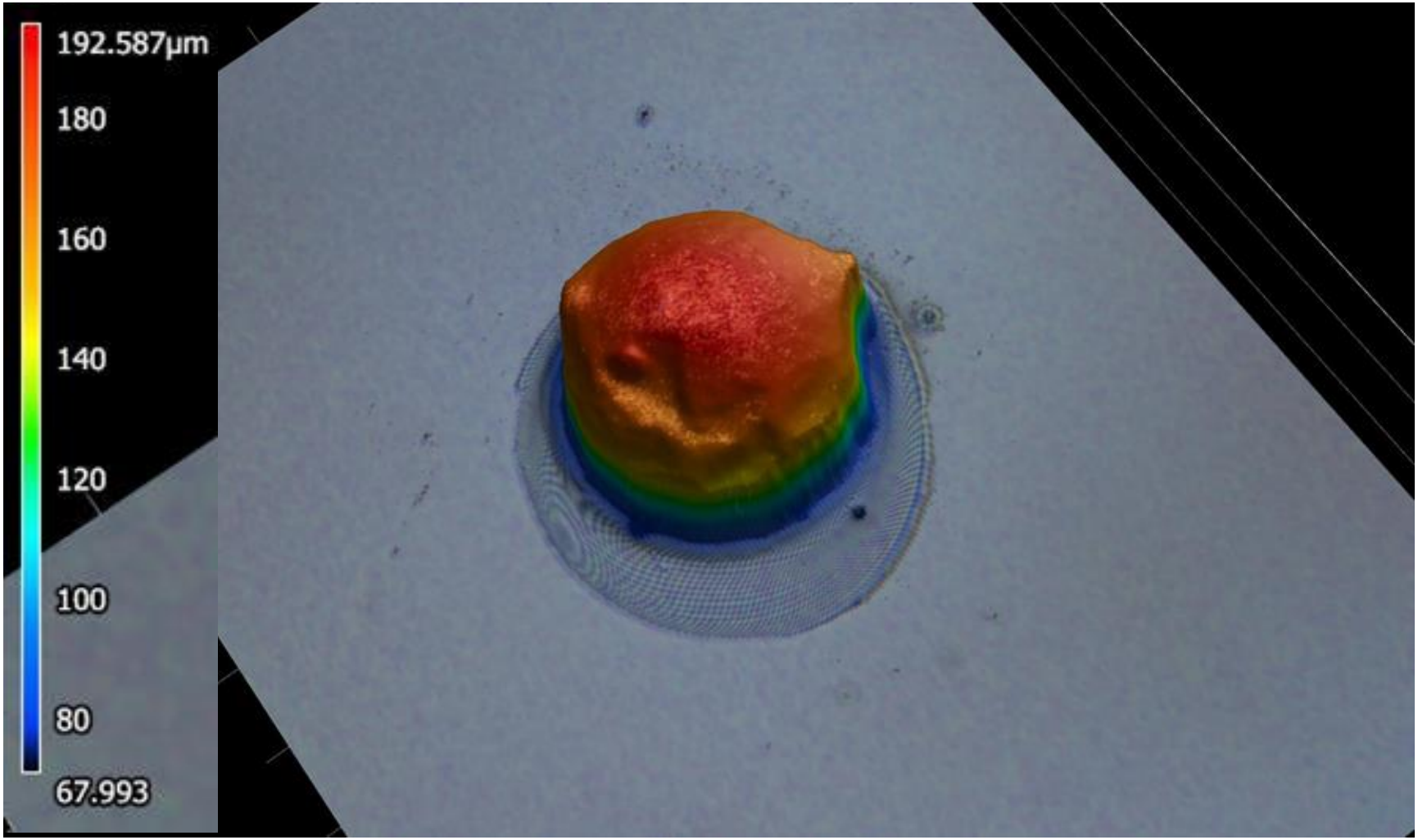


After



Metric: Laser cut apertures for consistent and repeatable reflow

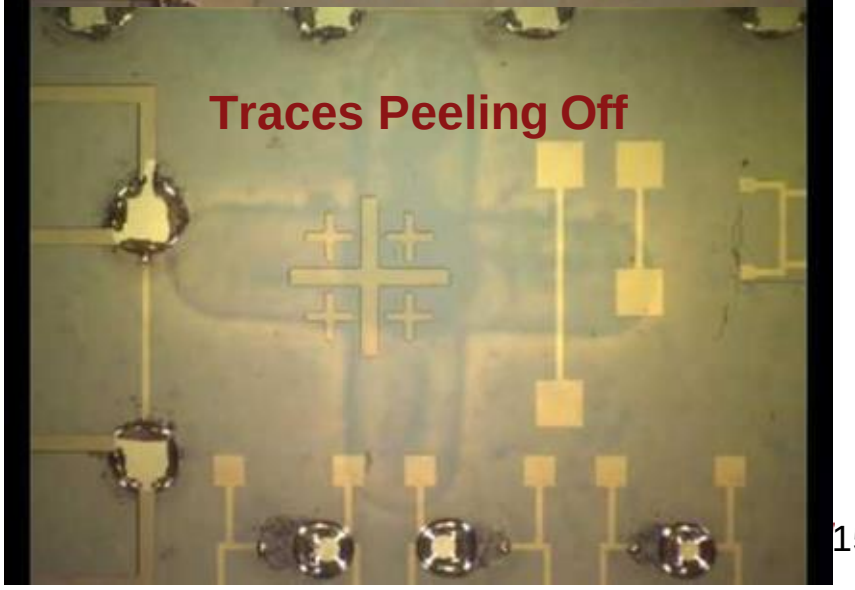
Image from Keyence Demo Tool on Dec 2



Common Failure Modes of Flip Chip Bonding

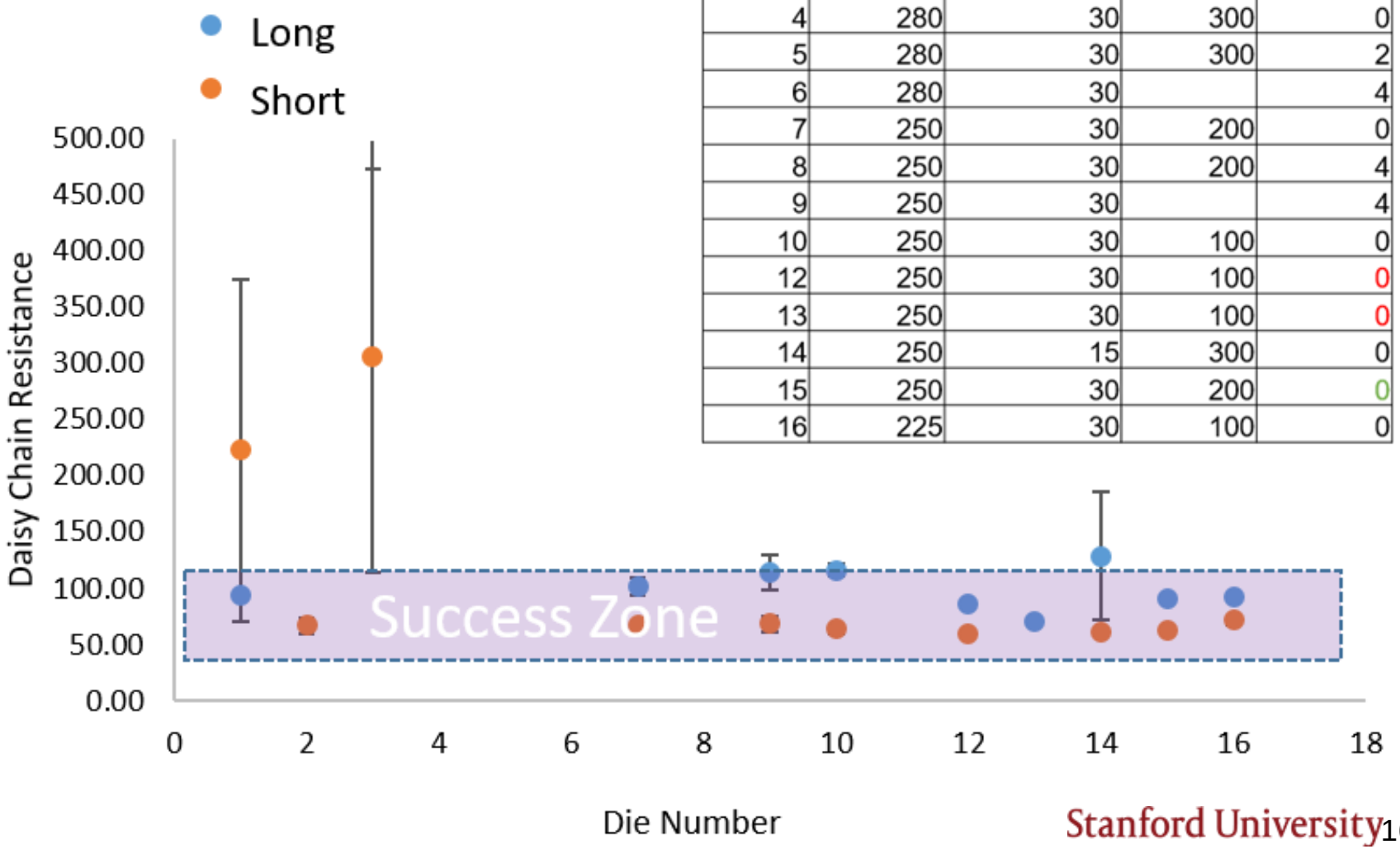
Click me! We're all videos!

- Die misalignment due to z height of solder beads
- Die shifting during reflow
- Broken traces from high temperatures and long plateaus

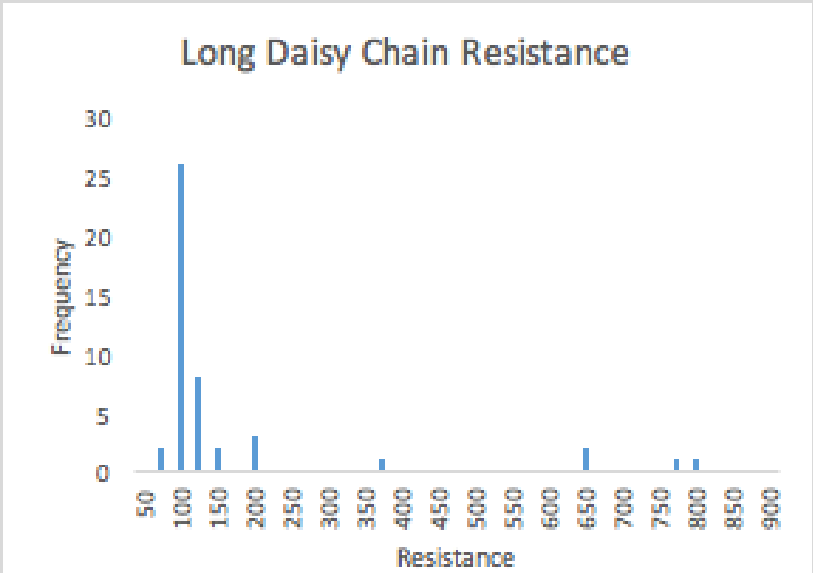


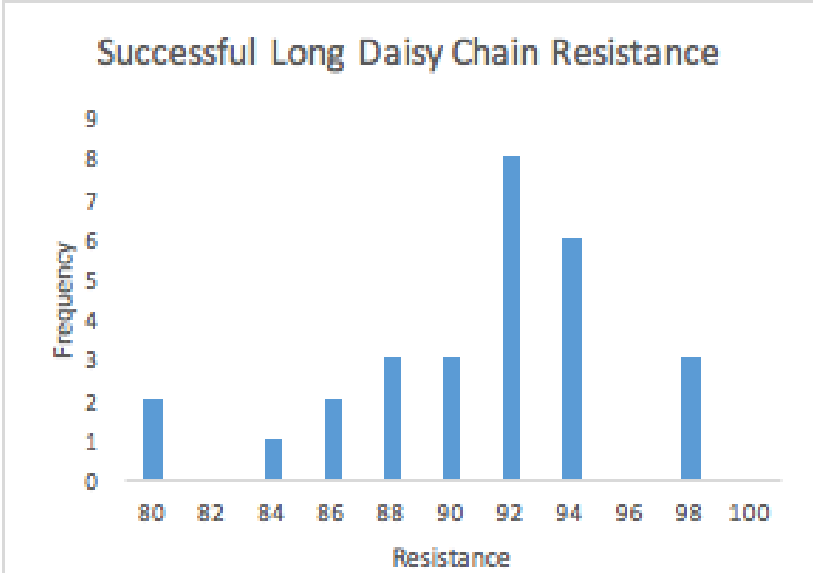
Experiment Runs

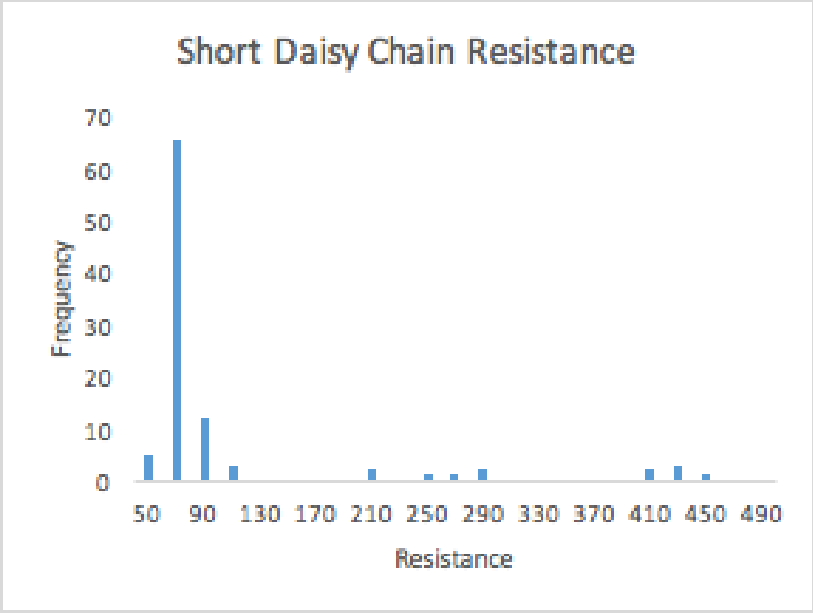
number	Temp (deg C)	Plateau Time (s)	Bond Pad Size (um)	Force (N)
1	250	45	200	0
2	250	30	300	2
3	250	30	200	4
4	280	30	300	0
5	280	30	300	2
6	280	30		4
7	250	30	200	0
8	250	30	200	4
9	250	30		4
10	250	30	100	0
12	250	30	100	0
13	250	30	100	0
14	250	15	300	0
15	250	30	200	0
16	225	30	100	0

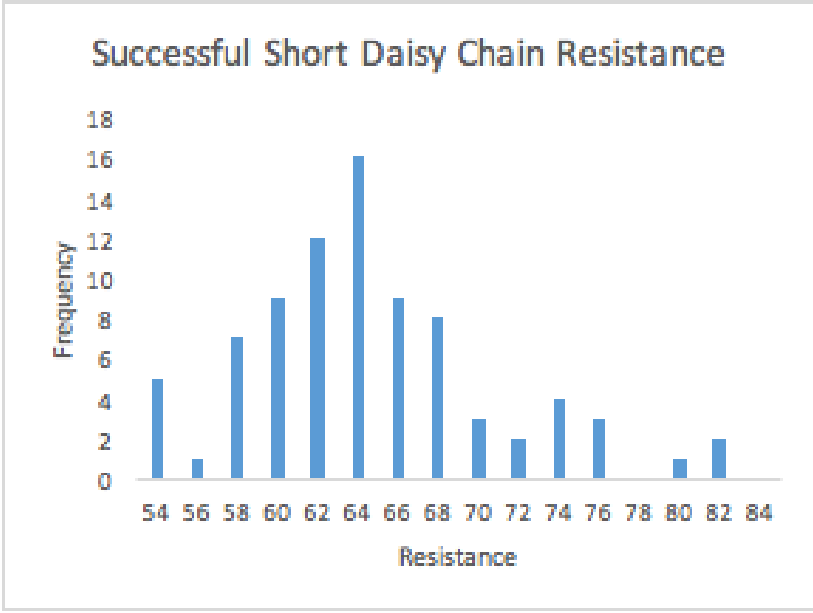


Results


Long Daisy Chain Resistance
Frequency
30
25
20
15
10
5
0
50 100 150 200 250 300 350 400 450 500 550 600 650 700 750 800 850 900
Resistance

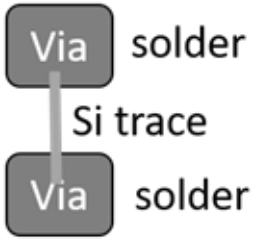

Successful Long Daisy Chain Resistance
Frequency
9
8
7
6
5
4
3
2
1
0
80 82 84 86 88 90 92 94 96 98 100
Resistance

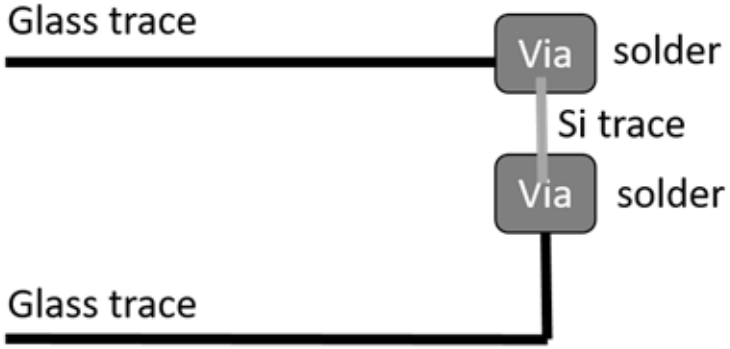

Short Daisy Chain Resistance
Frequency
70
60
50
40
30
20
10
0
50 90 130 170 210 250 290 330 370 410 450 490
Resistance


Successful Short Daisy Chain Resistance
Frequency
18
16
14
12
10
8
6
4
2
0
54 56 58 60 62 64 66 68 70 72 74 76 78 80 82 84
Resistance

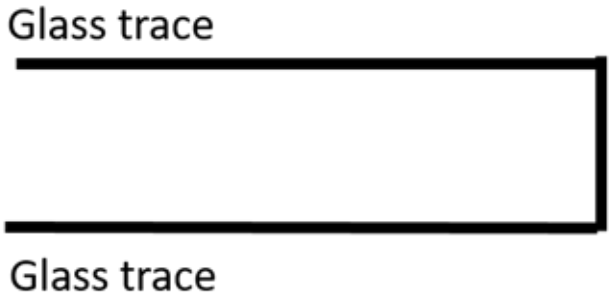
Four Point Probe Measurements - Solder Joint Resistance

$R_{4pp} = 2\ Solder + Tr_{Silicon}$

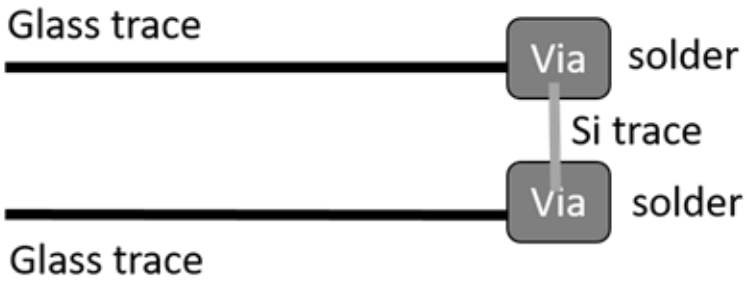




$R = 2\ Tr_{Glass} + 2\ Solder + 2Tr_{Silicon}$



$R = 2\ Tr_{Glass} + Tr_{Silicon}$

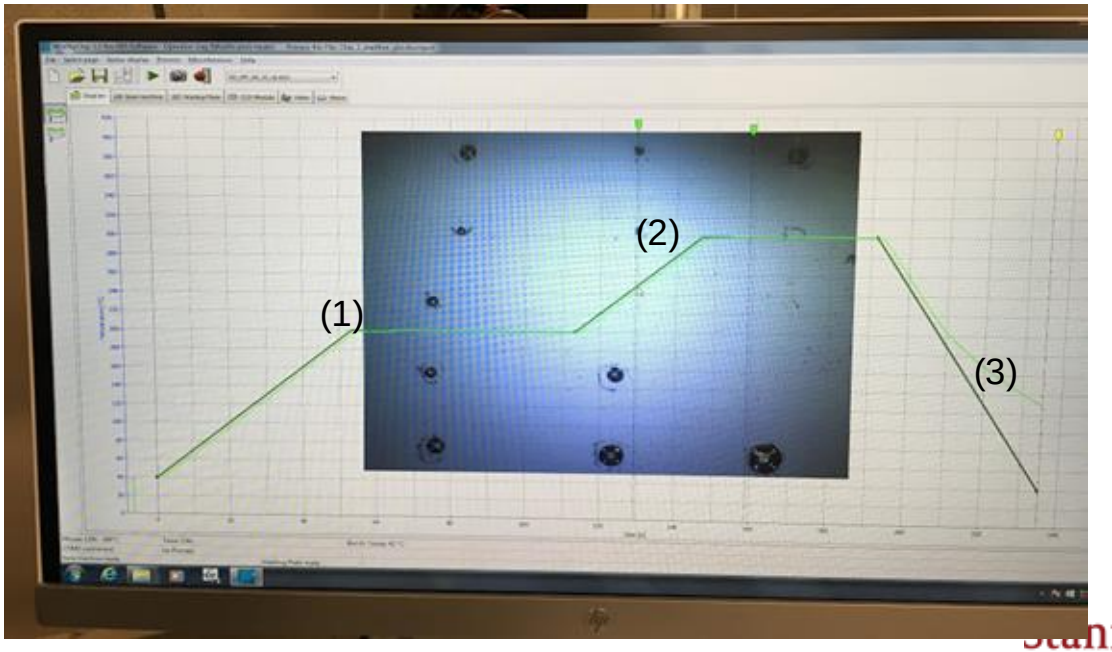


$R = 2\ Tr_{Glass} + 2\ Solder + Tr_{Silicon}$

Average Contact Resistance of Good Solder Joint: 2-3 Ohm, but variation in fabrication and measurements

Lessons from Solder reflow Experiments - SAC 305

1)Flux Temp and hold time	200 C, 60 seconds
2)Reflow Temp and hold time	250C, 15-30 seconds
3) temperature ramps	3 degC/sec
Force	0 N, alignment issues may happen
Bond Pad Sizes	all worked (100 to 300 um)
Heating side	Heat from bottom, Chip head too small



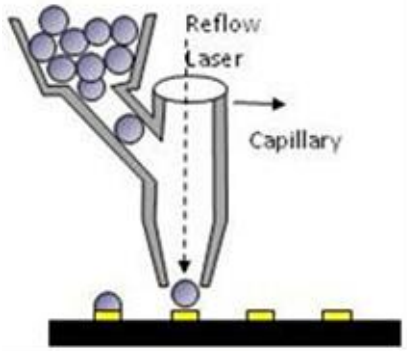
Future Experimental Design Considerations

- Characterize solder paste temperature profile with open face reflow experiments
- Include space on edge of tape stencil for glass weights
- Design to include windows and large and easy alignment features
- Test flip chip alignment with clear substrate before permanent bonding
- Use thick metal pads (>500 nm) to prevent trace breakage
- Maintain oxide top layer to prevent excessive capillary movement during reflow
- Use base plate for heating instead of head
- Place alignment mark at center of finetech camera viewer

Future Suggested Projects

- Solder voids with Xray Microscopy
- Bond strength via Instron pull tests
- Apply to real devices!
  - EE 410 transistors anyone?
- Shorting - density of pads
- Alloys - High and Low Temp Solder
- Uniformity of Bump Arrays across die
- Use spheres directly
  - pactech.com

Instron in SMF



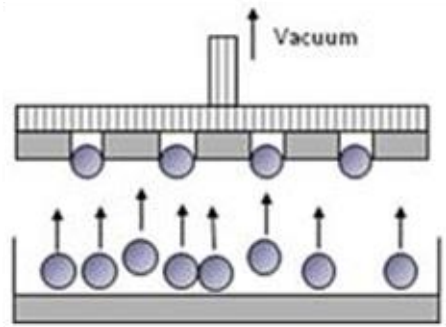


Image credit: Pactech.com

Acknowledgements

- Mentors: Usha Raghuram, J Provine, Astrid Tomada
- Prof. Howe, Mary Tang, Caitlin Chapin, Michelle Rincon
- Industry Mentors from Class!
- Finetech: Leigh Jackson
- SNSF: Shiva Bhaskaran, Keyence: David Hayes