C-V Measurement results on Capacitors from "Golden Silicon" versus EE410 Cap Samples:

This report discusses the CV measurement result done in SNF measurement Lab Micromanipulator station using the CV sweep algorithm (which controls the Agilent 4275A LCR Meter). A known good sample of oxide (130 Ang) capacitor fabricated elsewhere was used to calibrate the measurement setup prior to measuring the EE410 Sample. Results from both measurements are presented in this report.

(1) Results from Capacitors from Golden Silicon:

An intrinsic Area Cap of (130 Ang +/- 12) thick gate oxide (Area=100 um*100 um) with a $POCl_3$ - doped Poly plate was used to calibrate the measurement setup. The CV sweep was from +5v to -5v D.C. , with 10 mV small signal a.c. sweep at high frequency (100 kHz & 1 MHz). This 2-terminal structure has a **Poly Tap**, which is surrounded by N+ Source/Drain region (to mimic an NMOS) and a surrounding C-shaped ring of **P-well Taps** which is isolated by the LOCOS isolation w/ field threshold implant from the N+ Source/Drain region (left floating for the measurement). The x-sectional and top view of the structure is given in the next section. The parallel R-C model was used for the measurement since a good substrate connection was available. In manual measurement, usually an open and short calibration is recommended up to the probe tip point.

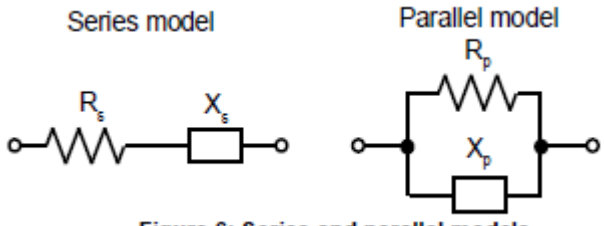
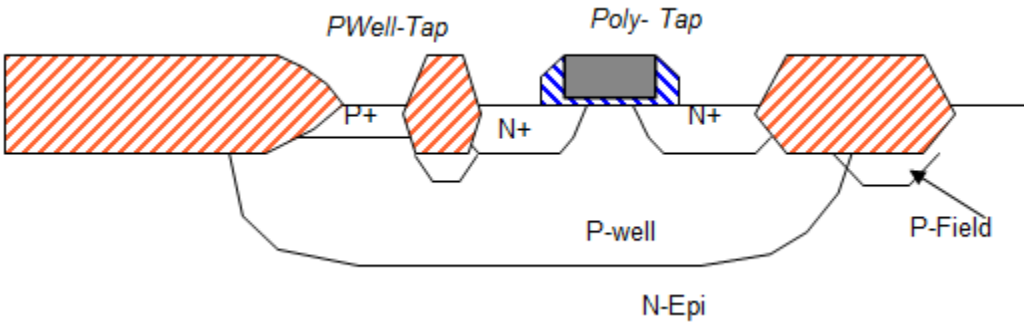
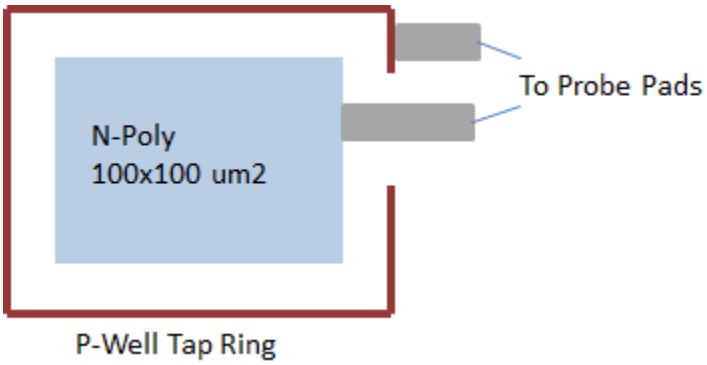


Figure 6: Series and parallel models

Structure X-section and Top view:





Calculation:

Cox = ε* Area / Tox =

=(3.9 * 8.854 * 1E-12)*(100 *100 *1E-12)/(130*1E-10)

= 2.6562E-11 Farad= 26.56 pF

Measurement Results:

Oxide C-V and I-V characterization was done. Results are shown in the next page.

1. CV Sweep & Tox : Measured Cacc= 26.5 pF ; Measured Thickness = 129 Ang.

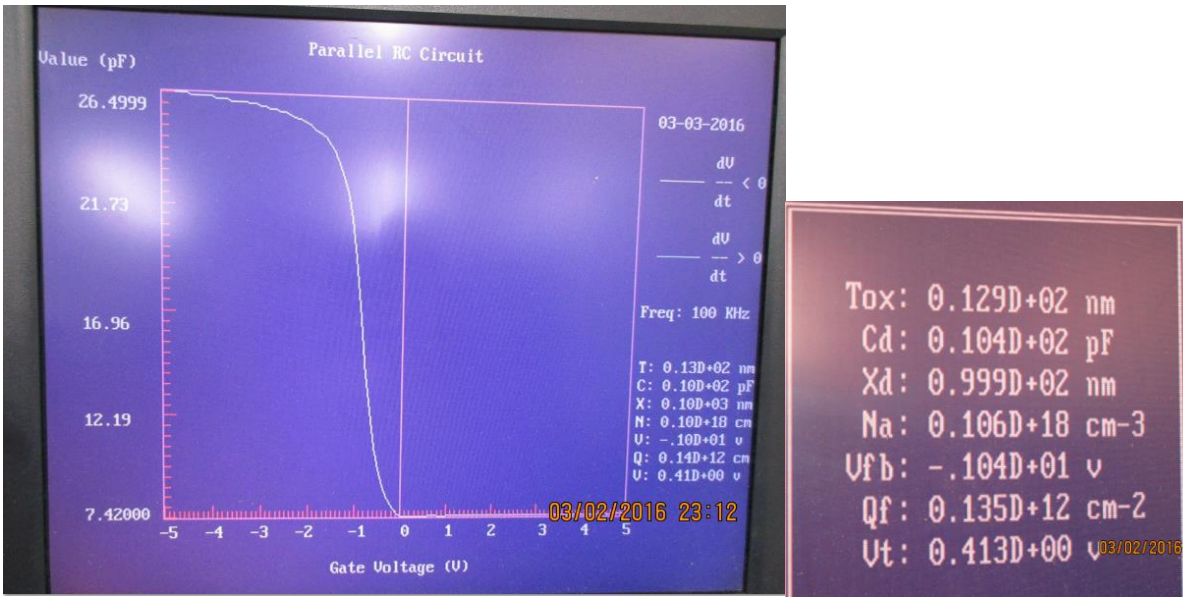


Fig 1: CV measurement result of provided sample

2. Oxide Fowler/Nordheim Tunneling data:
   Breakdown field= (20*1E-6)/(130*1E-8) = 15.4 MV/cm. (dry oxide)

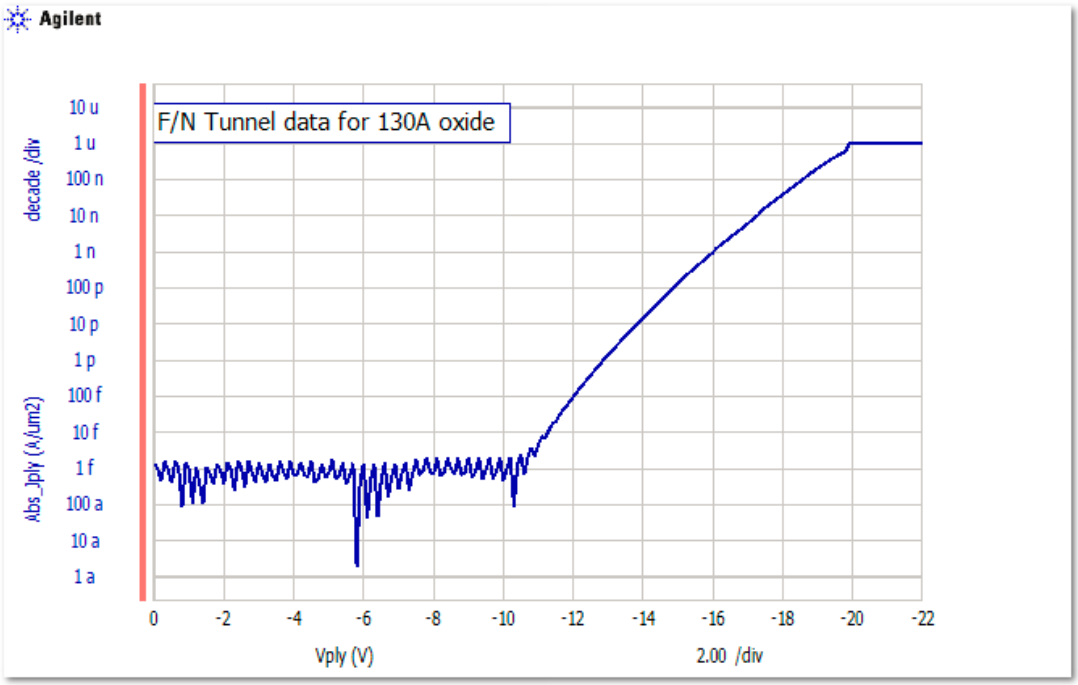


Fig 2: F/N Tunneling current measurement

(2) Results from EE410 Sample (sample provider: Muyu Xue):

The samples provided had Pt-gate terminal, surrounded by Source/Drain terminals, however no dedicated well tap was available. The backside of the wafer had Al-plating after the native oxide was removed by HF-dip. Oxide area was 50x50 um^2 and provided value of oxide thickness is 40 nm. i.e, The equivalent capacitance of this structure will be **2.15 pF**. (which is about 12x less than the previous sample). The X-section drawing and Top drawing for the MOSFET used for Oxide thickness measurement is provided below (source: EE410 course material).

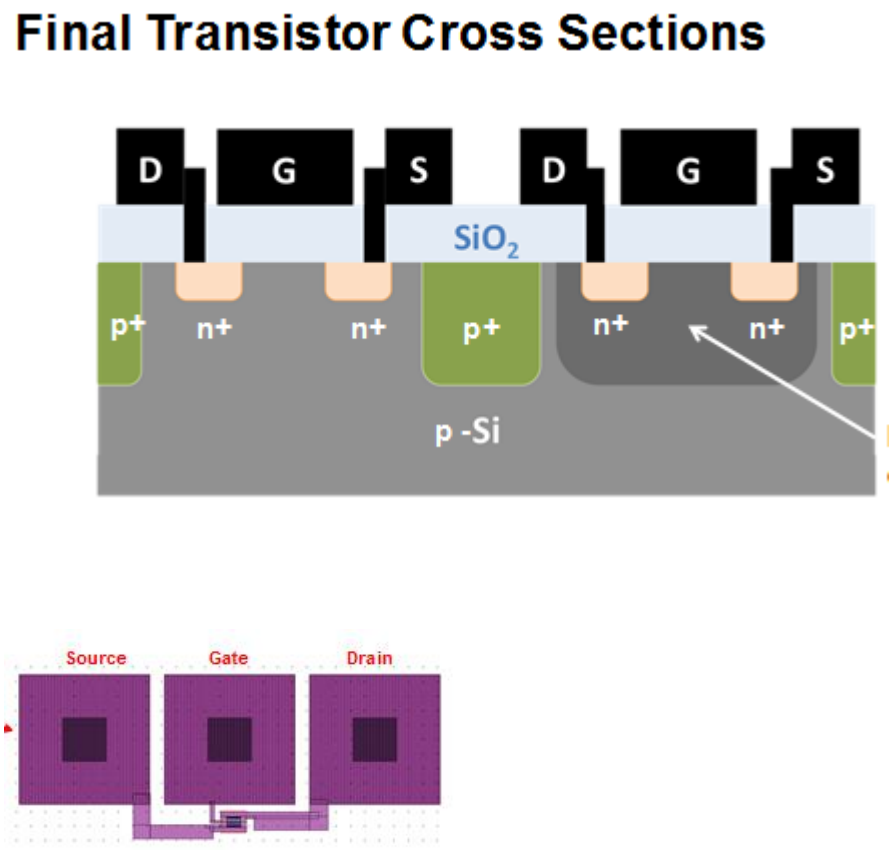


Fig 3: Transistor X-section in EE410

Several attempts were made to connect the backside of the wafer to Cap-Low by using an Aluminum foil underneath the wafer. A myler sheet was put in between the chuck and Aluminum foil to isolate the chuck series resistance from

the measurement. Case (a): The parallel R-C model yielded a very high thickness value with plenty of erratic measurement points in CV sweep. Case (b): The series R-C model with Cap-High at Al-foil gave 380 nm. The series R-C model with Cap Low to the Al-foil gave 70 nm. It is noted that the Al-foil did not provide a continuous smooth surface and may present some air gap in between the wafer & the Al-foil.

In the final attempt, Case (C): a second probe was put very close to the gate pad, i.e, on the silicon (the wafer is not passivated) and connected to Cap-Low, while Cap-High connected to Gate pad and series R-C model was used to measure the thickness of 70 nm. It is not clear how much native oxide would be present on silicon, even after scratching the surface with the probe tip. The result is still about 1.8x off the expected value.

The difference in measured capacitance between parallel vs. series R-C model is due to the loss in the DUT from dissipation factor [$D= \omega C_s R = 1/Q$], i.e, from the series resistance component. The difference in measurement value in Cap-High connected to Al foil vs. Cap-Low connected to Al-foil [case (b): 380 nm vs. 70 nm] points out there is stray capacitance & admittance between Cap High terminal and ground, when Cap High is connected to Al-foil.

Therefore, it is clear from the difference in results that a P-well tap around the structure, which will eliminate a lot of series resistance from connection through bulk or thickness of silicon, is one of the factors affecting the result significantly.

(3) Suggested improvements on C-V Measurement Structures:

The wafers under test were from NMOS-Depletion process flow. This flow employs very few number of processing steps compared to golden silicon used to calibrate the measurement. However, it is noted that, these wafers have dedicated MOS structures with a 300 um diameter pad size and dedicated implants. Expecting a 40 nm oxide thickness, the accumulation capacitance would be about 61 pF. Variation of the basic structure has p-substrate, P+, high VT and S/D N+ implants.

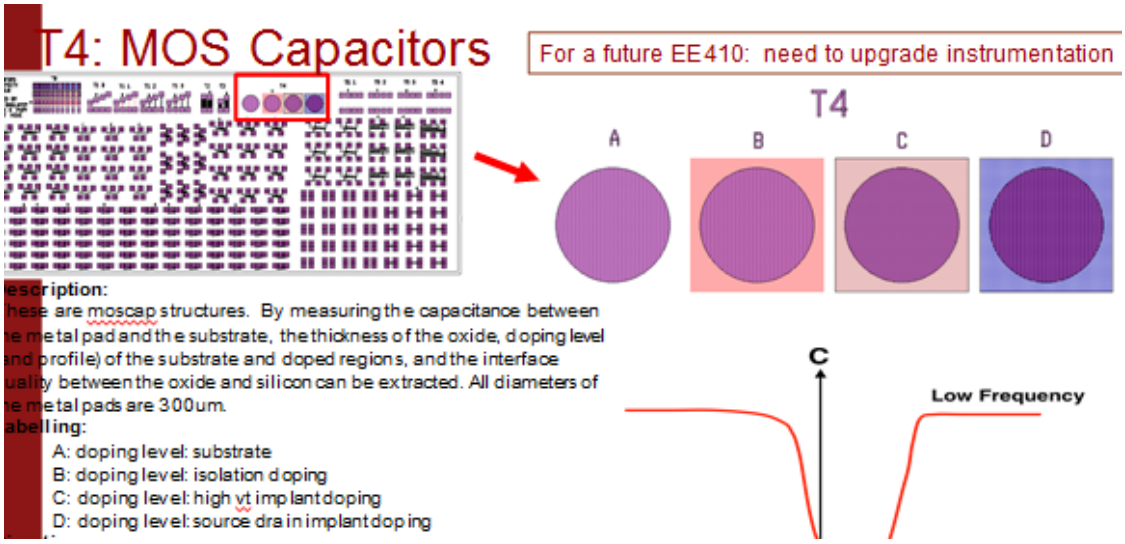


Fig 4: MOS Capacitors in EE410

From the process flow, there are 3 implants available:

(1) S/D implant: Arsenic @2.0E15 cm-2 @ 60 keV,
(2) Isolation P+ implant: Boron @5.0E15 cm-2 @60 keV
(3) High Vt-implant: Boron @1.0E13 cm-2 @ 60 keV.

Choosing the P+ implant in P-substrate to give lowest sheet rho, take the structure "B" as the structure of interest to measure oxide thickness in accumulation. The doping profile, as implanted, is shown in the next page.

Ion Implantation Profile Calculator/Graph

Substrate:	(•) Si ( ) Amorphous Si ( ) SiO_2 ( ) Si_3N_4
Dopant:	( ) Arsenic (•) Boron ( ) Phosphorus
Ion Energy:	60 [keV] (0-200)
Ion Dose:	5.0e15 [ions/cm^2]
Substrate Depth (x):	0.2 [µm]
	Calculate Concentration
Ion Concentration at x:	3.6351466385826265e20 [atoms/cm^3]

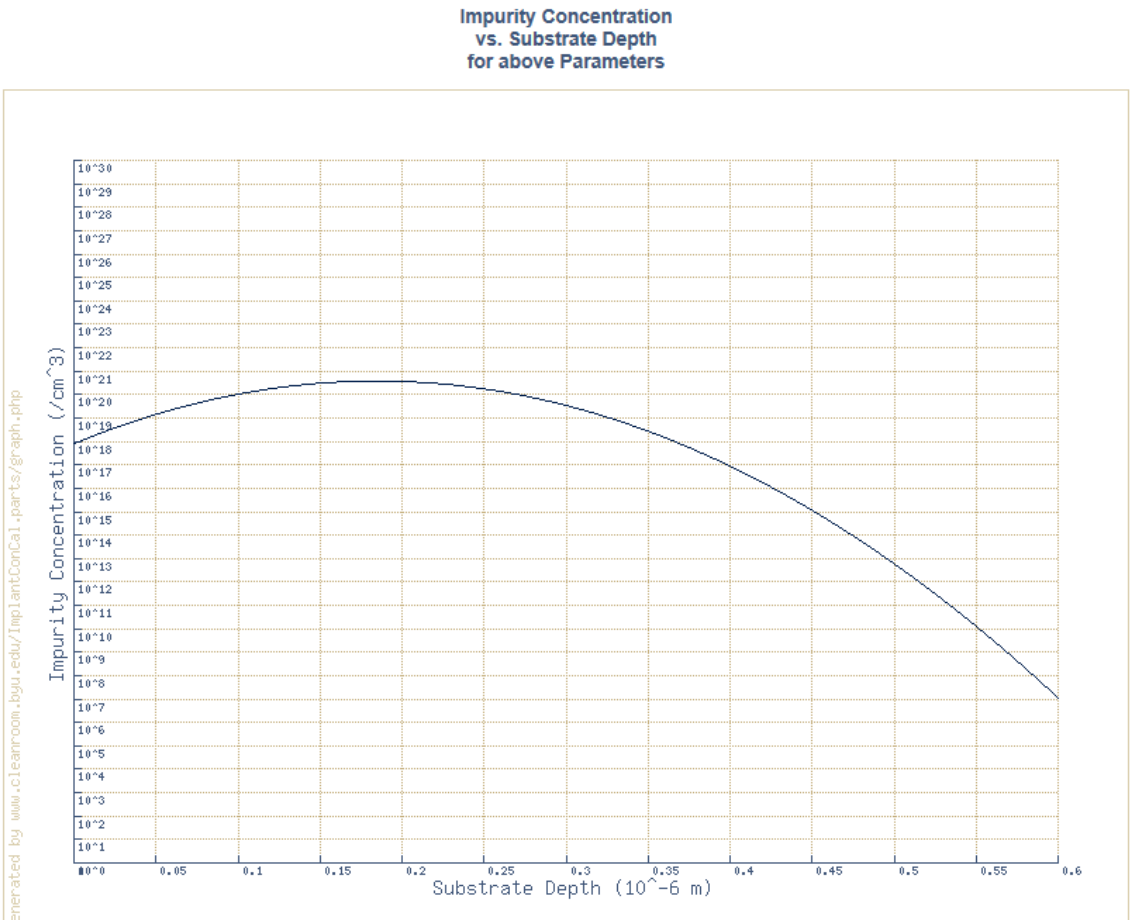
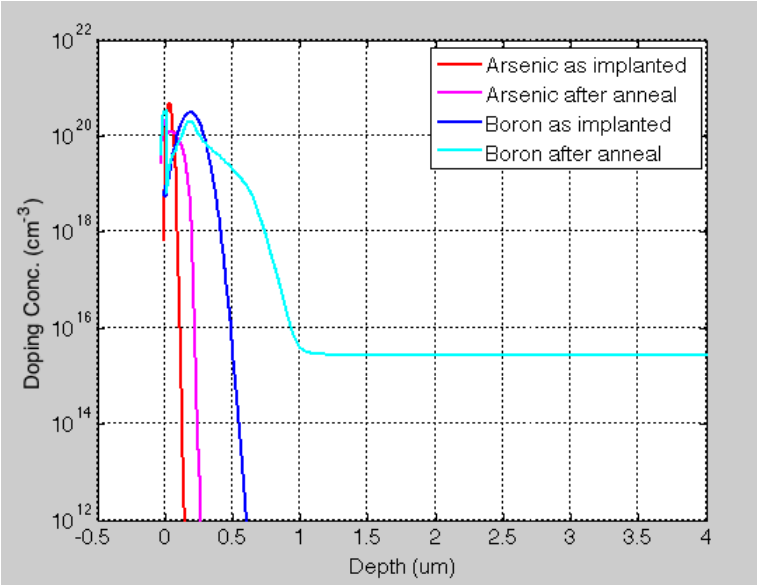


Fig 5 (Top): P+ Doping profile as implanted. [Source: Using on-line profile calculators.]

Fig 6(Bottom): Doping profiles after anneal. Note: Boron as implanted profile (peak and projected range matches closely with Fig 5). [Source: EE410 report.]



Using an average P+ region doping as 1E19/cm3 after anneal, the resistivity of that region will be around 0.01 Ohm-cm, which is orders of magnitude lower than the P-substrate material ground path, which is being used currently.

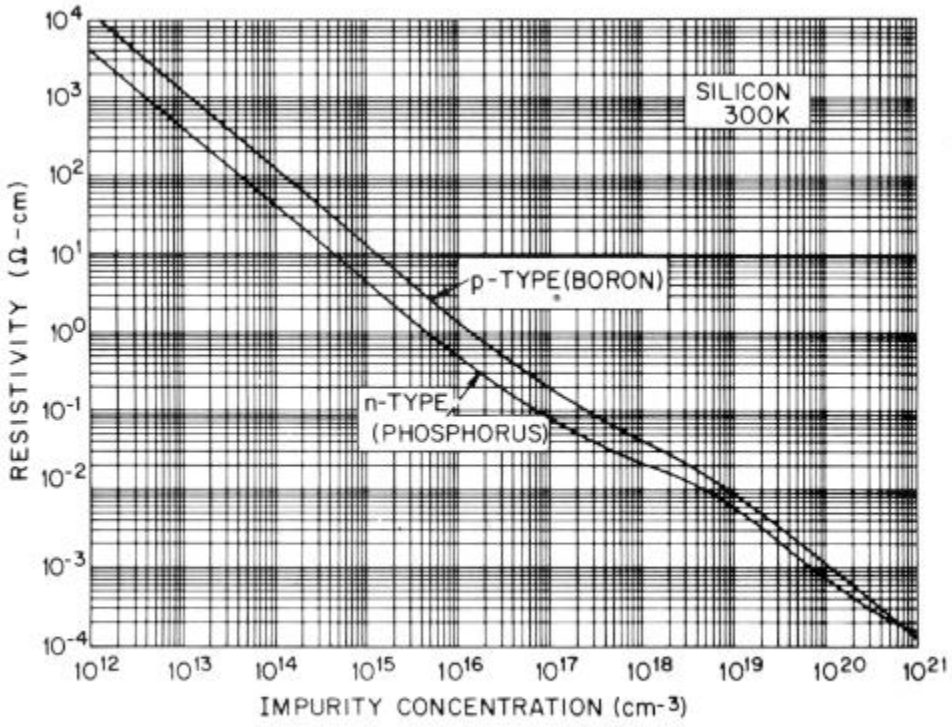
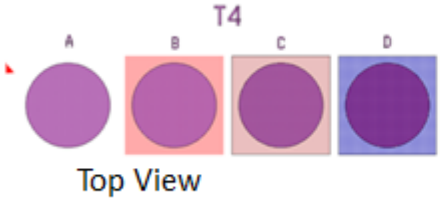
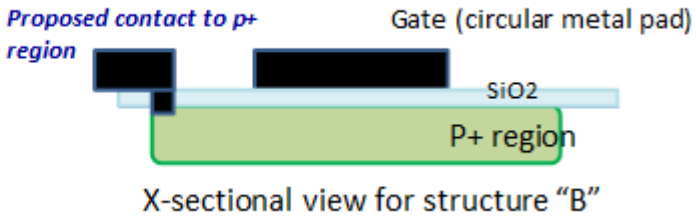


Fig. 21 Resistivity versus impurity concentration for silicon at 300 K. (After Beadle, Plummer, and Tsai, Ref. 38.)

Therefore, the following proposal is made to improve the C-V measurement in EE410 material:





(1) Use the Structure "B" P+ region around the gate metal as the substrate for C-V measurement. It needs a contact mask and a metal mask to connect to a probe pad. This will be possible by a 2-mask revision: (CONT + MET). No additional implant is necessary and the same flow could be maintained.

(2) Contact should be placed a safe distance away from gate in the p+ region (> 10 um), so that quality of gate oxide is not compromised during etch. Since the measurement involves a displacement current, so only a few contacts is required.
(3) Metal pad for p+ pick up needs be safely far away to keep fringing cap a minimum.
(4) Similarly, structures "C" & "D" can have this type of pick up tap for doping level & interface quality measurement. For this we need to plot $1/C^2$ vs Bias Voltage and measure the slope. For Interface quality hysteresis in CV curve (forward & backward sweep) needs be measured.

(4) Conclusion:

The golden wafer measured with the same setup provided comparable thickness value as measured elsewhere and as calculated from capacitance value. This isolates the mismatch of measured versus calculated oxide thickness value of the provided sample to test structure problem. Observation showed the P-substrate tap connection is a significant contributing factor. Proposal for improvement by putting a P+ pick up pad around the dedicated MOS structure is the most convenient. It will require only 2-mask revision, and will be compatible with the NMOS depletion process flow.