Optimization of Silicon Isotropic Plasma Etch in PT-DSE for GOPHER Process

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Abstract

The goal of this project what to optimize an isotropic plasma etch in the PT-DSE, with the particular aim of applying it to the GOPHER process for fabricating photonic microstructures. A recipe was developed using the existing DSE FAT recipe for deep reactive ion etching and previous experience with etch recipe development on the tool to come up with a starting point. Screening tests were run to see what parameters should be explored during the subsequent 2^3 full factorial experiment guided by the JMP software for design of experiments. Due to factors later identified, the experiment did not help to yield an ideal isotropic etch recipe, but the experimental design methodology and lessons learned about choosing appropriate test structures and analysis using a focused ion beam system can hopefully be helpful to labmembers in the future.

Introduction

The GOPHER process (Generation Of PHotonic Elements by RIE) has been developed at Stanford and used primarily in the fabrication of photonic crystal membranes for mirrors and sensors [1]. It allows for the patterning of subsurface structures in silicon, and has been used primarily for the fabrication of suspended photonic crystal membranes from single crystal silicon. The process flow consists of an initial patterning of the silicon surface via anisotropic plasma etch through a hard mask, and subsequent conformal oxide deposition and isotropic plasma etch to create subsurface bubble in the silicon. More detail on the process is shown in figure 1 and an example application can be seen in figure 2. Currently, the process relies on using the Drytek2, a flexible CCP etcher, for the isotropic plasma etch step. I wanted to investigate alternatives to this tool, in particular looking at one of the ICP silicon etchers, as those systems provide independent control over plasma density and substrate bias. The prediction was that this would be an important factor in tuning the etch recipe to achieve an ideal isotropic etch profile that could be modified for other applications. As a starting point, the primary feature of interest for the isotropic etch are submicron holes (~500nm) with an oxide hard mask.

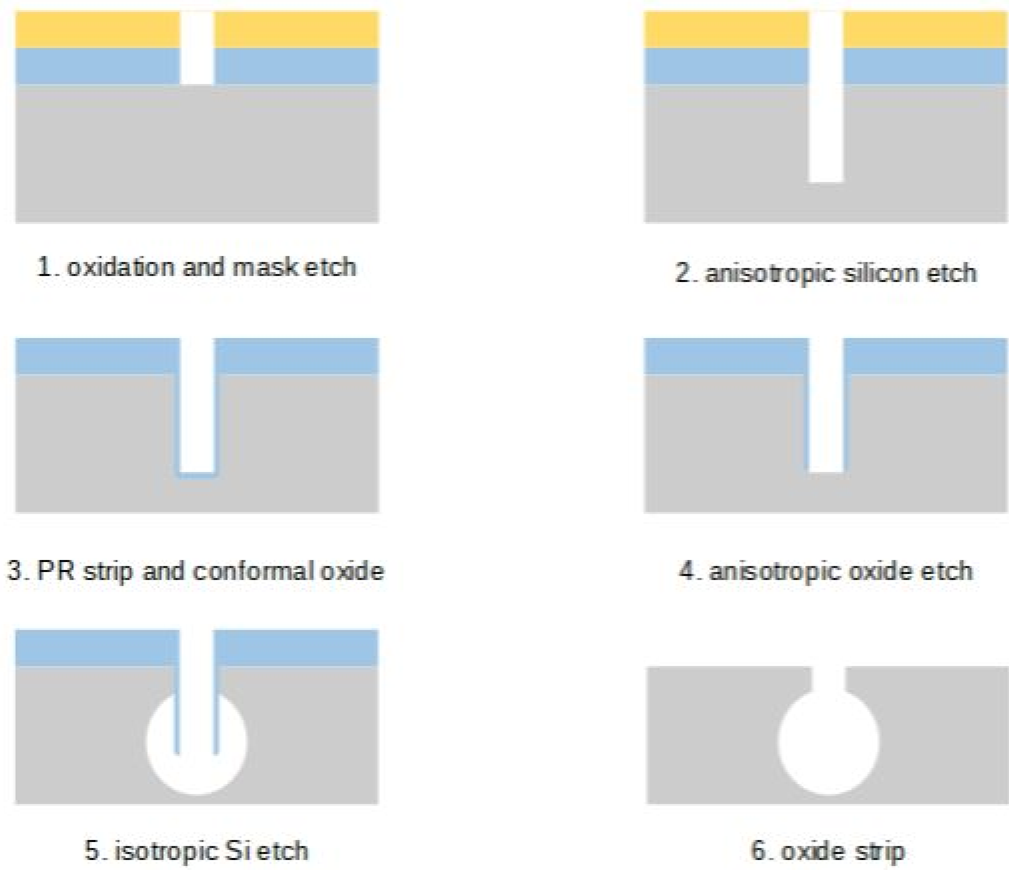

Figure 1: Schematic process flow of the GOPHER process in cross section, demonstrating the ideal etch profile from a circular hole patterned in the oxide layer. yellow = photoresist, blue = oxide, grey = silicon.

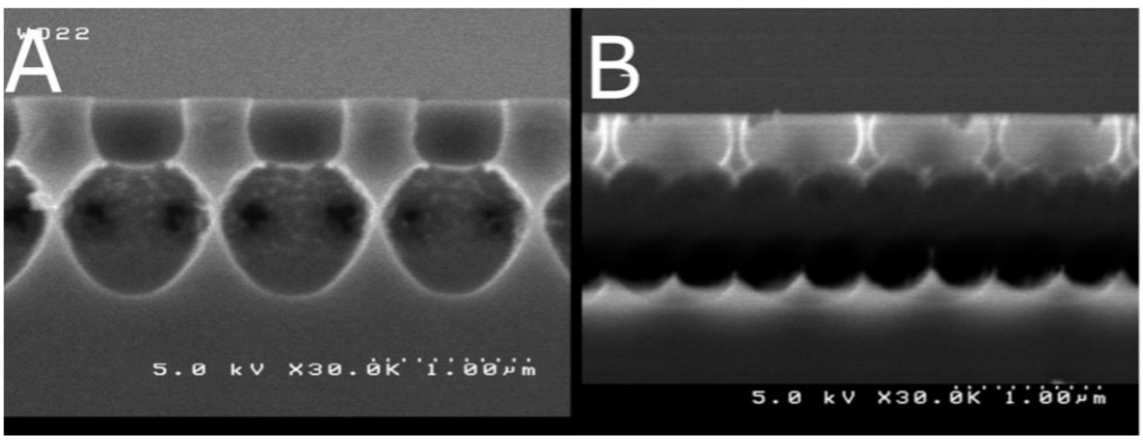

Figure 2: Example of (A) partially released and (B) fully released photonic crystal membranes fabricated in single crystal silicon using the GOPHER process.

The typical isotropic dry etch for silicon consists of an SF_6 plasma, often with additives, that generates fluorine radicals to remove silicon from exposed surfaces. Available options for ICP tools capable of performing the desired etch were the PT-DSE and the Lampoly. The tool with which I worked during this project was the PT-DSE, one of the three PlasmaTherm Versaline ICP etchers in the SNF whose primary application is deep reactive ion etching (DRIE) of silicon, primarily due to the fact that the Lampoly has been characterized as an isotropic etcher in the past.

Methods

Process Flow

Rather than run an entire GOPHER process flow, I decided to simplify the process to do a straightforward characterization of the vertical etch depth vs. the lateral etch undercutting the mask features I had defined, using a structure like that shown in figure 3. The process starts with a thermal oxidation for the mask, which was patterned in the ASML and anisotropically etched to create the test structures. The test wafers from this point were each etched in the PT-DSE using a different recipe. Throughout the project, the main changes to this were the specific mask used for the lithography and the recipe parameters for the etch in the PT-DSE. Appendix A provides more of the tool-specific details for the process flow used during the full factorial experiment described later.

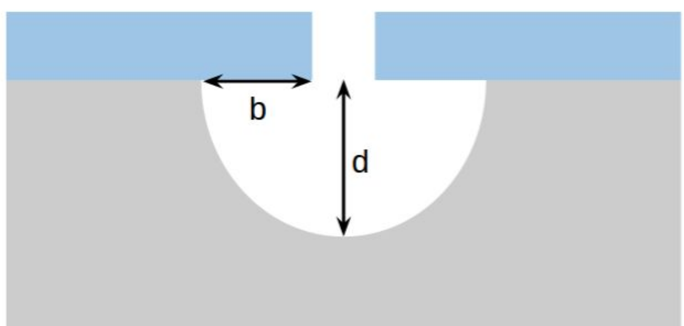

Figure 3: Schematic of the test structure characterized during the project demonstrating the measurements made of the vertical etch depth d and the lateral etch distance b for each etch in the statistical experiment.

Mask Choice

Etch tests often involve several types of generic features of varying size, such as hole arrays, lines and spaces, isolated lines, and isolated caps in the shape of circles, squares or crosses. Depending on the desired application, different tests structures should be considered. I am most interested in the etch profile from isolated holes. I began my testing with old masks for photonic crystals that were made available by labmates, as pictured in figure 4, thinking that I would have enough control over the etch rate to prevent the overlap of neighboring etch pockets. This proved too difficult without reducing the etch time to mere seconds, and the result was almost always an etch such as that shown in figure 5.

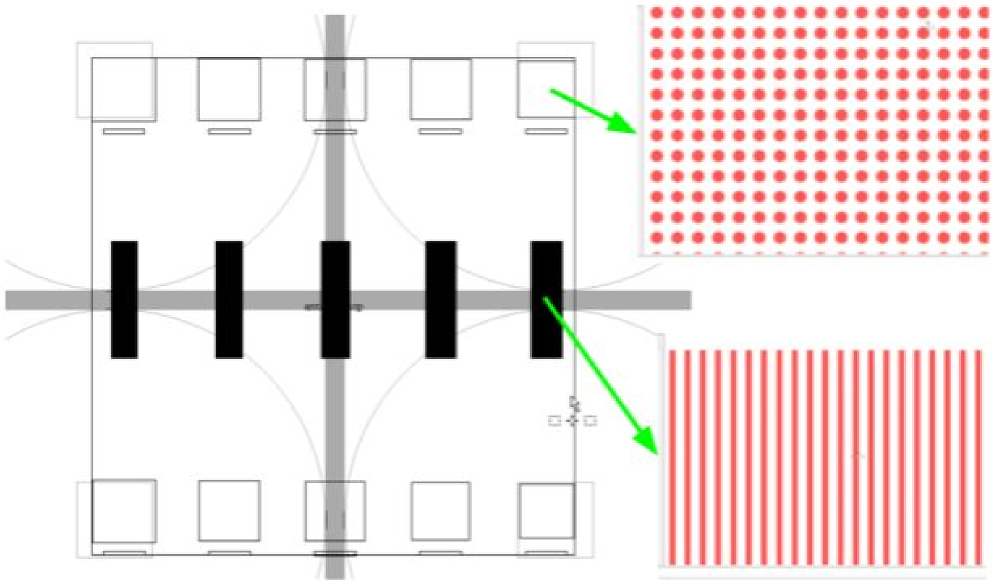

Figure 4:Initial mask design consisting of 3 types of patterns. On the top is a set of photonic crystal array 0.5mm x 0.5mm as shown in the top blowup, in the middle a set of gratings as in the bottom blowup, and on the bottom a set of photonic crystals as in the first set, but with engineered defects. From left to right the pitch increases from 900nm to 1100nm, but hole diameter (640nm) and line width (400nm) do not change.

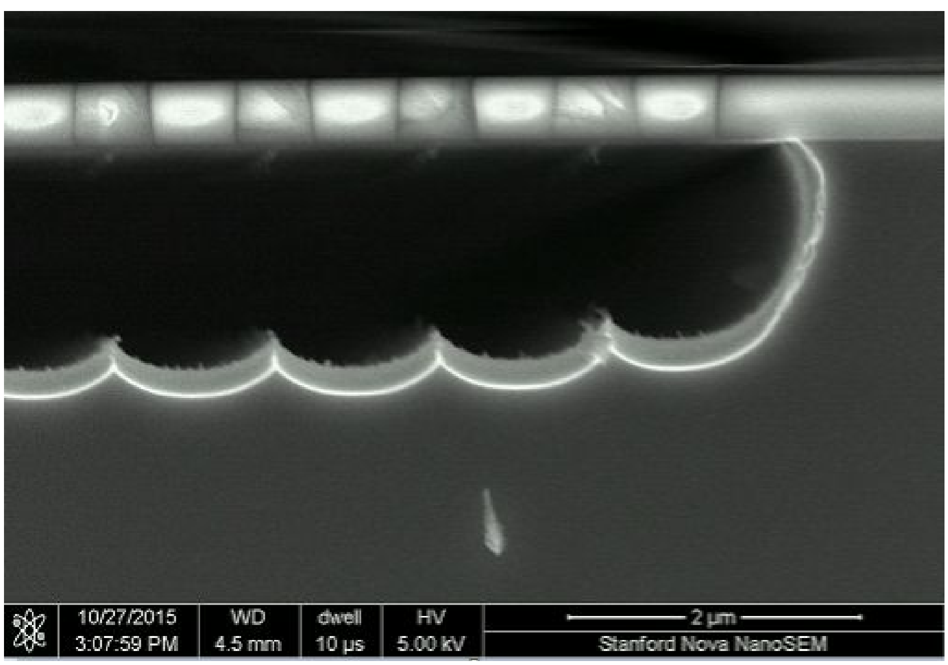

Figure 5: Example etch using the photonic crystal structure on the original mask used, showing pockets that completely overlap and destroy the etch rate information.

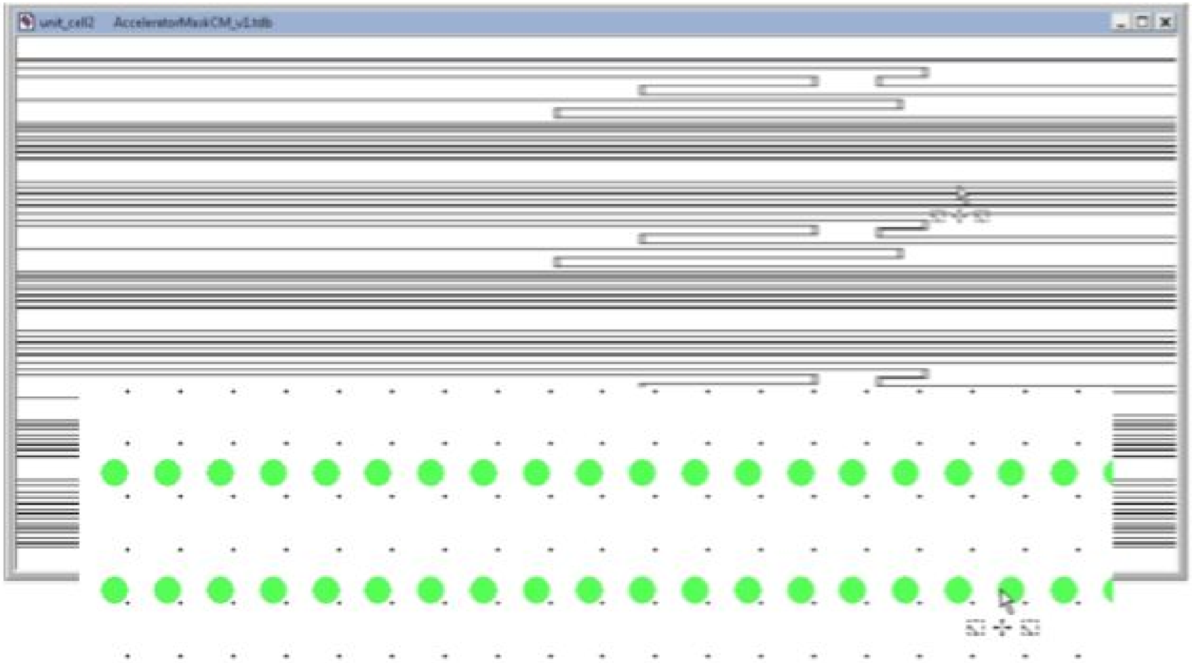

Figure 6: Final mask design used in this project for etch characterization. The holes are 500nm in diameter and the pitch in the horizontal dimension is 1µm. The center-center separation in the vertical direction is greater than 2µm, which allowed for greater etch distances than the former test structure.

It became necessary to use a much sparser features, and so the mask shown in figure 6 was used for the remainder of the testing in this project. It was chosen mainly because it was readily available. The larger separation in one dimension allowed for recipes with higher etch rate to be tested without destroying information, but as discussed later the etches still seemed limited to a regime where the etch was not ideally isotropic.

Process Development

The process development began with taking the standard DRIE recipe in the PT-DSE, which consists of a polymer deposition step, a high bias etch step, and a low bias etch step, and keeping only the latter. The low bias step was further adjusted to a bias setting within tens of volts of the lower limit of the tool, down from well over 100V. A series of screening test was performed where various parameters of interest were adjusted to determine which most strongly affected the resulting etch rates of interest. Through experience with optimizing DRIE recipes on the tool during a previous instance of EE 412 and published process trends for DRIE profile (such as those in [2]), I thought to look at chamber pressure, electrode bias, electrode temperature, etch gas flow, and ICP power. I determined that the first three were the most interesting parameters in terms of their effect on the etch rate and profile and used the JMP statistical software package to design a 2^3 full factorial experiment to investigate their effects. Unfortunately as mentioned, the regime in which I decided to operate was one of considerably low etch rates in order to accommodate the close packing of the holes in my test pattern. I was shown in the end that this operating in this regime does not allow us to achieve an ideal etch profile.

Characterization

The structures used for evaluation of the etch process posed some initial challenges for the characterization. The relative sparsity of structures on the wafer made it difficult to cleave the samples such that there were useful features on the edge of the cleaved chip. The suggestion was made to instead use a FIB, a dual beam system with an electron beam for imaging and an ion beam for selective milling and deposition of material. The advantage of this type of tool is that a top-down SEM imaging mode can be used to find a feature anywhere on the surface of the wafer or chip, and then material can be selectively milled away to expose a cross section of features below the surface. There are two FIB systems available in the Stanford Nano Shared Facilities. Additionally, ion beam induced deposition of conductive and insulating layers is also available for micromachining, or as explained below, to aid in imaging. The first is the DB235 in the McCullough building and the second is the Helios in Spilker, the tool primarily used in this project due to its wider range of option and better imaging and milling capabilities.

Discussion

Results

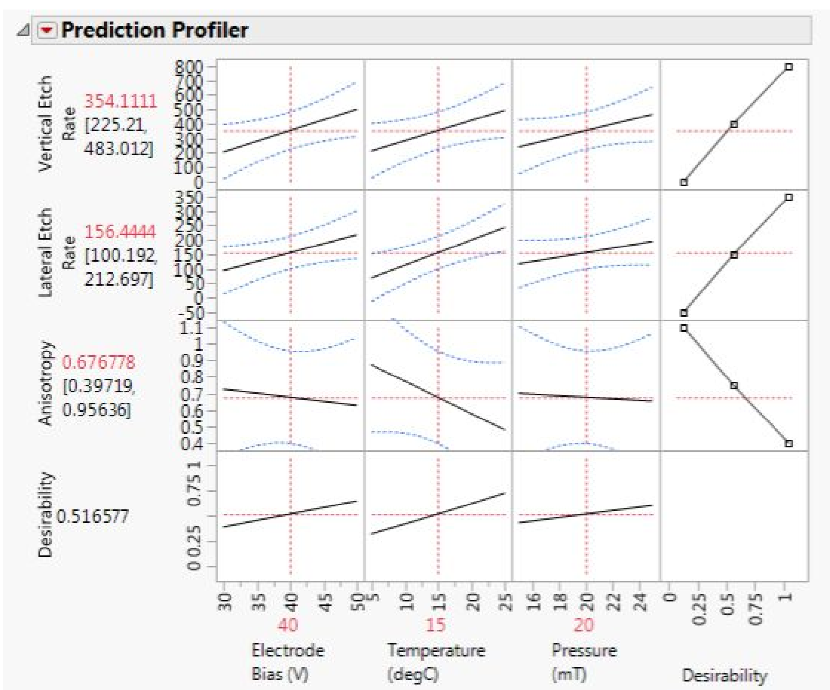

Figure 7: Prediction curves and desirability profiles for the statistical model attempting to explain the effects of the chosen parameters on the lateral etch depth, the vertical etch depth, and the anisotropy, a value given by A_F = 1-b/d [3].

The plots in figure 7 summarize the results of the final experiment. The electrode bias and temperature influence most strongly the etch rates, with p-values of p=0.044 and p=0.025, respectively.The pressure also explains some of the variation in the outputs, with p=0.072, as we had expected. However, an interesting interaction seems to be statistically relevant as well, that between the electrode bias and temperature, with p=0.071. The trends associated with the prediction curves for the temperature and pressure agree with what was expected going into the experiment, but the trend for the electrode bias is the opposite. It was believed that higher bias would lead to more directional ions and therefore to a more directional etch. Since this is not what was observed, the new hypothesis is that the etch in the regime explore is strongly affected by transport of reactive species through the submicron hole of the test structures. It also leads to the prediction that the somewhat statistically significant interaction noted earlier is related to this limitation. That is to say, the higher the pressure in the chamber, the more reactive species there are and the less bias is needed to drive a given amount of reactive species into our structures. Though the model predict that an interaction may be present, it does not tell us what effect the interaction is actually having, so we would have to design a new experiment to investigate the phenomenon further.

Next Steps

Limitations in our parameter space stemmed not from any limitations of the tool, but from the non-ideal choice of test mask. The arrays of closely spaced hole in both test patterns were chosen for the ability to cleave the wafer through them and have something to look at on the exposed edges. With the flexibility afforded by the decision to use the FIB for imaging, it was possible to change the test structure to a much sparser feature on the wafer without making it impossible to characterize. Unfortunately, I was entrenched in the design choices already made and stuck with them to the end of the project. In order to better complete the task of finding an optimal recipe for this project, it will be necessary to design a mask with custom test structures well suited to the target application, rerun the screening tests, and redesign the factorial experiment, taking into account the expanded parameter space.

Conclusion

In this project an optimization of a new isotropic etch recipe in the PT-DSE was attempted. The result was not a complete success, but lessons learned can guide a future attempt. Experience in experimental design and characterization should be able to help labmembers with similar optimization problems in the future

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References

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Appendices

Appendix A - Detailed Process Flow

1. wbclean: sc1 -> HF -> sc2
2. thermco1-3: 1-3WETOX, 1050degC, 1hr (500nm target)
3. yes oven
4. svgcoat2: 5 0.7um w/VP 2mm EBR
5. asml: mask-specific exposure from 100-250mJ/cm^2
6. svgdev 9321
7. amtetcher: recipe 3, 20min
8. gasonics 016
9. pt-dse: recipe varies
10. Helios FIB

Appendix B - Notes on FIB Cross Sections

A typical cross sectioning workflow is one of the more basic applications of the FIB, but here it is important to explain a few details of the process for those unfamiliar with it. First, due to natural spread of the ion beam, milling away a cross section will cause some (potentially) undesirable damage to exposed edges and can obfuscate information about the original edge profile, as in figure []a. To address this issue the surface can be prepared by depositing a thin layer of platinum, which will help to preserve the sample edge and also prevent charging of photoresist and insulating mask layers. This is depicted in figure []b. The platinum can also provide some contrast to aid in imaging. Another important thing to note is that the angle between the electron and ion beam axes is 52° and that the sample surface is normal to the ion beam during deposition, milling, and subsequent imaging. Thus, one must be aware of this when analysing cross sections to ensure that the appropriate geometric correction be applied when recording length measurements. Specifically in this case, we can use horizontal measurements without correction, but measurements in the vertical direction should be divided by the sine of the angle between the beams.

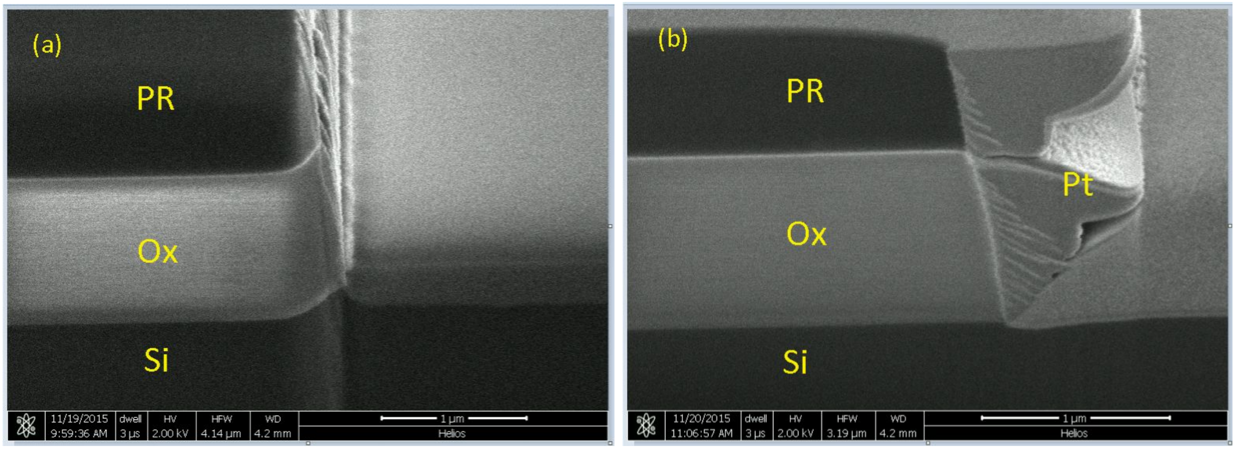

Figure [8]: Examples of FIB cross section of exposed edges of a silicon dioxide (Ox) feature etched on a silicon (Si) wafer with the photoresist (PR) mask still in place: (a) without and (b) with a platinum (Pt) layer deposited beforehand. The vertical edge is visibly rounded in (a) and due to significant differences in milling rates the exposed region of Si is milled more dramatically than that under the Ox/PR stack.

Appendix C - Experimental Run Details

	Pattern	Electrode Bias (V)	(degC)	Pressure (mT)
1	−+−	30	25	15
2	−++	30	25	25
3	+−+	50	5	25
4	000	40	15	20
5	++−	50	25	15
6	−−+	30	5	25
7	+++	50	25	25
8	+−−	50	5	15
9	−−−	30	5	15

Figure [9]: Parameter values for the 9 runs of the 2^3 full factorial experiment with a center point.