

Optimization of Isotropic Plasma Etch in PT-DSE for GOPHER Process

EE 412 Final Presentation

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Outline

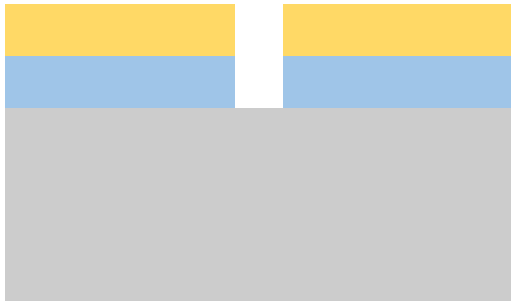
- Motivation
- Background
- Methods
- Results
- Conclusion

Introduction to GOPHER process

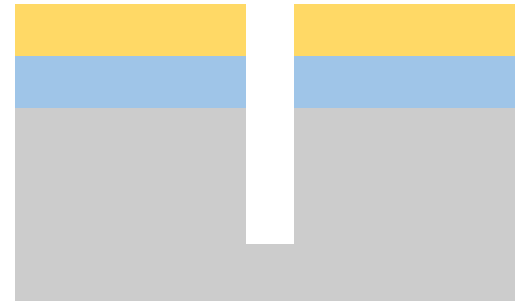
GOPHER:

- Generation Of PHotonic Elements by RIE
 - anisotropic etch → conformal deposition → clear bottom → isotropic etch → clear mask
- fabrication of photonic crystal membranes from single-crystal silicon
- investigate alternative to standard Drytek2

GOPHER Process Flow I



1. oxidation and mask etch



2. anisotropic silicon etch

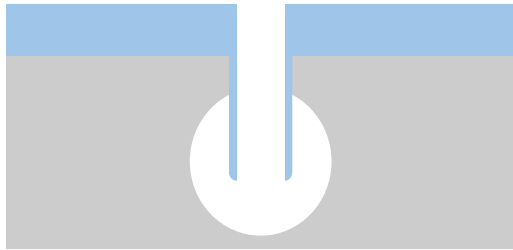


3. PR strip and conformal oxide

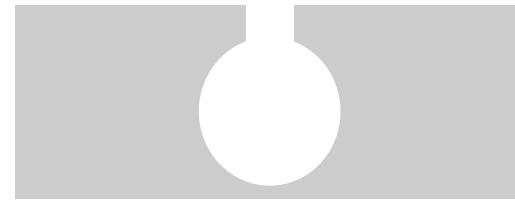


4. anisotropic oxide etch

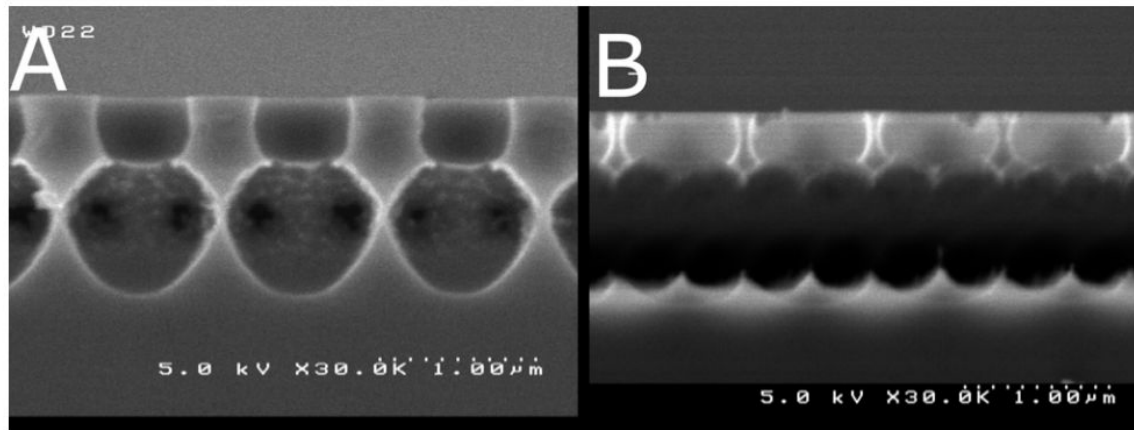
GOPHER Process Flow II



5. isotropic Si etch



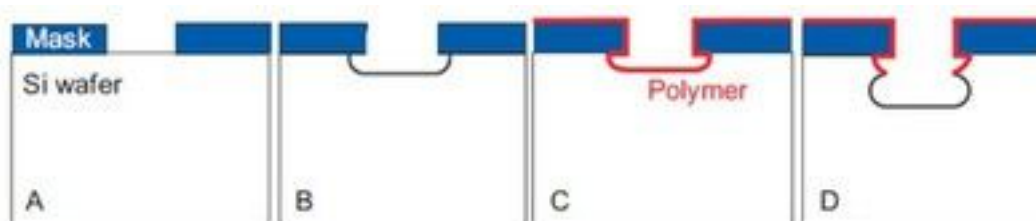
6. oxide strip



Hadzialic et al. (2010)

PT-DSE Introduction

- fast gas switching, high ICP power and gas flow capabilities
- very capable DRIE tool



Time Division Multiplex Etch Process

A Silicon wafer with patterned mask
B First etching cycle

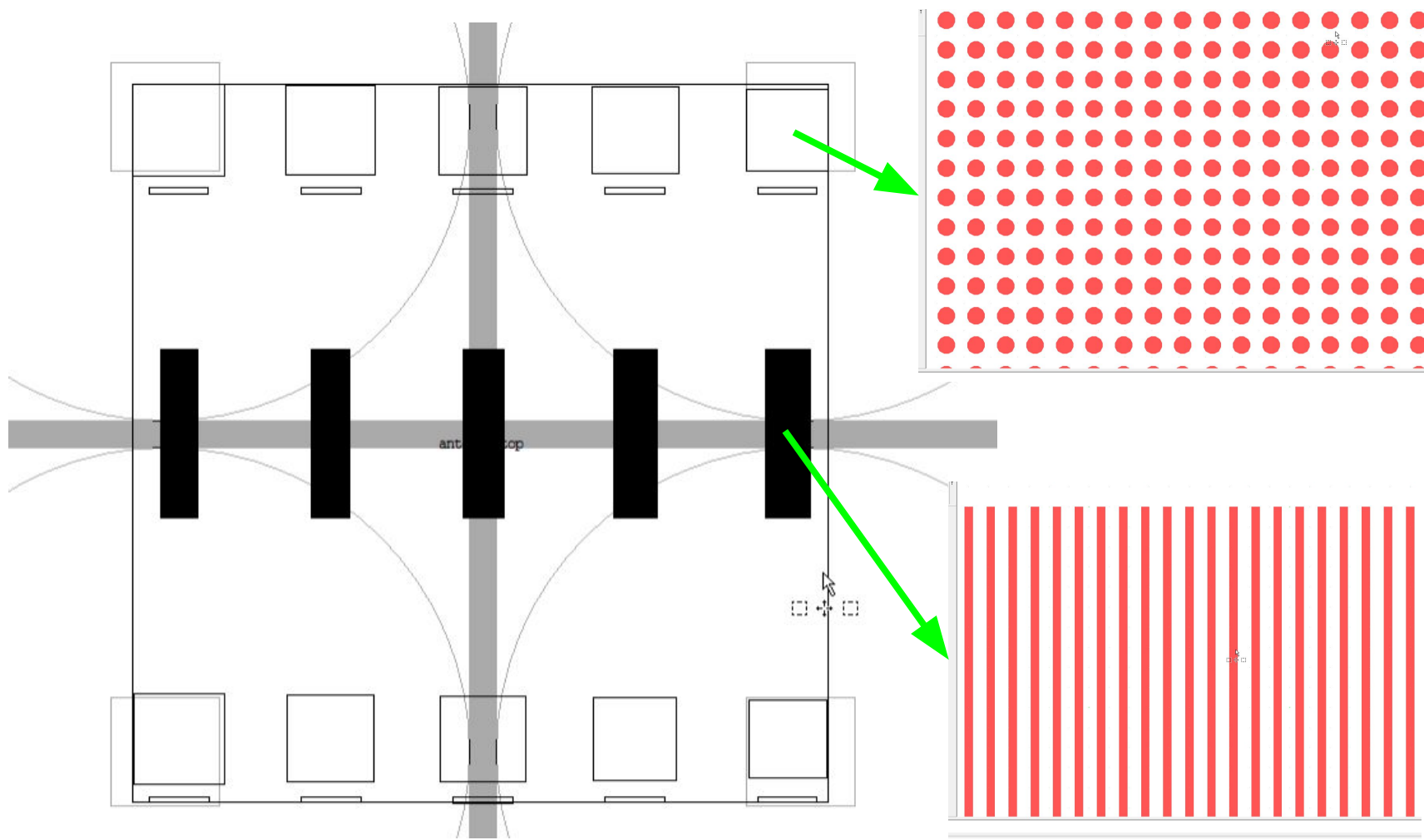
C Passivation cycle
D Second etching cycle



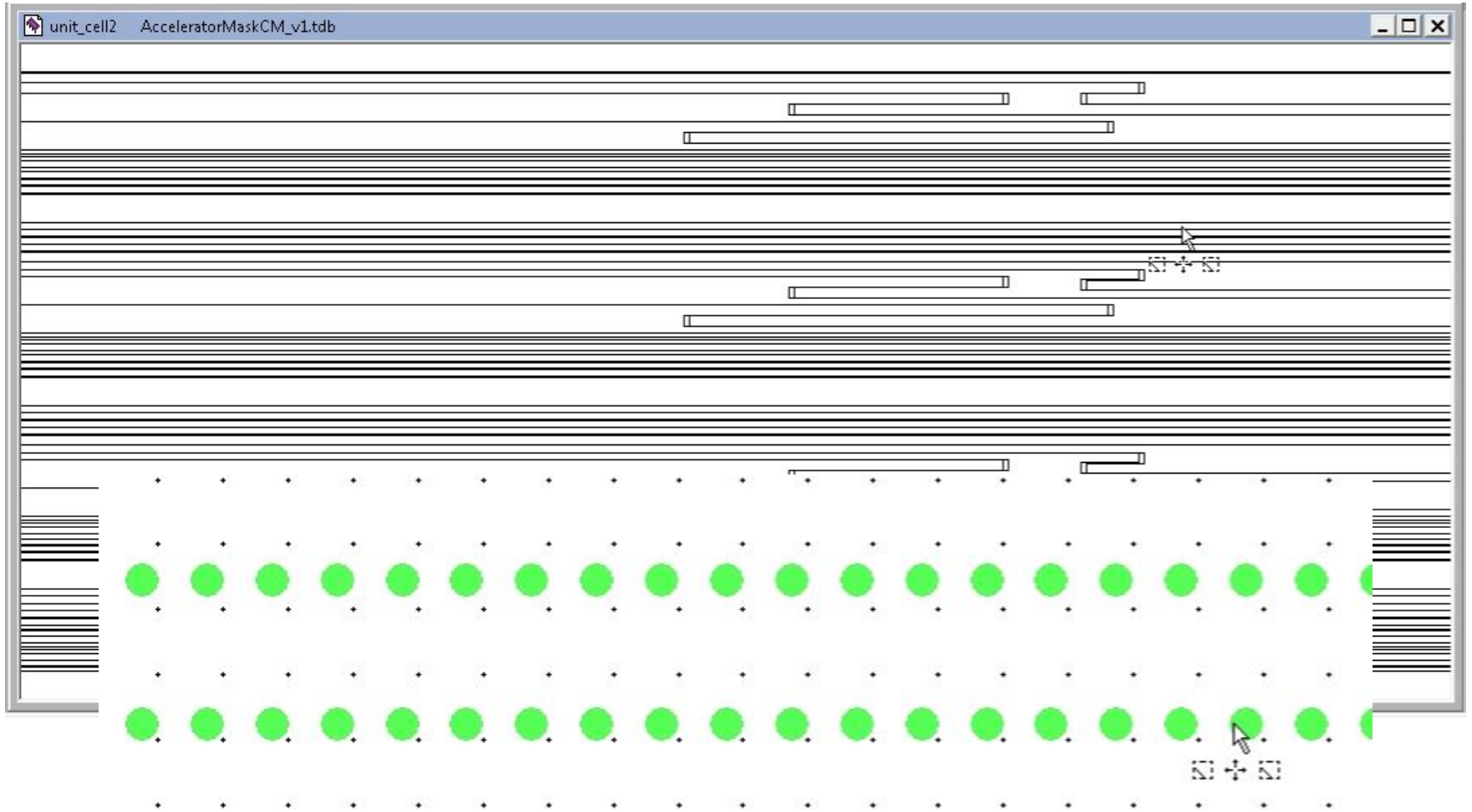
Experimental Process Flow

- thermal oxidation
- litho - asml
- oxide etch - amtetcher
- strip resist/polymer - gasonics
- measure mask film thickness - nanospec
- isotropic etches
- FIB measurements an final mask thickness

Test Structure I



Test Structure II



Experimental Plan I

- Baseline recipe based on EtB from DSE FAT
 - ❑ only other steps: GS, LT, PWD - no cycling
 - ❑ electrode bias reduced
 - ❑ other parameters selected based on experience with DRIE process optimization

Experimental Plan II

Table1. Summary of process trends.

Trends for Controlling process results	Etch rate	Profile (↑ negative) (↓ positive)	Selectivity	Grass	Breakdown	Sidewall Roughness
Etch gas increase	↑↑	↑↑	↑	↓	↑	↑
Dep gas increase	↓↔	↔	↑	↑	↓↔	↓
Etch:Dep time ratio increase	↑	↑	↑↔	↓	↑↔	↑
Pressure increase	↑↑	↑	↑	↓↔	↑	↑
Dep Coil Power increase	↓↔	↓↔	↑↔	↑	↓↔	↓
Etch Coil Power increase	↑	↑	↑	↓	↑	↑
Platen Power increase	↑↔	↑↔	↓	↓	↔	↔
EM1 value (e) increase	↓↔	↓↔	↑	↑↔	↓↔	↔
EM1 delay (e) increase	↑↔	↑↔	↓	↓↔	↑↔	↔

E=etch

↔ no effect or negligible effect

↑ increase

↓ decrease

(J.W. Jeong)

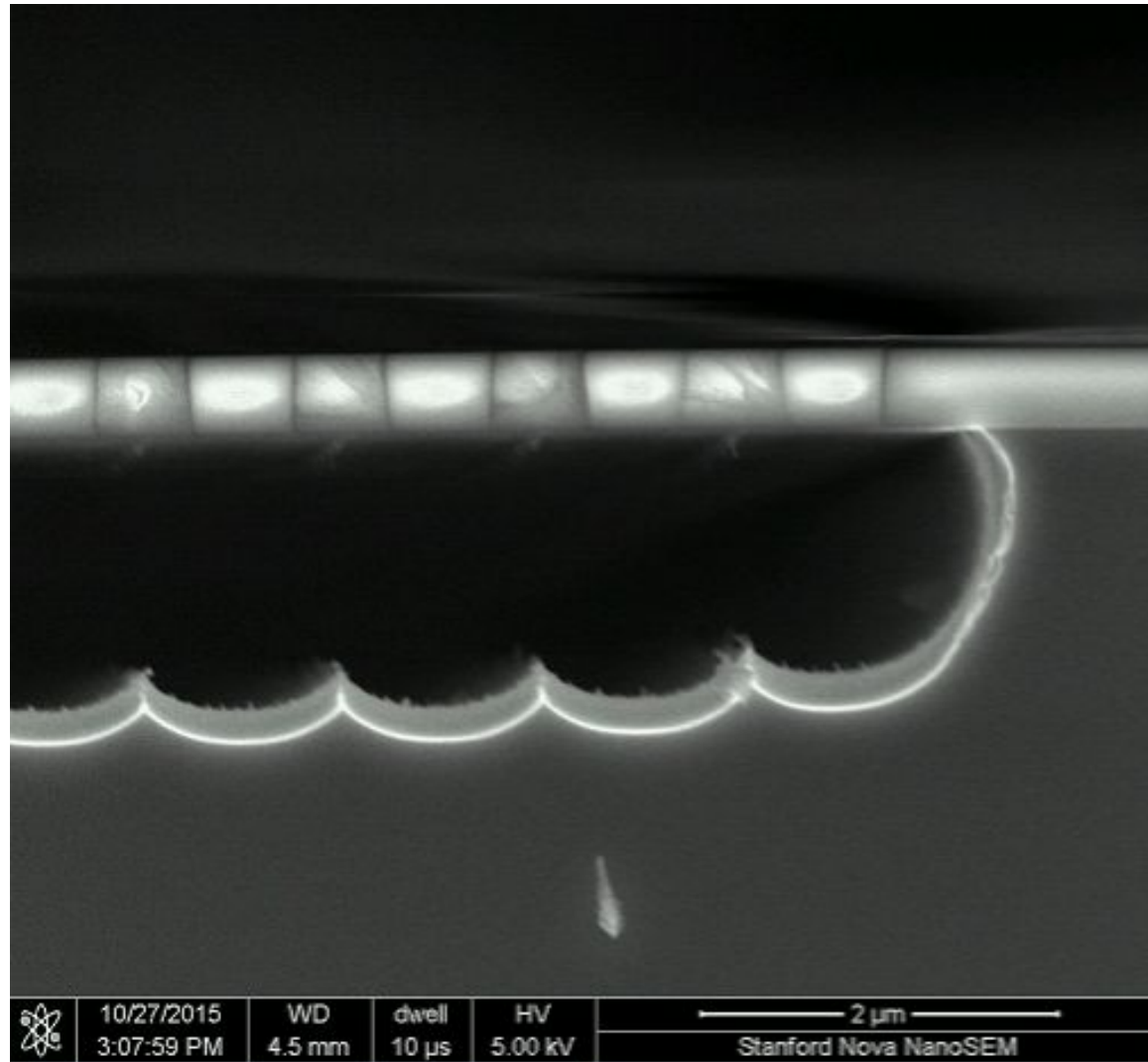
Experimental Plan III

- 2^3 full factorial DOE: ~9 wafers
- process variables
 - ❑ electrode bias (30-50 V)
 - ❑ pressure (15-25 mTorr)
 - ❑ electrode temperature (5-25 °C)
- measurements via FIB, optical film measure
 - ❑ vertical (d) and lateral (b) etch rates
 - ❑ anisotropy (calculated as $A_F = 1 - b/d$)
 - ❑ mask selectivity - TBD

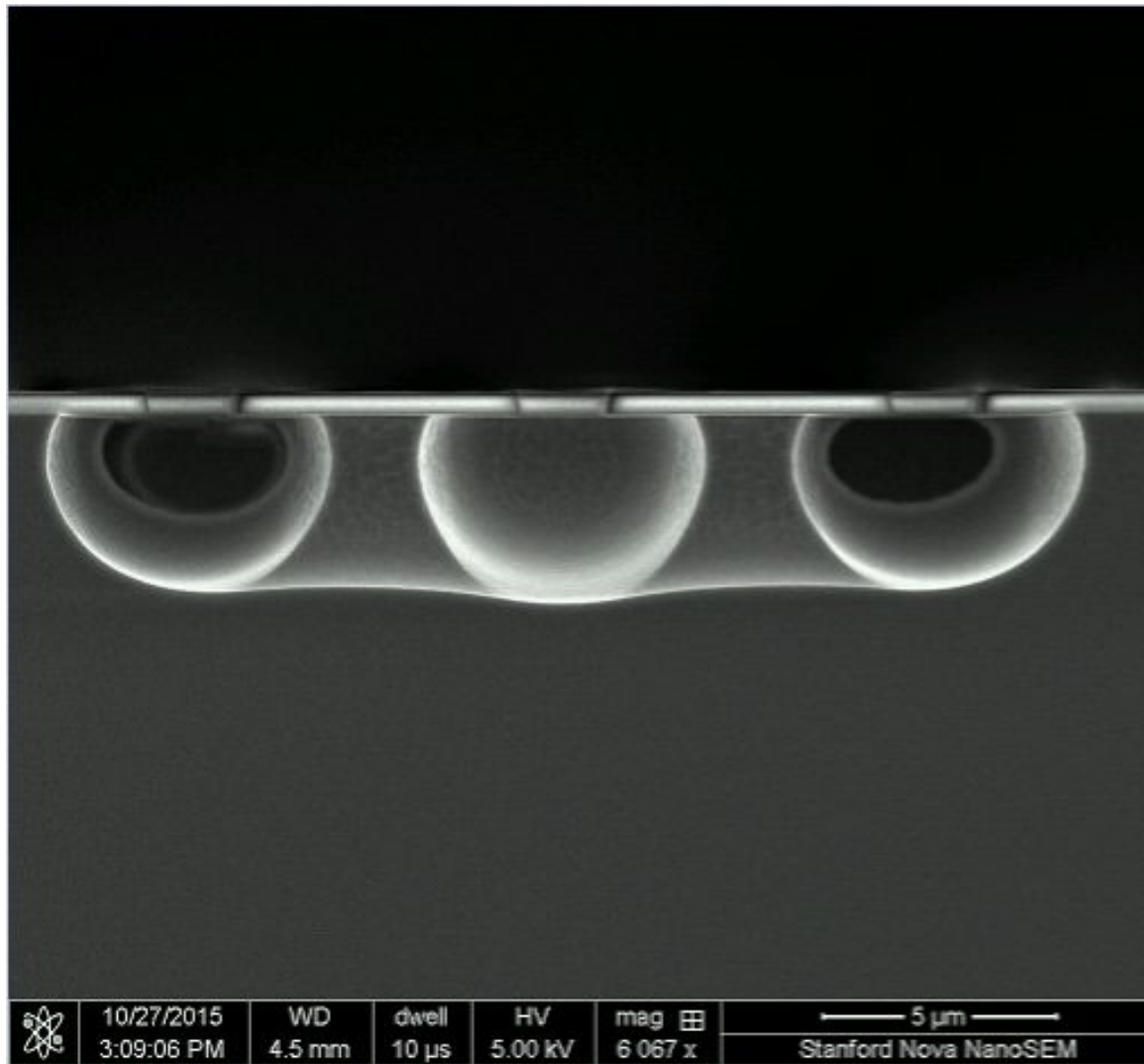
Experimental Plan IV

	Pattern	Electrode Bias (V)	(degC)	Pressure (mT)
1	--+	30	25	15
2	-++	30	25	25
3	+--	50	5	25
4	000	40	15	20
5	++-	50	25	15
6	---	30	5	25
7	+++	50	25	25
8	+-+	50	5	15
9	---	30	5	15

First Etch Example I



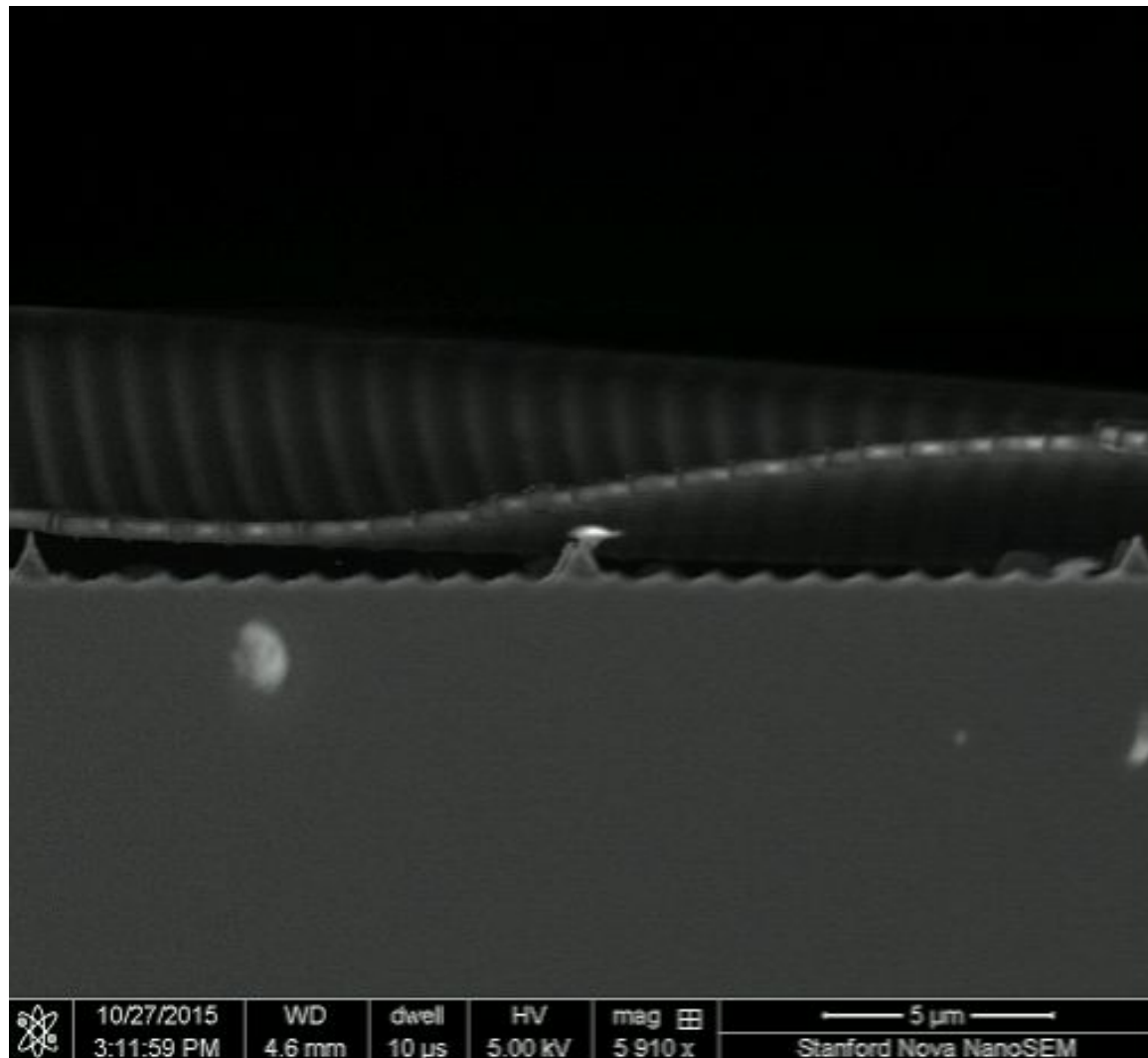
First Etch Example II



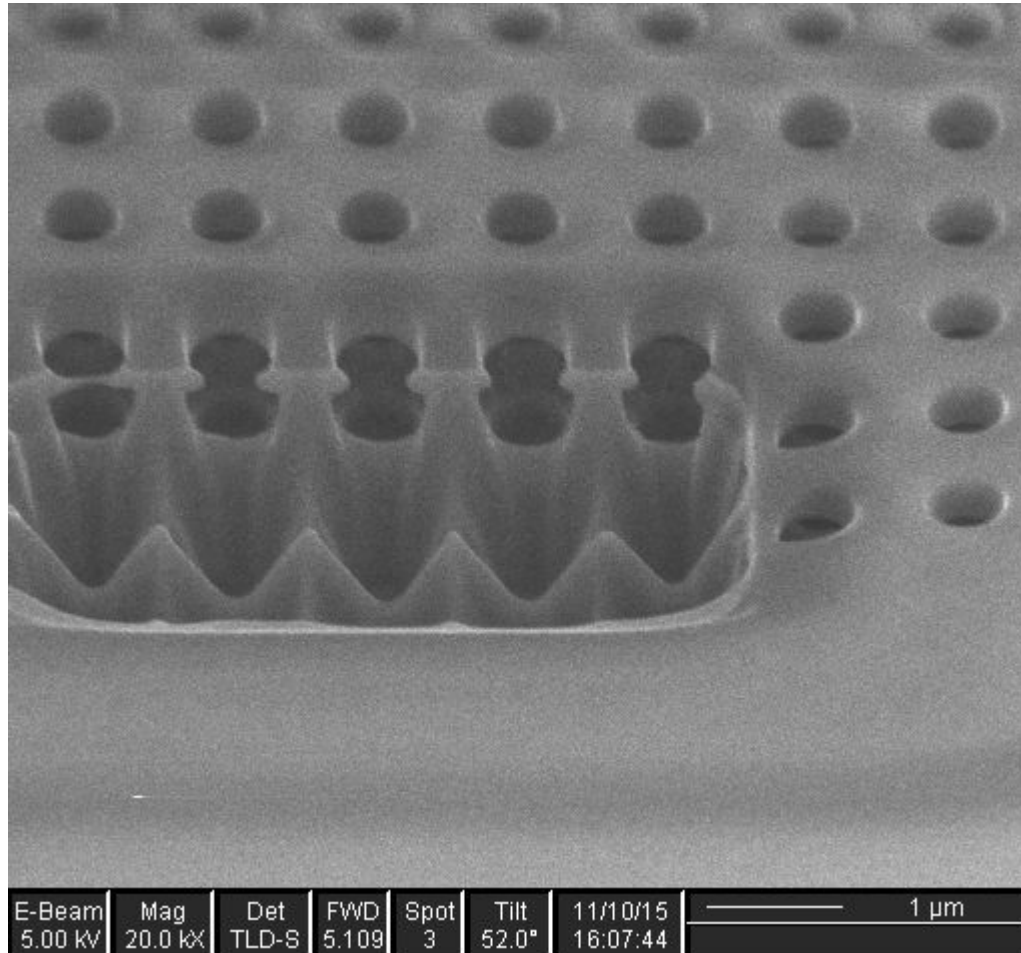
First Etch Example III



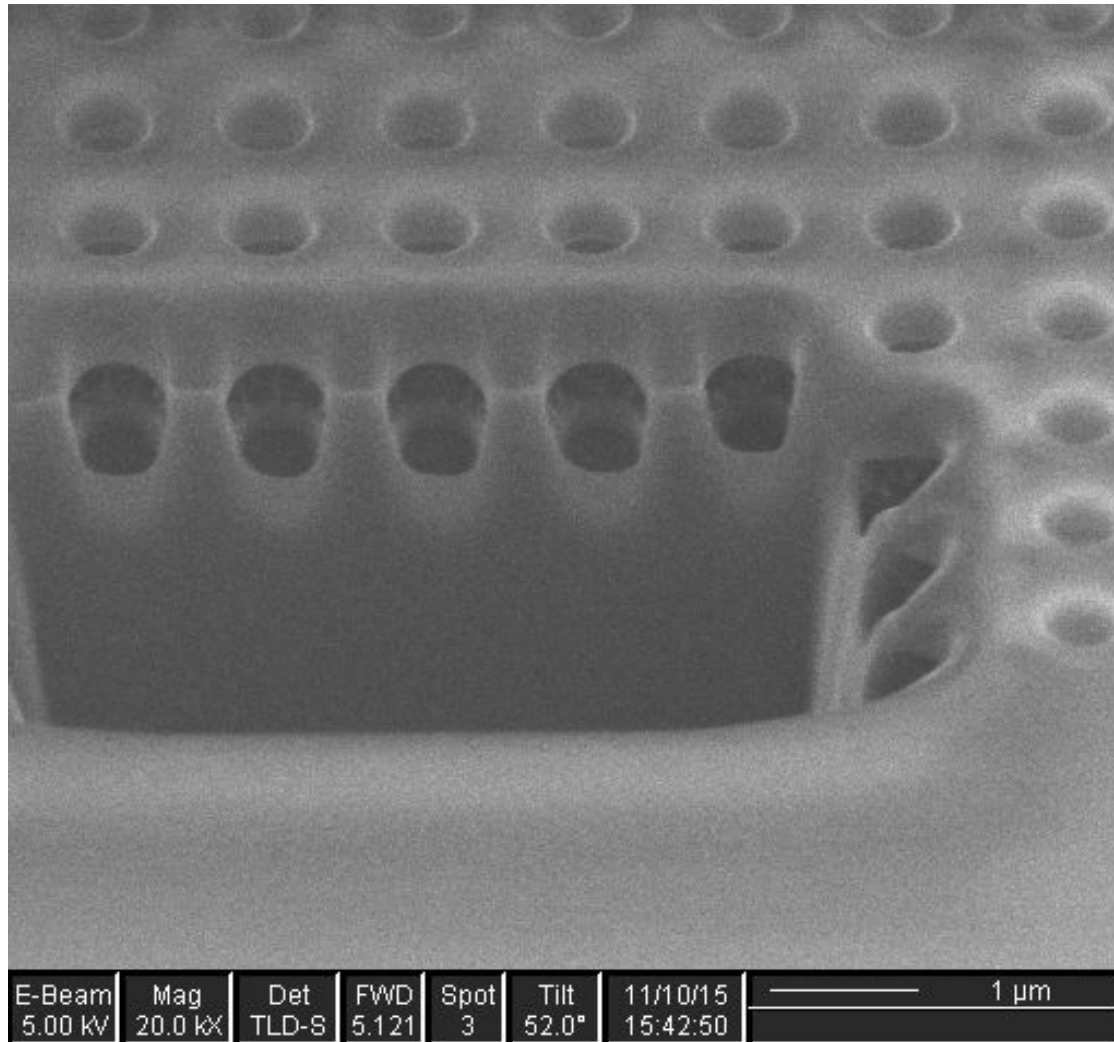
First Etch Example IV



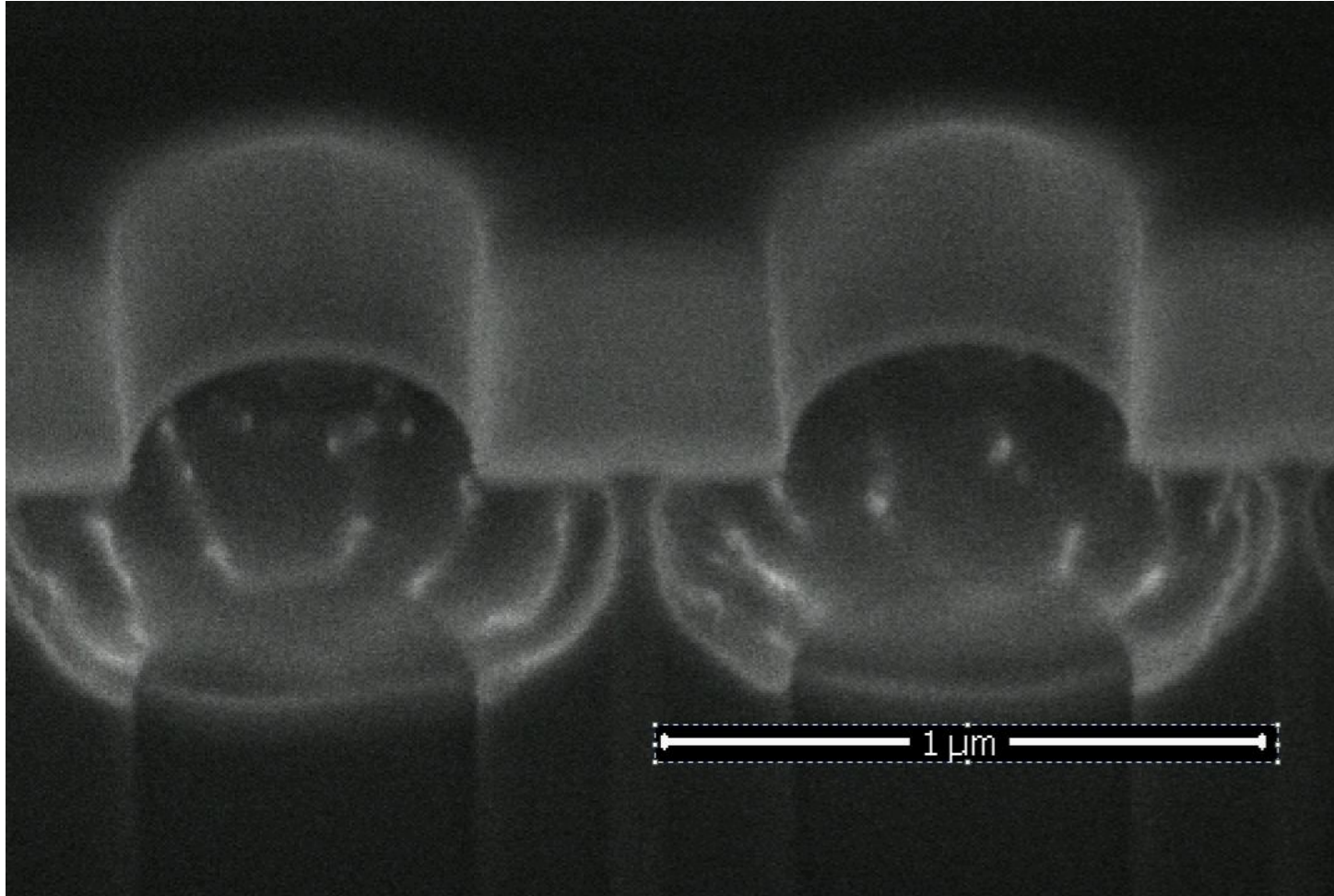
Screen Etch - electrode T (DB235)



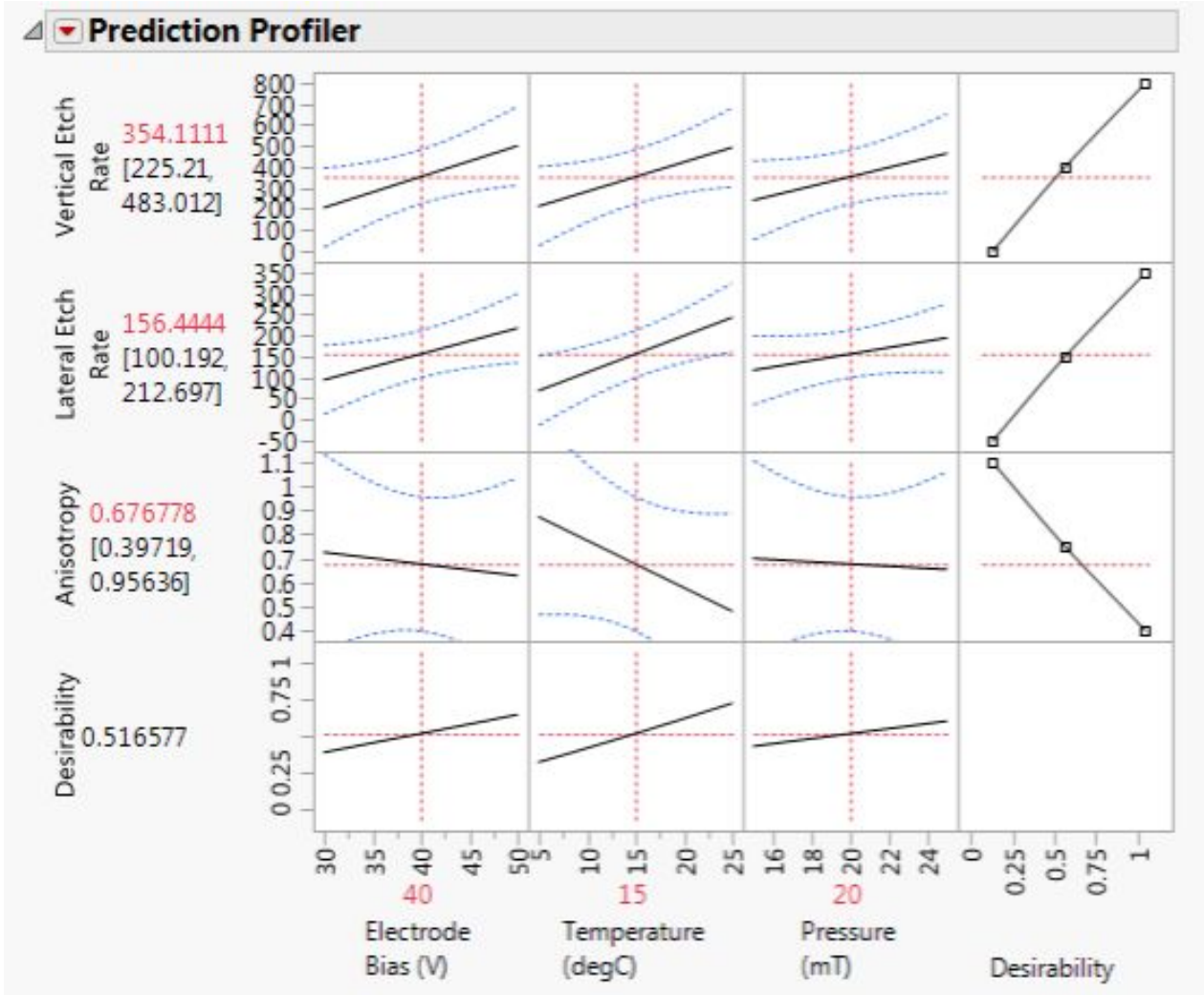
Screen Etch - pressure (DB235)



Screen Etch - pressure (Helios)



Least Squares Model - All Response



Least Squares Model - All Response

Least Squares Fit

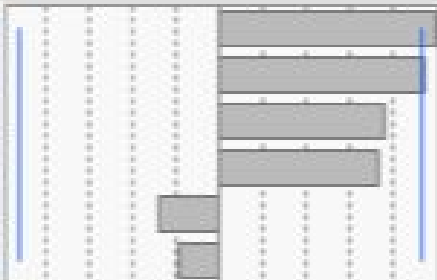
Effect Summary

Source	LogWorth	PValue
Temperature (degC)(5,25)	1.611	0.02448
Electrode Bias (V)(30,50)	1.359	0.04376
Electrode Bias (V)*Pressure (mT)	1.149	0.07095
Pressure (mT)(15,25)	1.141	0.07235 ^
Temperature (degC)*Pressure (mT)	0.793	0.16090
Electrode Bias (V)*Temperature (degC)	0.332	0.46610

Least Squares Model - Vertical

Sorted Parameter Estimates

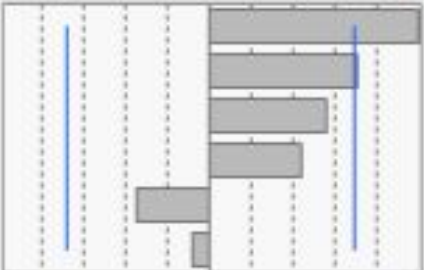
Term	Estimate	Std Error	t Ratio	Prob> t
Electrode Bias (V)(30,50)	146.875	31.77572	4.62	0.0438*
Temperature (degC)(5,25)	139.875	31.77572	4.40	0.0479*
Pressure (mT)(15,25)	111.625	31.77572	3.51	0.0723
Electrode Bias (V)*Pressure (mT)	108.875	31.77572	3.43	0.0756
Temperature (degC)*Pressure (mT)	-41.625	31.77572	-1.31	0.3205
Electrode Bias (V)*Temperature (degC)	-28.375	31.77572	-0.89	0.4661



Least Squares Model - Lateral

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob> t
Temperature (degC)(5,25)	87	13.86705	6.27	0.0245*
Electrode Bias (V)(30,50)	61.5	13.86705	4.43	0.0473*
Electrode Bias (V)*Pressure (mT)	49.25	13.86705	3.55	0.0709
Pressure (mT)(15,25)	38.5	13.86705	2.78	0.1089
Temperature (degC)*Pressure (mT)	-30.25	13.86705	-2.18	0.1609
Electrode Bias (V)*Temperature (degC)	-7.25	13.86705	-0.52	0.6532



Next Steps

- design new mask with custom structures
- rerun similar full factorial DOE utilizing an extended parameter space
- hopefully, Helios electron beam imaging issues will be addressed in the near future

Conclusion

- Sought to characterize a new option for isotropic plasma etching of silicon
- Etch profiles strongly affected by temperature, significant effect of bias
- However, more work necessary to achieve desired etch profile → better test structures!

Acknowledgements - Thank You!

- Usha and Elmer for advice, tool upkeep
- Prof. Howe, Mary, other mentors, and fellow classmates for additional tips and guidance

References

- Sanja Hadzialic, S. Kim, A. S. Sudbø, and O. Solgaard, “Two-Dimensional Photonic Crystals Fabricated in Monolithic Single-Crystal Silicon,” IEEE PHOTONICS TECHNOLOGY LETTERS, VOL. 22, NO. 2, JAN 15, 2010
- Jeong, Jae-Woong, “High Aspect Ratio Si Etching in STS2,” EE412 Fall ‘10 Final Reports, snf.stanford.edu/SNF/processes/ee412/fall-10/final-reports/EE412_STS2-HAR_Final_Report.pdf/view
- Plummer J., “Etching - Chapter 10,” EE212 lecture notes
- SNF Wiki, snf.stanford.edu/SNF/equipment/dry-etching/plasmatherms/plasmatherm-deep-silicon-etcher/equipment-description-and-operating-instructions-for-plasma-therm-deep-silicon-etcher-pt-dse