Stanford Nanofabrication Facility

ALD Process for Top-Gating 2D Materials

ENGR241 Autumn

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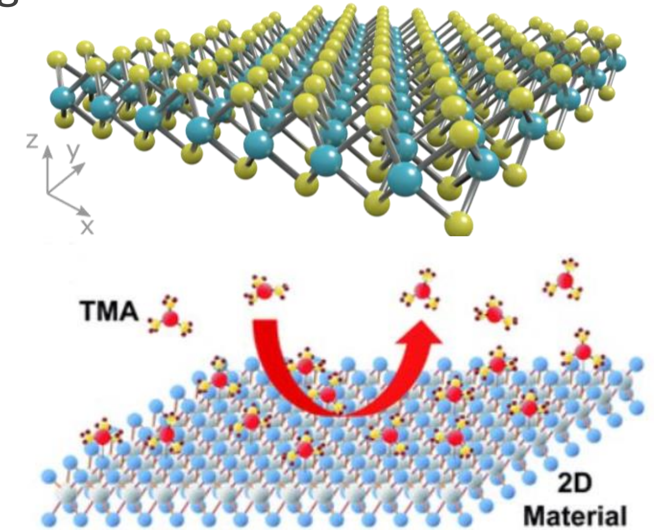
Introduction

- Uniform and full coverage of high-k gate dielectrics is essential for top-gated 2D devices
- ALD is difficult due to lack of dangling bonds
- No recipe exists in SNF for depositing high-k on 2D
  - Only alumina has been tried from ALD tool in Pop lab (not in SNF)
  - Seed layer thickness must be optimized
  - Film quality has not been characterized



- Goal: Develop process flow for ALD top-gating on 2D for reliable and controlled growth of high-k materials
- CVD-grown monolayer MoS_2 on SiO_2/Si samples will be provided from Pop group

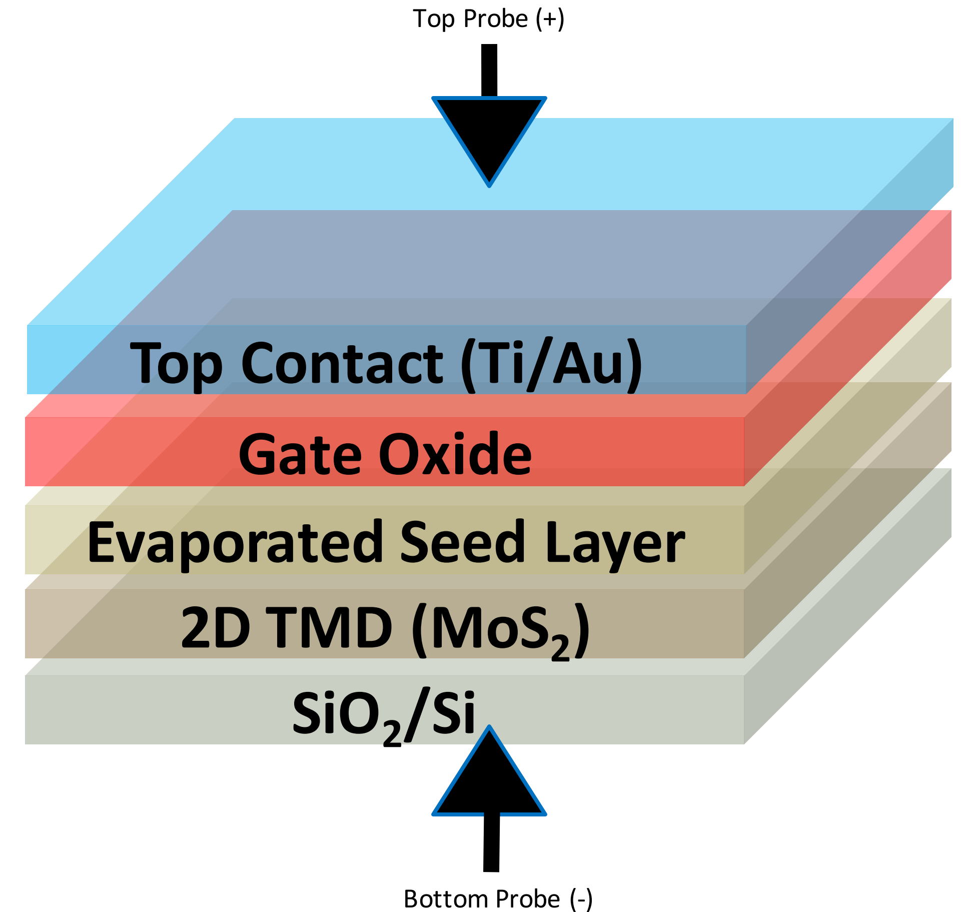
Benefit to SNF

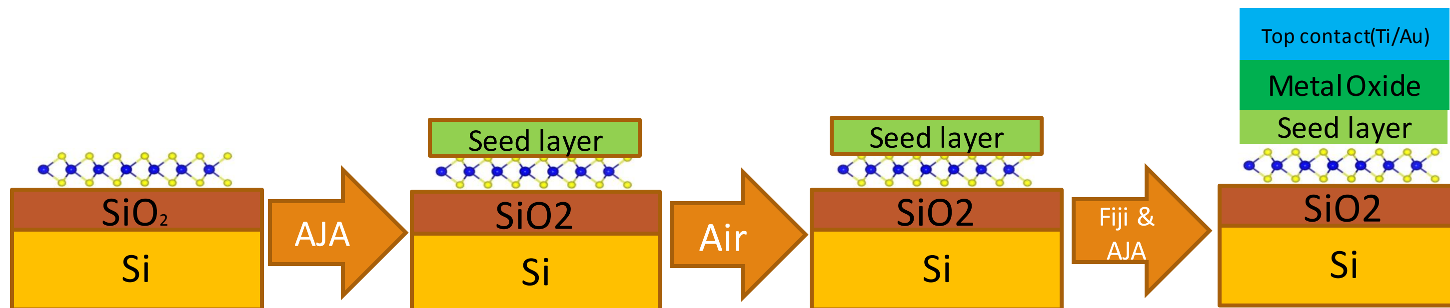
- Process flow for top gating on 2D materials
- Characterization (electrical, surface image) with
  - Different seed layer thickness
  - Different seed layer material
- Recipe for ALD on 2D materials and samples with seed layer

→**All available with tools in SNF!** (but 2D material samples were provided from Pop Group in EE)

Structure and Process Flow

1. E-beam evaporate (AJA) Al
   - On prepared MoS2 for surface characterization
   - On SiO2/Si substrate for electrical characterization
2. Oxidize in air → becomes alumina
3. ALD (Fiji2) alumina on oxidized seed layer
4. E-beam evaporate Ti(5nm)/Au(20nm) for top electrode



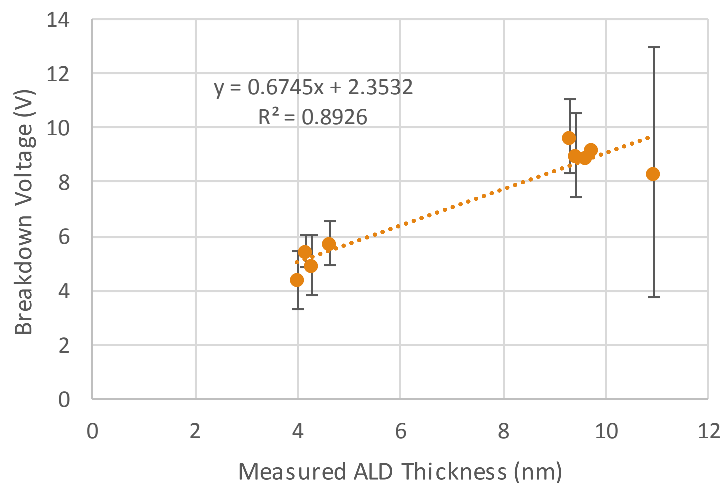


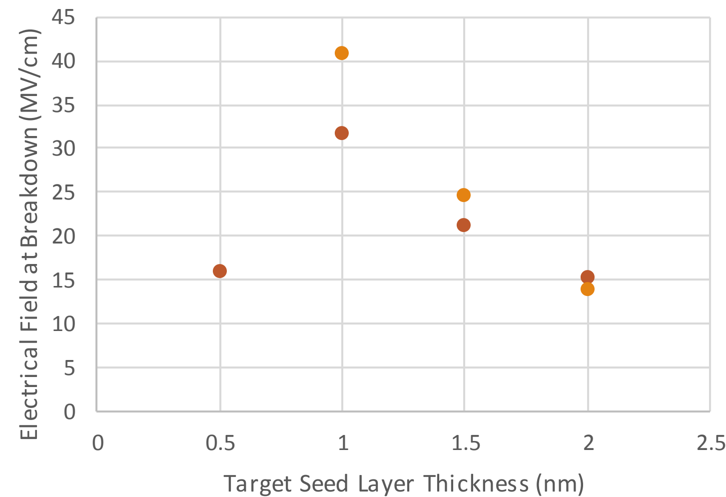
Electrical Characterization

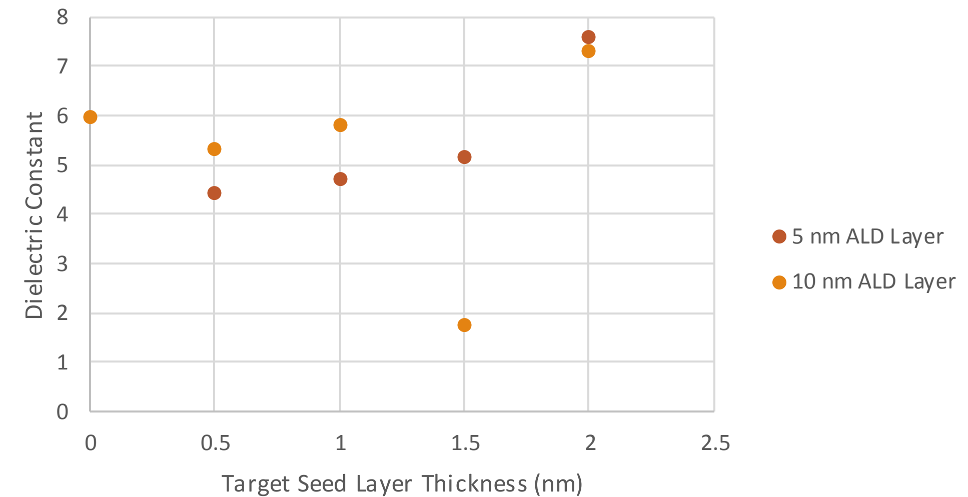
Electric field at breakdown seems to decrease with larger target seed layer thicknesses

Dielectric constant increases with larger seed layer thicknesses

Need more data to verify and reduce error bars: also will test with hafnia







Surface Characterization

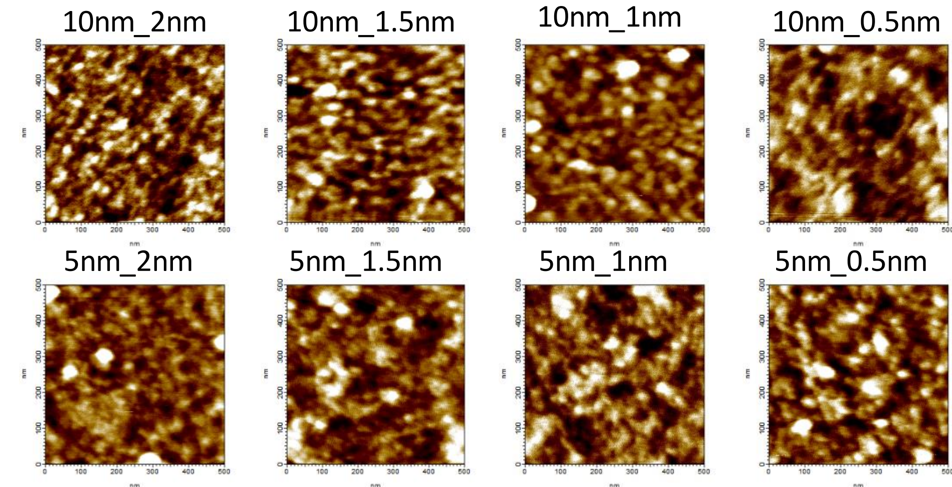
Prepared MoS_2 sample: RMS ~0.197nm

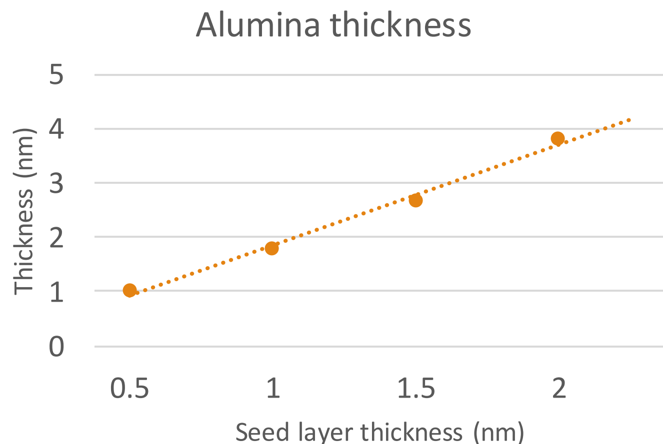
RMS of ALD w/o seed layer

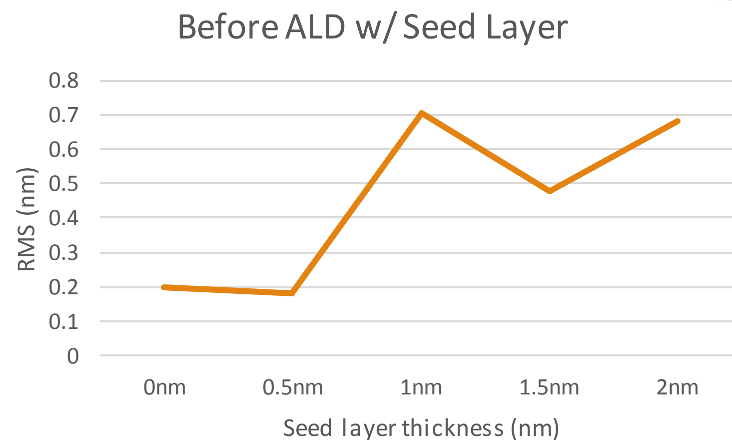
- ALD alumina 5nm ~1.036nm, 10nm ~0.914nm

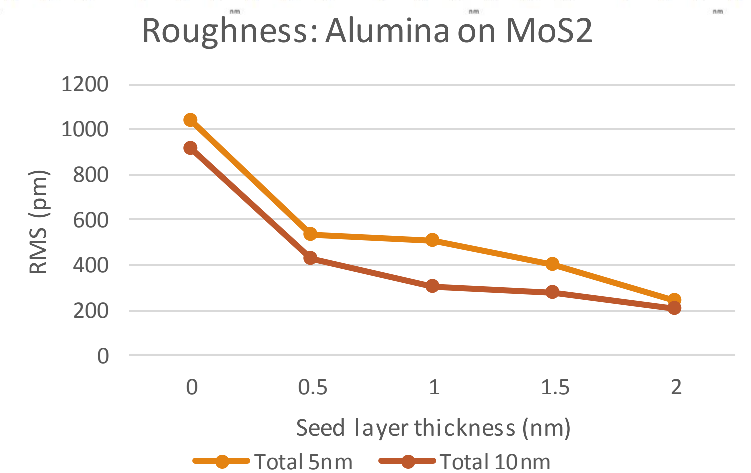
Thicker seed layer before ALD → Rougher surface

Thicker seed layer after ALD → Smoother surface









Conclusion

ELECTRICAL CHARACTERIZATION

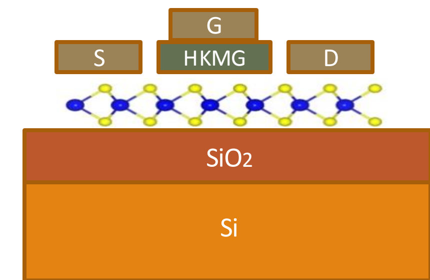
1. On Si substrate, with MIM structures…
2. Electric field at breakdown seems to decrease with larger target seed layer thicknesses
3. Dielectric constant increases with larger seed layer thicknesses

SURFACE CHARACTERIZATION

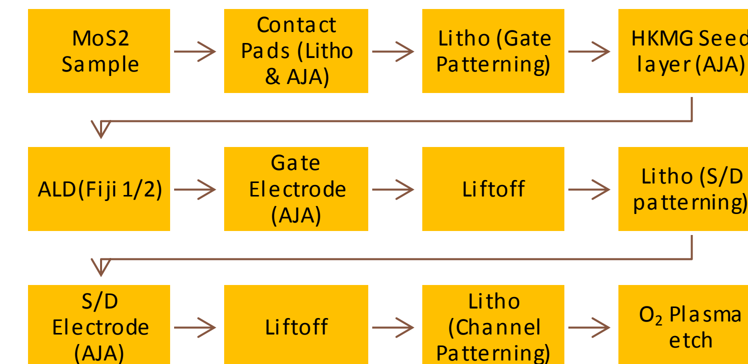
1. Seed layer deposition creates nucleation sites on 2D materials
   - Roughness decreases as seed layer thickness increases
2. Roughness variation is large on same sample
   - Mark samples first and measure same flakes (next quarter plan)

Next Quarter Plan: Top-gating 2D-Devices

- MOSFET structure for I-V measurement
  - C-V for extracting dielectric constant is difficult due to ultrathin film (~0.65nm for 1L MoS_2)



- Different seed material & ALD material
  - Various oxides available in Fiji & Different seed layer i.e. Hf



- PEALD on 2D materials
  - Potential damage on surface due to plasma
- Mark samples to measure on same flake (or spot) using litho
  - Potential PR residue problem
- Total expenditure for autumn quarter: $4943.09 (Most of the trainings are done!)