2015 EE410-LOCOS 0.2µm Poly CMOS Process Run Card Lot ID:_____ STEP 0.00 - PHOTOMASK #0- ZERO LEVEL MARKS Starting materials is n-type silicon (5-10 ohm-cm). Add four test STEP 0.18 - RESIST DEVELOP wafers labeled T1-T4. T1 and T2 will travel with the device Develop using SVG Dev track, develop program 3 (develop) and wafers and get all of the processing steps. T3 and T4 will be bake program 1 (bake) added at Gate Ox and LTO Dep to be used for thickness measurements and for etch rate determination. For Zero Level System used: \(\supset svgdev \) \(\supset svgdev2 \) Marks, all device wafers are processed, plus T1 and T2. Use T1 Date ____ Time ____ Operator __ and T2 to optimize focus and exposure. STEP 0.01 - SCRIBE & CLEAN Hand-scribe wafers on the front side near the flat. Angle the lettering so no lines are drawn perpendicular or parallel to the flat. STEP 0.20 - VISUAL INSPECTION Visual microscope inspection. Check for defects, alignment and Piranha Clean in wbnometal - 120°C; 10min; Dump rinse; SRD exposure quality. Wafers inspected Date _____ Time ____ Operator __ STEP 0.10 - SINGE & PRIME yes standard oven singe/HMDS prime REWORK DONE? □yes □no Date _____ Time ____ Operator _____ Wafers reworked: Comments If yes, attach REWORK sheet here. STEP 0.12 - SPIN COAT RESIST STEP 0.24 - ALIGNMENT MARK SILICON ETCH Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge All device wafers plus T1 and T2. Exclusion, using SVG Coat track programs 7 (coat and softbake). amtetcher, Program 4 for 0:05:00. System used: Usvgcoat2 Usvgcoat (backup option) Date_____ Time ____ Operator _____ Date_____ Time _____ Operator _____ Comments STEP 0.25 - RESIST ASH STEP 0.13 - Spin Rinse Dry All device wafers plus T1 and T2 All device wafers plus T1 and T2; Inspect backside of wafers for particles/ resist, clean w/ q-tip if needed prior to SRD gasonics, recipe sequence 014 Date_____ Time _____ Operator _____ LithoSRD Comments Date_____ Time _____ Operator _____ STEP 0.26 - STANDARD RESIST STRIP Comments All device wafers plus T1 and T2 STEP 0.14 - NON-ALIGNED EXPOSURE wbnonmetal, Piranha @ 120°C, 30', dump rinse, spin dry Expose using ASML stepper: Date_____ Time _____ Operator _____ Job name: ee410LOCOSR1 Comments_Measure step ht (Spec 1200+/-200A)___ Layer ID: GLOBALMARKS Layer Number: 0 Image ID: XPA STEP 0.28 - STANDARD PRE-DIFFUSION CLEAN Reticle ID: 45023981A009 All device wafers plus T1 and T2. Exposure used: Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH @ 50°C, 10',dump rinse; 50:1 DI:HF @ Room Temp, 30 sec, dump rinse Date _____ Time ____ Operator __ 5:1:1 DI:H2O2:HCI @ 50°C, 10',dump rinse, spin dry Comments ____ Time _____ Operator ___ STEP 0.16 - POST EXPOSE BAKE Bake using SVG Dev track, bake program 1 (bake only) STEP 0.30 - BLANKET SUBSTRATE IMPLANT

Comments___

All device wafers- Add one bare Si (N-type) TW per box (scribed w/ implant ID) for monitoring; Store test wafers after implant.

Date _____ Time ____ Operator _____

Implant Services: 150 keV, P31, 1.5 x10¹³ cm⁻².

System used: □svgdev □svgdev2

Comments_

Date _____ Time ____ Operator __

2015 EE410-LOCOS 0.2µm Poly CMOS Process Run Card Lot ID:_____ STEP 0.32 - STANDARD PRE-DIFFUSION CLEAN STEP 1.13 – Spin Rinse Dry -All device wafers plus T1 and T2 All device wafers plus T1 and T2 Inspect & clean backside of all wafers for particles/ resist residue Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH, 50°C, 10', dump LithoSRD rinse, 50:1 DI:HF @ Room Temp, 30 sec, dump rinse Date _____ Time ____ Operator __ 5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse, spin dry Time Operator STEP 1.14 – ALIGNEDFOCUS-EXPOSURE MATRIX Expose using ASML stepper: STEP 0.34 - LOCOS PAD OXIDATION GROWTH Job name: ee410LOCOSR1 All device wafers plus T1 and T2. Ramped process 850°C, wet Layer ID: 1 Layer Number: ISO for 12min., ≈ 200Å, Thermco1: 1WETOX Image ID: ISO thermco2: 2WETOX Tube Used: ___ Reticle ID: EE410 2008 1 _____ Time _____ Operator ___ Focus Minimum: 0.0 um Focus Step: 0.2 um Oxide Growth Time: ___ Exposure Min.: 40 mJ Exposure Step: 10 mJ _ Exposure Used: ___ Comments: Focus Used: _ Time _ _____ Operator __ STEP 0.36 - LOCOS NITRIDE DEPOSITION All device wafers plus Test Wafers. 785°C, 2,000 Å Wafers must go in to Nitride deposition within 1 hour of oxide growth. thermcoNitride: Program: N2 STEP 1.16 - ALIGNED EXPOSURE tylannitride: Program Nitride2 Tube used_____ Expose using ASML stepper: Job name: ee410LOCOSR1 Layer ID: 1 Date _____ Time ____ Operator _____ Layer Number: ISO Image ID: ISO Nitride Deposition Time:____ Reticle ID: EE410 2008 1 Comments: Focus Used: ____ Exposure used:__ STEP0.38 -THICKNESS MEASUREMENT Date _____ Time ____ Operator _____ Use Woollam, WVASE program EE410 / LOCOS to measure the oxide and nitride thickness and uniformity on T1. Comments_ Oxide: T_____ C___ B____ R____ L____ STEP 1.18 – POST EXPOSE BAKE Nitride: T_____ C___ B____ R____ L____ Bake using SVG Dev track, bake program 1 (bake only) Thk % Uniformity: Oxide_____ Nitride_____ System: □svgdev □svgdev2 Date _____ Time ____ Operator _____ Comments Comments____ STEP 1.00 - PHOTOMASK #1- ISO All device wafers plus T1 and T2. Use T1 and T2 to optimize focus and exposure. STEP 1.20 - RESIST DEVELOP Develop using SVG Dev track, develop program 3 (develop) and bake program 1 (bake) STEP 1.10 - SINGE & PRIME yes standard oven singe/HMDS prime System: □svgdev □svgdev2 ___ Time _____ Operator ___ Date _____ Time ____ Operator ____ Comments_ Comments_____

STEP 1.22 – VISUAL INSPECTION Visual and microscope inspection. Check for defects, alignment and exposure quality.	
Wafers inspected	
Date Time Operator	
Comments	

STEP 1.12 - SPIN COAT RESIST

Comments_

Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).

____ Time _____ Operator___

System used: \(\sumsystem \) svgcoat (backup option)

2015 EE410-LOCOS 0.2µm Poly CMOS Process Run Card Lot ID:____ REWORK DONE? □yes □no STEP 1.34 - THICKNESS MEASUREMENT Use Nanospec program 1 to measure the Field oxide thickness Wafers reworked: and uniformity on T1. If yes, attach REWORK sheet here. Oxide: T____ C__ B__ R__ L___ STEP 1.24 - LOCOS NITRIDE DRY ETCH Thk % Uniformity: Oxide_____ All device wafers plus T1 and T2. Use T1 to establish the etch Comments Drvtek 2: Recipe: Nitride STEP 1.36 – OXIDIZED NITRIDE STRIP 6:1 BOE, ~45sec. Total Etch Time _____ Date_____ Time ____ Operator _____ **WBNONMETAL** Comments _ Etch Time: Date _____ Time ____ Operator _____ STEP 1.26 - THICKNESS MEASUREMENT Use Nanospec program 7 to measure the Pad oxide thickness Comments: _ and uniformity on T1. Oxide: T____ C__ B__ R__ L___ STEP 1.38 - NITRIDE WET STRIP All device wafers plus T1 and T2. Thk % Uniformity: Oxide wbnitride, Hot Phosphoric Acid, 155C, ~60min., dump rinse, Comments spin dry STEP 1.27 - RESIST ASH All device wafers plus T1 and T2 Date _____ Time ____ Operator ____ gasonics, recipe sequence 014 Comments: _ Date_____ Time ____ Operator _____ STEP 1.40 - THICKNESS MEASUREMENT Comments Use Nanospec program 1 to measure the field oxide and program 7 to measure the Pad oxide and uniformity on T1. FieldOx: T____ C___ B___ R___ L____ STEP 1.28 - STANDARD RESIST STRIP All device wafers plus T1 and T2 Thk % Uniformity: FieldOx_____ wbnonmetal, Piranha @ 120°C, 20', dump rinse, spin dry PadOx: T____ C__ B__ R___ L___ Date_____ Time _____ Operator _____ Thk % Uniformity: PadOx Comments Comments STEP 1.30 - STANDARD PRE-DIFFUSION CLEAN STEP 2.00 - PHOTOMASK #2 - P-WELL IMPLANT All device wafers plus T1 and T2 All device wafers plus T1 and T2. Use T1 and T2 to optimize focus and exposure. Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH @ 50°C, 10', dump rinse; 50:1 DI:HF @ Room Temp, 30 sec, dump rinse; 5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse, spin dry STEP 2.10 - SINGE & PRIME yes standard oven singe/HMDS prime Date_____ Time _____ Operator _____ Date _____ Time ____ Operator _ Comments_ Comments **STEP 1.32 - FIELD OXIDATION** All device wafers plus T1 and T2. Ramped process STEP 2.12 - SPIN COAT RESIST Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Wet Oxide at 1000C, 1hr:40 min, ~5,400 Å Exclusion, using SVG Coat track programs 7 (coat and softbake). Thermco1 or 2: WETOX ☐ Thermco1 ☐ Thermco2 System used: : \(\supset svgcoat \) (backup option) Date_____ Time _____ Operator___ Date _____ Time ____ Operator _____ Comments Comments_

2015 EE410-LOCOS 0.2µm Poly CMOS Process Run Card Lot ID: STEP 2.13 - Spin Rinse Dry STEP 2.23 - RESIST ASH All device wafers plus T1 and T2 All device wafers plus T1 and T2 Inspect backside of wafers for particles and resist residue & clean prior to SRD gasonics, recipe sequence 014 LithoSRD ____ Time _____ Operator ___ Time _____ Operator __ Comments STEP 2.24 - STANDARD RESIST STRIP All device wafers plus T1 and T2 STEP 2.14 - ALIGNED EXPOSURE Expose using ASML stepper: wbnonmetal, Piranha @ 120°C, 20', dump rinse, spin dry Job name: ee410LOCOSR1 Layer ID: 2 Date_____ Time ____ Operator ___ Layer Number: P-WELL Image ID: P-WELL Comments_ Reticle ID: EE410 2008 1 STEP 2.26 - STANDARD PRE-DIFFUSION CLEAN Exposure used:___ All device wafers plus T1 and T2 Date _____ Time ____ Operator ___ Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH, 50°C, 10', dump rinse; 50:1 DI:HF @ Room Temp, 30 sec, dump rinse; Comments_ 5:1:1 DI:H2O2:HCI @ 50°C, 10', dump rinse, spin dry STEP 2.16 – POST EXPOSE BAKE ___ Time _____ Operator __ Bake using SVG Dev track, bake program 1 (bake only) Comments System: □svgdev □svgdev2 STEP 2.28 - Kooi Oxidation and P-WELL Drive-In Date _____ Time ____ Operator _____ All device wafers plus T1 and T2. Comments Thermco1: 1WTOXAN Kooi: 15min, 850C in steam STEP 2.18 - RESIST DEVELOP Drive-in: 300min, 1000C in nitrogen Develop using SVG Dev track, develop program 3 (develop) and _____ Time _____ Operator _____ bake program 1 (bake) System used: □svgdev □svgdev2 Comments_ Date _____ Time ____Operator __ STEP 2.30 - THICKNESS MEASUREMENT Use the Nanospec program 1 to measure the Kooi oxide Comments___ thickness and uniformity on T1. STEP 2.20 - VISUAL INSPECTION Oxide: T____ C___ B____ R___ L___ Visual and microscope inspection. Check for defects, alignment Thk % Uniformity: Oxide_____ and exposure quality. Wafers inspected ___ Comments Date _____ Time ____ Operator _ STEP 2.32 - STANDARD PRE-DIFFUSION CLEAN All device wafers plus T1, T2 and T3 (for Gate Ox measurement) REWORK DONE? □yes \Box no Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH, 50°C, 10', dump Wafers reworked: rinse; 50:1 DI:HF @ Room Temp, 30 sec, dump rinse; If yes, attach REWORK sheet here. 5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse, spin dry ____ Time _____ Operator ___ STEP 2.22 - P-WELL IMPLANT All device wafers- Add one bare Si (N-type) TW per box (scribed w/ implant ID) for monitoring; Store test wafers after implant. Implant Services: 180keV, 4e13, B11 cm⁻². STEP 2.34 - SACRIFICIAL OXIDE STRIP All device wafers plus T1,T2 & T3 Date _____ Time ____ Operator ____ Wbclean-1 or -2 50:1 DI:HF @ Room Temp, dump rinse, spin dry Comments ____ ___mins Etch Time: _____

Date_____ Time _____ Operator _____

Comments

2015 EE410-LOCOS 0.2µm Poly CMOS Process Run Card

Lot ID:_

STEP 2.36 - THICKNESS MEASUREMENT Use Nanospec program 7 (thin oxide) to measure T1 to ensure complete Sacrificial oxide removal.	Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).
System used: □nanospec □nanospec2	System used: : svgcoat2 svgcoat (backup option)
TCBRL	Date Time Operator
Date Time Operator	Comments
Comments	STEP 3.13 – Spin Rinse Dry -All device wafers plus T1 and T2 Inspect and clean backside of wafers for particles/ resist residues
STEP 2.38 - GATE OXIDATION All device wafers plus T1, T2 and T3. Ramped process 20min @ 900°C, dry for ~100Å	LithoSRD Date Time Operator
NOTE: Run (1/2)TLCCLEA program on Thermco 1/2 to clean	Comments
tube before GATEOX. This will take about 4 hours to complete. Wafers must go immediately into thermcopoly after GateOx with no cleaning steps. This is to ensure contamination is minimal.	STEP 3.14 – ALIGNED EXPOSE
Thermco1 or 2: (1/2) DRYOX	Expose using asml stepper: Job name: ee410LOCOSR1
Oxidation Time:	Layer ID: GATE Layer Number: 3
Date Time Operator	Image ID: GATE Reticle ID: EE410 2008 1
Comments:	Date Time Operator
STEP 2.40 - POLYSILICON DEPOSITION	Exposure used:
All device wafers plus T1 and T2. T3 has been removed for Gate Ox measurement.	Comments
LPCVD @ 550°C, ≈ 2,000Å	STEP 3.16 – POST EXPOSE BAKE Bake using SVG Dev track, bake program 1 (bake only)
Thermocpoly Program P550POLY	System: □svgdev □svgdev2
Deposition Time:	Date Time Operator
Date Time Operator	Comments
Comments:	STEP 3.18 - RESIST DEVELOP
STEP 2.42 – THICKNESS MEASUREMENT	Develop using SVG Dev track, develop program 3 (develop) and bake program 1 (bake)
Use Woollam, WVASE program EE410 / GATE POLY to measure the oxide and nitride thickness and uniformity on T1.	System used: □svgdev □svgdev2
Poly: T C B R L	Date Time Operator
Oxide: T C B R L	Comments
Thk % Uniformity: Poly Oxide	STEP 3.20 - INSPECTION Inspect and clean backside of all wafers for particles/ residues.
Comments	Visual and microscope inspection. Check for defects, alignment AND exposure quality.
STEP 3.00 - PHOTOMASK #3 - GATE All device wafers plus T1 and T2. Use T1 and T2 to optimize focus and exposure.	Wafers inspected Date Time Operator
STEP 3.10 - SINGE & PRIME yes standard oven singe/HMDS prime	Comments
Date Time Operator	REWORK DONE? □yes □no
Comments	Wafers reworked: If yes, attach REWORK sheet here.
	ii yoo, allaan KEVVOIM Sheet hele.

2015 EE410-LOCOS 0.2µm Poly CMOS Process Run Card Lot ID: STEP 3.22 - POLY ETCH Exposure used: All device wafers plus T1 and T2. Use T1 to establish end point Comments time. P5000 Program: POLY ETCH STEP 4.16 – POST EXPOSE BAKE End Point Algorithm: SU_POLY1.alg Bake using SVG Dev track, bake program 1 (bake only) End Point Time: Over Etch Time System: □svgdev □svgdev2 Date _____ Time ____ Operator _____ Date _____ Time ____ Operator __ Comments_ Comments STEP 3.23- RESIST ASH STEP 4.18 - RESIST DEVELOP All device wafers plus T1 and T2 Develop using SVG Dev track, programs 3 (develop) and 1 (bake) gasonics, recipe sequence 014 System used: □svgdev □svgdev2 Date_____ Time ____ Operator _____ Date_____ Time _____ Operator __ STEP 3.24 - STANDARD RESIST STRIP STEP 4.20 - VISUAL INSPECTION All device wafers plus T1 and T2 Visual and microscope inspection. Check for defects, alignment and exposure quality. wbnonmetal, Piranha @ 120°C, 20', dump rinse, spin dry Wafers inspected ____ Date_____ Time ____ Operator __ Date _____ Time ____ __ Operator __ Comments STEP 4.00 - PHOTOMASK #4 - N-DOPE All device wafers plus T1 and T2. Use T1 and T2 to optimize REWORK DONE? □yes □no focus and exposure. Wafers reworked: If yes, attach REWORK sheet here. STEP 4.10 - SINGE & PRIME yes standard oven singe/HMDS prime STEP 4.22 - RESIST HARDENING (for implantation) ___ Time _____ Operator ___ Hard bake 30 mins @ 110C. Comments__ Time Operator STEP 4.12 - SPIN COAT RESIST Comments Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake). STEP 4.24 - N-SOURCE/DRAIN IMPLANT All device wafers- Add one bare Si (N-type) TW per box (scribed System used: : \(\supset svgcoat \) \(\supset \) \(\supset svgcoat \) \(\text{(backup option)} \) w/ implant ID) for monitoring; Store test wafers after implant. Date _____ Time ____ Operator __ Implant Services: 50 keV, As75, 2x10¹⁵ cm⁻² Comments Date _____ Time _____ Operator ____ STEP 4.13 – Spin Rinse Dry -All device wafers plus T1 and T2 Comments Inspect and clean backside for particles and resist residues STEP 4.26 - RESIST ASH All device wafers plus T1 and T2 Date Time Operator gasonics, recipe sequence 014 Date_____ Time _____ Operator _____ STEP 4.14 - ALIGNED EXPOSE Comments Expose using asml stepper: Job name: ee410LOCOSR1 STEP 4.26 - STANDARD RESIST STRIP Layer ID: N-DOPE All device wafers plus T1 and T2 Laver Number: 4 Image ID: N-DOPE wbnonmetal, Piranha @ 120°C, 20', dump rinse, spin dry Reticle ID: EE410 2008 1 Date_____ Time ____ Operator ____ _____ Time _____ Operator __

Lot ID: 2015 EE410-LOCOS 0.2µm Poly CMOS Process Run Card Comments STEP 6.10 - SINGE & PRIME yes standard oven singe/HMDS prime STEP 5.00 - P-DOPE BLANKET IMPLANT Date _____ Time ____ Operator _____ All device wafers- Add one bare Si (N-type) TW per box (scribed w/ implant ID) for monitoring; Store test wafers after implant. Comments *Implant Service:* 50 keV, BF₂ 49, 5x10¹⁴ cm⁻² Date _____ Time _____ Operator ___ STEP 6.12 - SPIN COAT RESIST Comments _ Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake). STEP 5.30 - STANDARD PRE-DIFFUSION CLEAN System used: : Dsvgcoat2 Dsvgcoat (backup option) All device wafers plus T1, T2 and T4. Date _____ Time ____ Operator __ Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH @ 50°C, 10', dump rinse; 50:1 DI:HF @ Room Temp, 30 sec, dump rinse; Comments 5:1:1 DI:H2O2:HCI @ 50°C, 10', dump rinse, spin dry STEP 6.13 - Spin Rinse Dry- All device wafers plus T1 and T2 Date_____ Time _____ Operator _____ Inspect and clean backside for particles and resist residues Comments LithoSRD STEP 5.32 - LTO DEPOSITION Date_____ Time ____ Operator _____ All device wafers plus T1, T2 and T4 (for LTO measurement after Densify). Undoped, LPCVD @ 400°C, ≈ 6000Å Comments tylanbpsg, Program LTO400PC STEP 6.14- ALIGNED EXPOSE Expose using asml stepper: Date_____ Time _____ Operator _____ Job name: ee410LOCOSR1 Layer ID: CONTACT Comments Layer Number: 6 Image ID: CONTACT STEP 5.34 - MODIFIED PRE-DIFFUSION CLEAN Reticle ID: EE410 2008 2 Note: The Modified Pre-Diffusion clean may be omitted if wafers Date _____ Time ____ Operator ____ move from LTO dep to LTO densification in less than one hour. All device wafers plus T1, T2 and T4 (for LTO measurement after Exposure used:___ Densification) Comments Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH @ 50°C, 10', dump rinse; 5:1:1 DI:H2O2:HCI @ 50°C, 10', dump rinse, spin dry STEP 6.16 - POST EXPOSE BAKE Time _____ Operator _ Bake using SVG Dev track, bake program 1 (bake only) System: □svgdev □svgdev2 Comments Date _____ Time ____ Operator __ STEP 5.36 - LTO DENSIFICATION All device wafers plus T1, T2 and T4. Ramped process 30' min @ Comments_ 950°C, in steam STEP 6.18 - RESIST DEVELOP Thermco1, 2 or 3: 1/2/3WETOX Tube___ Bake using SVG Dev track, programs 3 (develop) and 1 (bake) ____ Time _____ Operator System used: □svgdev □svgdev2 Comments_____ Date_____ Time ____ Operator ___ STEP 5.38 -THICKNESS MEASUREMENT Comments_____ Use Nanospec program 1 to measure the LTO thickness and uniformity on T1. STEP 6.20 - VISUAL INSPECTION Oxide: T____ C__ B___ R__ L___ Visual and microscope inspection. Check for defects, alignment and exposure quality. Thk % Uniformity: Oxide Wafers inspected _____ Comments Date _____ Time ____ Operator ____

Comments _____

STEP 6.00 - PHOTOMASK #6 - CONTACT

and so needs to be patterned.

All device wafers plus T1,T2, and T4. Use T1 and T2 to optimize focus and exposure. T4 will be used as a test wafer at SiO₂ RIE

2015 EE410-LOCOS 0.2µm Poly CMOS Process Run Card Lot ID:_____ REWORK DONE? □yes □no STEP 7.10 - SINGE & PRIME yes standard oven singe/HMDS prime Wafers reworked: If yes, attach REWORK sheet here. Date_____ Time ____ Operator ____ Comments STEP 6.22- PLASMA OXIDE ETCH All device wafers plus T1, T2 and T4. Establish the etch rate using T4. STEP 7.12 -1.6 micron SPIN COAT RESIST Apply 1.6 micron of 3612 positive resist w/o VP and 2mm Edge amtetcher, Program 3, CHF₃/O₂ Exclusion, using SVG Coat track program 8 (coat and softbake). System used: : Dsvgcoat2 Dsvgcoat (backup option) Etch Rate: _____ Etch Time:___ Date _____ Time ____ Operator _ Date _____ Time ____ Operator _____ Comments Comments STEP 7.13 - Spin Rinse Dry- All device wafers plus T1 and T2 STEP 6.24 - THICKNESS MEASUREMENT Use Nanospec program 7 (thin oxide) to measure T1 to ensure Inspect and clean backside for particles and resist residues complete oxide removal. LithoSRD System used: □nanospec □nanospec2 Date_____ Time ____ Operator _____ T______B____R___L____ Comments Date_____ Time ____ Operator __ STEP 7.14 - ALIGNED EXPOSE Comments Expose using asml stepper: Job name: ee410LOCOSR1 Layer ID: 7 STEP 6.24 - RESIST ASH Layer Number: METAL Image ID: METAL1 gasonics, recipe sequence 014 Reticle ID: EE410 2008 2 Date_____ Time _____ Operator _____ Date _____ Time ____ Operator __ Comments Exposure used:____ STEP 6.26 STANDARD RESIST STRIP Comments__ All device wafers plus T1 and T2. T4 may be omitted at this point. STEP 6.16 – POST EXPOSE BAKE wbnonmetal, Piranha @ 120°C, 20', rinse, spin dry Bake using SVG Dev track, bake program 2 (bake only) Date_____ Time ____ Operator _____ System: □svgdev □svgdev2 Comments Date _____ Time ____ Operator __ STEP 6.28 - STANDARD PRE-METAL CLEAN Comments All device wafers plus T1 and T2 STEP 7.16 - RESIST DEVELOP Wbclean-1 or-2, 5:1:1 H2O:H2O2:NH4OH @ 50°C, 10', dump Bake using SVG Dev track, programs 4 (develop) and 2 (bake) rinse; 5:1:1 DI:H2O2:HCI @ 50°C, 10', dump rinse 50:1 DI:HF @ Room Temp, 30 sec, dump rinse; spin dry System used: □svgdev □svgdev2 Date_____ Time _____ Operator _____ Date_____ Time _____ Operator ___ Comments_ Comments_ STEP 6.30 - METAL DEPOSITION STEP 7.18 - VISUAL INSPECTION Inspect and clean backside for particles and resist residues Intlvac_sputter, 10,000A of Al-1%Si; Program: STANDARD B Visual and microscope inspection. Check for defects, alignment and exposure quality. Date_____ Time _____ Operator _____ Wafers inspected _____ Comments Date _____ Time ____ Operator __ STEP 7.00 - PHOTOMASK #7 - METAL All device wafers plus T1 and T2. Use T1 and T2 to optimize Comments _

focus and exposure.

2015 EE410-LOCOS 0.2µm Poly CMOS Process Run Card		
REWORK DONE? □yes □no		
Wafers reworked: If yes, attach REWORK sheet here.		
STEP 7.20 - METAL ETCH		
<i>p5000etch</i> , Recipe CH A. METAL, ~120-150 sec. End Point Algorithm: SU_AI_Ig.alg		
End Point Time: Overetch Time:		
Date Time Operator		
Comments		
STEP 7.22 – POST ETCH METAL PASSIVATION Must be done immediately following removal from etch system		
wbmetal, dump rinse, spin rinse dry		
Date Time Operator		
Comments		
STEP 7.24 - METAL RESIST STRIP Make sure the wafers are dry before putting in to PRS-3000 bath.		
wbmetal, PRS-3000, @ 60°C, 20'; dump rinse, spin dry		
Date Time Operator		
Comments		
STEP 7.26 - METAL CLEAN Make sure the wafers are dry before putting in to PRS1000 bath.		
wbmetal, PRS1000, @ 40°C, 10', dump rinse, spin dry		
Date Time Operator		
Comments		
OTER 7.00 ANNEAL AND ALLOY		
STEP 7.30 - ANNEAL AND ALLOY 45' forming gas (4% H ₂ in N ₂) @ 400°C		
tylanfga Program FGA400		
Date Time Operator		
Comments		

ELECTRICAL TEST!

Lot ID:____

2015 EE410-LOCOS 0.2µm Poly CMOS Process Run Card Lot ID: STEP 100.00 - REWORK SHEET STEP 100.18 - VISUAL INSPECTION REWORK PHOTOMASK LAYER# Visual and microscope inspection. Check for defects, alignment and exposure quality. Reworked wafers: Wafers inspected ___ ☐ Resist removal for wafers before metal deposition: Date _____ Time ____ Operator ___ wbnonmetal, piranha clean, dump rinse 6X, spin-rinse dry Comments _ ____ Time _____ Operator _ ☐ Resist removal for wafers after metal deposition wbmetal, PRS1000, dump rinse, spin-rinse dry ____ Time _____ Operator ___ Comments STEP 100.10 - SINGE & PRIME yes standard oven singe/HMDS prime ____ Time _____ Operator __ Comments_ STEP 100.12 - RESIST SPIN COAT Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG coat programs 7 (coat and softbake) System used: : \(\supset svgcoat2 \) \(\supset svgcoat \((backup option) \) ___ Time ____ _____ Operator __ Comments _ STEP 100.13 - Spin Rinse Dry- All device wafers plus T1 and T2 - Inspect and clean backside for particles and resist residues LithoSRD Date_____ Time ____ Operator __ Comments_ STEP 100.14 - ALIGNED EXPOSE Expose using ASML Stepper, □ 0 - Global Marks: ee410LOCOSR1: 45023981A009 ☐ 1 - ISO: ee410LOCOSR1: EE410 2008 1 □ 2 - P-Well: ee410LOCOSR1: EE410 2008 1 □ 3 - Gate: ee410LOCOSR1: EE410 2008 1 □ 4 - N-Dope: ee410LOCOSR1: EE410 2008 1 ☐ 6 - Contact: ee410LOCOSR1: EE410 2008 2 ☐ 7 - Metal: ee410LOCOSR1: EE410 2008 2 Exposure Used: ___ ____ Time ____ Operator __ Comments STEP 100.16 - RESIST DEVELOP Develop using SVG Dev track, programs 3 (develop) and 1 (bake) System used: \(\supset svgdev \) \(\supset svgdev2 \) Time _____ Operator ____

Comments _

2015 EE410-LOCOS 0.2µm Poly CMOS Process Run Card Lot ID: STEP 200.00 - REWORK SHEET STEP 200.18 - VISUAL INSPECTION REWORK PHOTOMASK LAYER# Visual and microscope inspection. Check for defects, alignment and exposure quality. Reworked wafers: Wafers inspected ___ ☐ Resist removal for wafers before metal deposition: Date _____ Time ____ Operator ___ wbnonmetal, piranha clean, dump rinse 6X, spin-rinse dry Comments _ ____ Time _____ Operator _ ☐ Resist removal for wafers after metal deposition wbmetal, PRS1000, dump rinse, spin-rinse dry ____ Time _____ Operator ___ Comments STEP 200.10 - SINGE & PRIME yes standard oven singe/HMDS prime ____ Time _____ Operator __ Comments_ STEP 200.12 - RESIST SPIN COAT Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG coat programs 7 (coat and softbake) System used: : \(\supset svgcoat2 \) \(\supset svgcoat \((backup option) \) ___ Time ____ ____ Operator _ Comments _ STEP 200.13 - Spin Rinse Dry- All device wafers plus T1 and T2 - Inspect and clean backside for particles and resist residues LithoSRD Date_____ Time ____ Operator __ Comments_ STEP 200.14 - ALIGNED EXPOSE Expose using ASML Stepper, □ 0 - Global Marks: ee410LOCOSR1: 45023981A009 ☐ 1 - ISO: ee410LOCOSR1: EE410 2008 1 □ 2 - P-Well: ee410LOCOSR1: EE410 2008 1 □ 3 - Gate: ee410LOCOSR1: EE410 2008 1 □ 4 - N-Dope: ee410LOCOSR1: EE410 2008 1 ☐ 6 - Contact: ee410LOCOSR1: EE410 2008 2 ☐ 7 - Metal: ee410LOCOSR1: EE410 2008 2 Exposure Used: ___ ____ Time ____ Operator __ Comments STEP 200.16 - RESIST DEVELOP Develop using SVG Dev track, programs 3 (develop) and 1 (bake) System used: \(\supset svgdev \) \(\supset svgdev2 \) ____ Time ____ Operator ____

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