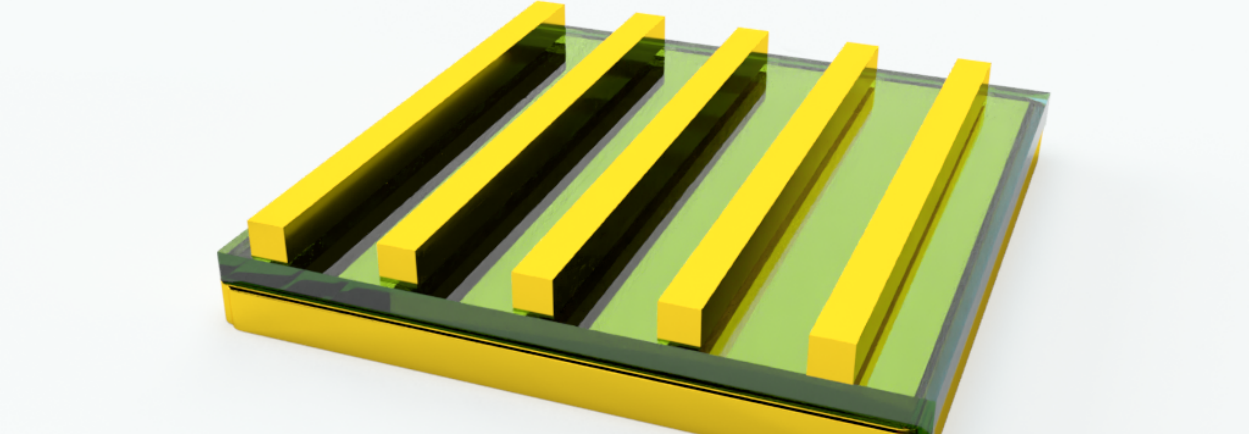

Standard Operating Procedures

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Sub-micron metal patterning on polymer substrates using nitride nanostencil

Materials

1. 1 or more silicon wafers: 100 mm, ≤350 um thick, <100> orientation, double polished
2. 3 silicon dummy wafers: 100 mm
3. Target substrate: silicon, polymer, or any other material that you want to nanopattern metal on
4. Positive photoresist: Shipley SPR 3612
5. KOH 45%
6. Positive EBL resist: CSAR

Tools:

1. Wafer cleaning: *wbclean1*
2. LPCVD: *ThermcoNitride*
3. Photoresist prime: *yes*
4. Photoresist deposition: *svgcoat*
5. Photolithography: *Heidelberg1* or *Heidelberg2*
6. Reactive Ion Etching: *oxford-rie* and *RIE: Oxford PlasmaPro 80*
7. Electron beam lithography: *JEOL Ebeam_snp*
8. KOH etching setup: *wbflexcorr-4*

Procedure:

I. Silicon nitride deposition

1. Clean all Si wafers (including dummy) on *wbclean1*: SC1 (5:1:1 = water: H2O2: NH4OH) at 50 C for 3 to 4 dips- > dump rinse -> SC2 (5:1:1 = water: H2O2: HCl) at 50 C for 3 to 4 dips -> dump rinse -> SRD machine.
2. Coat silicon nitride in LPCVD *thermcoNitride:* Put 2 dummy wafers (2 in front of and 1 behind process wafers). Run recipe LSN3 for 50 min to get ~350 nm silicon nitride layer.
3. Measure thickness of SiN_x layer across the surface. This thickness measurement will be used to determine the RIE time. The tools that can do this are the *nanospec3* or *woollam* using spectroscopy and ellipsometry, respectively.

Notes:
Use LPCVD not PECVD. LPCVD results in a denser and lower stress nitride layer.

II. Photolithography of backside windows

Use photolithography to pattern a mask of windows for the dry etching of backside SiN_x.

1. Prime the double polished wafers with HMDS to enhance SPR 3612 resist adhesion. Run the standard cycle in the *yes* oven.
2. Coat positive photoresist on one side of the wafers using the *svgcoat*. This side will become the back of the wafers (i.e. the side without the membranes). Use 1 um thickness SPR 3612 without HMDS prime (as it was done previously), no EBR, and 60 s at 90 C.
3. Measure bow of the wafers on flexus. This is a safety measure to make sure that the wafers have low bow and will not touch the write head of the direct write photolithography machine. If bow is greater than 20 um, do not use the wafers and redo the silicon nitride deposition to be more uniform. A perfectly uniform SiN_x deposition on front and back should have very low bow (<10 um).
4. Expose backside window pattern using direct write photolithography machine *heidelberg*. Use dose 70 defocus -2 for optical autofocus focus on *heidelberg2*.
5. Post exposure bake: 115 C for 1 min on hotplate.
6. Develop: 40 s in MF-26A developer.
7. Post bake at 110 C for 60 s on hotplate.

III. Reactive Ion etching (RIE) of backside window mask

Etch backside SiN_x to create bare Si surface for etching with KOH later. Use Oxford RIE *oxford-rie* in SNF.

1. Use proper oxygen plasma clean for machine, and condition on a test wafer.
2. Etch using the following recipe:

Table 1. Nitride dry etching recipe (SNF Oxford RIE)

Recipe name	OA-SiN-RIE1
Gas flow	75: 15: 10 = CHF_3: CF_4: O_2
Forward power	200 W
DC bias	508 V
Time	5 min

Notes:

Time for etching may vary. If the SiN_x thickness is greater than 350 nm use a longer etching time. The Oxford RIE in SNF usually requires EBR on the wafers inserted. Consult the tool trainer to approve of no EBR.

IV. Potassium Hydroxide etching through Si wafer

Use SiN_x as a mask and KOH solution to etch all the way through wafer to form nitride membranes in the window regions.

1. In *wbflexcorr-4*, create a 30% KOH solution in large beaker by combining 1500 ml of 45% KOH with 750 ml of water.
2. Place beaker of the solution in temperature-controlled bath of water set to 90 C. Use a condenser on top. Wait for bath to come to 90 C (about 1 hour).
3. Place wafers inside the solution and recover with condenser. This is the beginning of the etching. Start a timer and run the process for the desired time assuming about a 135 um/hour etch rate. Mix the KOH solution every hour or so to make sure KOH concentration is uniform throughout the beaker and that the etch rate is constant.
4. After etching has finished, remove beakers from KOH solution and wash KOH off-of wafers (see post notes): Fill one or more beakers with water, enough to completely submerge the wafers and their containers. Dip the wafers in the water, moving up and down for 60 s. Make sure not to apply fluid pressure to the membranes by moving them perpendicular to the surface plane. Remove wafers and replace water with fresh water. Repeat 6 times.
5. Do a quick visual check to see if the membranes are etched through. The membranes should be almost completely transparent.
6. Dry wafers on hot plate at 90 C. Do not blow dry, as the air pressure may break the membranes.
7. Check under microscope to make sure that all the Si has been etched away and the backs of the membranes are clear of KOH solution. If the membranes are opaque and not completely etched through, return them to the KOH bath. If there appears to be drops on the back of the membranes, re rinse the wafers or try a more vigorous washing method (see notes).

Notes:

1. During our attempts to wash the KOH of the wafers, there was still some KOH solution dotting the back of the membranes. A more vigorous wash may be required, such as a spray wash with water. You can test if there is any KOH left in the water wash bath by measuring the pH with pH paper.
2. After a rinse, if the membranes are broken you can see the water form a meniscus around where the windows are indicating there is no material there. If the water does not do this, you can assume the membrane is still intact.

V. Electron beam lithography on silicon nitride membrane

Use electron beam lithography (EBL) to define the final pattern on the SiN_x membranes. This process sacrifices two of the windows for alignment and does not need front side alignment markers.

1. Spin coat 200 nm CSAR positive e-beam resist. If you have a non-vacuum chuck, use it. If not, attach the membrane wafer to a larger dummy wafer using Kapton tapes. In addition, place 4 square bumps (for example, double-sided foam mounting tapes) on the 4 sides around the wafer to further

prevent wafers from flying away during the spin coating process. If possible, use many kapton tapes around the wafer to prevent the resist leak to the backside of the wafer. When leaked, the resist may attach two wafers tightly and it can be difficult to separate the them.

2. Use an optical microscope to adjust the rotation of the wafer on the holder. Manually rotate the wafer until the rotation angle is less than 6 um/mm ($\Delta y/\Delta x$). This step makes it easier to later find the sacrificial windows in SEM. Take notes of the coordinates of the center of the sacrificial windows.
3. Expose on EBL machine (JEOL):
    a. In the schedule file (.sdf), enable manual alignment option by uncomment the following. Command line: GLMDET M; Global alignment (M is for Manual).
    b. In the job file (.jdf), type the coordinates of the center of the two sacrificial windows (P and Q). The coordinates should match their coordinates in the v30 pattern. Command line: GLMPOS P = (-22000, 0), Q = (22000, 0).
    c. Use the SEM to locate where P and Q actually are. Use the coordinates measured in the optical microscope as a starting point. Move the stage around to find the exact position of P and Q. Calculate the needed offset in x direction and y direction. Type the offset in the schedule file.
    d. Expose patterns. A window will pop up to ask you confirm the alignment mark positions. Use SEM to verify the positions, if things are as expected, continue to exposure.
    e. Expose the remaining windows. Choose propose dose and current for your pattern.
4. Develop in xylenes for 40 s, rinse in IPA, and dry on hot plate at 90 C.

VI. Reactive ion etching of silicon nitride membrane

Use RIE with CSAR mask to etch the patterns into the SiN_x membranes. Use SNSF *RIE: Oxford PlasmaPro 80*.

1. Follow appropriate plasma clean and conditioning recipes for machine.
2. Etch 25% more time than the time required to fully etch the SiN_x membranes for you given thickness. This will ensure that the SiN_x is fully etched through. For our 350 nm thick membranes we etched 10 min on the *RIE: Oxford PlasmaPro 80*.

Table 2: Nitride dry etching recipe (SNSF Oxford RIE)

Recipe name	Frank slow nit
Gas flow	15: 45: 30 = CHF_3: CF_4: Ar
Forward power	200 W
DC bias	440 V
Pressure	100 mTorr
Time	10 min

VII. Using nano stencil to deposit gold on silicon substrate

We now have SiN_x nano stencils with CSAR resist coating. Removal of the CSAR is not necessary, and the wet process can damage the membranes. Here, we do not remove it. Use an evaporator with a large crucible to sample distance and source of evaporation as small as possible (ideally a point source).

1. Place the target wafer on the center of a flat evaporator chuck with many support clamp attachments.
2. Place the stencil on top (membrane side down), trying to avoid moving the stencil after it is in contact with target wafer.
3. Clamp the stencil to target wafer and use as many mechanical clamps as possible. Where this is not possible, use Kapton tape.
4. Place the stack into evaporator. After editing the recipe, use the gameboy to minimize the effective ebeam scanning size. Move the right joy stick left (reduce width) and down (reduce height). Move around the left joy stick to make sure the scanning region is centered. The display on the gameboy is a rough estimate.
5. Start evaporation. During the ramp up and the deposition, check the shape of the heated source. Don't enable substrate rotation.
6. Remove the chuck from evaporator, remove clamps, and then pull off stencil gently.

Notes:
To reduce the penumbra:
Maximize: Source to sample distance; number of mechanical clamps.
Minimize: Stencil to target wafer gap (To reduce the gap, you can choose a target wafer with the opposite bow to that of the stencil or use a piece of tape under target wafer to make it convex and give perfect contact between the two wafers); source size.