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High-k/SiO_2 Interface Charge Characterization for ALD Tools

Hong-Yu Chen hongyuc@stanford.edu
Luckshitha Liyanage luckys@stanford.edu

Mentor: J Provine

Abstract
Atomic Layer Deposition (ALD) has become a popular thin film deposition technique due to atomic level thickness control and reproducibility. Recent literature has reported different types of charges that arise at SiO_2/high-k interface which can substantially affect device performance. In this study, we characterized the charge densities for films deposited by CV studies for Savannah ALD. We developed a robust process flow and utilized standard analysis techniques following an extensive literature study. Interface dipole effects were observed and Interface charge densities were extracted for HfO_2, Al_2O_3 high-k materials under different forming gas anneal (FGA) conditions. In addition, our methodology can be used as a basis/standard for future cross contamination studies.

Introduction

One of the critical issues of high-k/metal gate CMOS is to control the threshold voltage (V_{th}). In the past fixed charge has been utilized to control the threshold voltage. Recent experimental results have demonstrated that a dipole layer formation at high-k/SiO_2 interface should be a dominant origin of the V_{th} shift. The direction and magnitude of V_{th} shift depend on the employed high-k materials as shown in Fig. 1.[1] This phenomena can be utilized as a V_{th} tuning technique and a barrier height tuning technique [2] for both high-k/metal gate transistors and schottkey diodes respectively. The technologically optimal conditions for a particular application can be found by understanding how these charges behave for different materials and/or process conditions. In this study, we hope to characterize the high-k/SiO_2 interface charge and contribute to the overall understanding of the interface quality which is a significant contribution to the SNF community.

In addition, our understanding of such charges can be utilized in some of the most promising novel materials such as carbon nanotubes (CNTs) on future nanoelectronic applications. One challenge of realizing complementary carbon nanotube field-effect transistor (CNFETs) circuits is the lack of NFETs. However, a change in carrier type (doping effect) of Carbon Nanotubes has been recently reported using atomic layer deposition (ALD) of HfO_2 on top of nanotubes. Although the underlying mechanism was not fully understood, the result was attributed to the charges that exist in the high-k layer [3], [4]. Therefore understanding the high-k/SiO_2 interface charges was vital not only for the SNF community, but also for us as researchers in the CNT community.

Thus, the objective of this project is to study the high-k/SiO_2 interface quality by fabricating the MOSCAPs and characterizing the interface charge/dipoles by CV measurements in Stanford Nanofabrication Facilities (SNF).

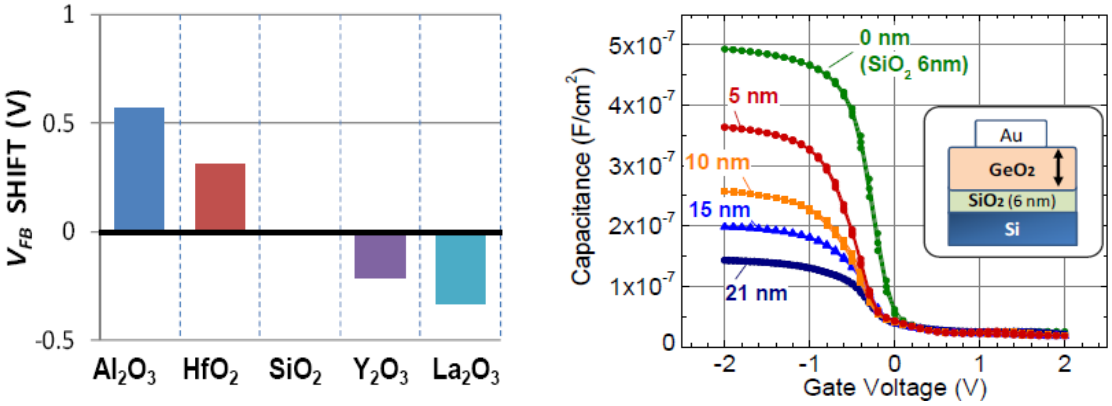


Figure 1: (Left) Experimentally observed V_{FB} shift caused by high-k/SiO_2 interface dipole formation for different materials. (Right) Positive dipole shift observed for SiO_2/GeO_2 interface.

Materials

We explored HfO_2 and Al_2O_3 because they have been commonly used by SNF lab members. Moreover, some groups in EE412 of Fall 2010 developed stable recipes of HfO_2 and Al_2O_3 and studied their interface characteristics on Si and Ge substrates. This project extends their work and explores the characteristics of HfO_2 and Al_2O_3 films deposited by Savannah ALD on SiO_2 substrates.

Device fabrication

The device fabrication started from a highly doped Si substrate since it was used as one of the electrodes for probing. Savannah ALD is classified as a semi-clean tool, so the oxide growth step and foaming gas annealing (FGA) steps are limited by the clean or semi-clean tools. Thus, TEL PECVD and tylanfga furnace were chosen. The most important reason to choose TEL PECVD is due the thickness control of oxide layer. In fact, we tried tylan and thermco furnaces, but 50% deviation of thickness variation over the whole wafer was observed by using woollam ellipsometry when we intended to deposit the film thickness below 10nm. For example, 80nm was measured in the left of the wafer while 120nm was measured in the right after thermal oxidation. TEL PECVD solved this issue and provided excellent uniformity. It was also advantageous to use TEL as it keeps the backside of the substrate clean. If the oxide layer was grown by thermal furnaces such as the tylan or the thermco, etching the oxide in the back of the wafer would have been required before probing. Therefore, using TEL PECVD significantly simplified our processing flow. After 30-minute FGA, different High-K materials with different thicknesses were deposited in the Savanah ALD using standard recipes developed by the EE412 groups of Fall 2010. We decided to use Gryphon sputtering tool for the metal deposition step, considering the high demand of Innotec e-beam metal evaporation tool. However, in our last batch of device fabrication, we had no choice but use innotec due to unavailability of Gryphon (FGA furnace and Gryphon were unavailable during the last few weeks of the quarter.) Finally the standard lithography and Al etching are employed to complete the device structure. Our initial plan was to etch through the oxide and define the capacitor area more rigorously. After

discussion we realized this was unnecessary. The revised fabrication process is summarized in Fig. 2. Since all the machines enabled us to control the thickness of films accurately, our CV curves overlap perfectly without variation (Fig. 3).

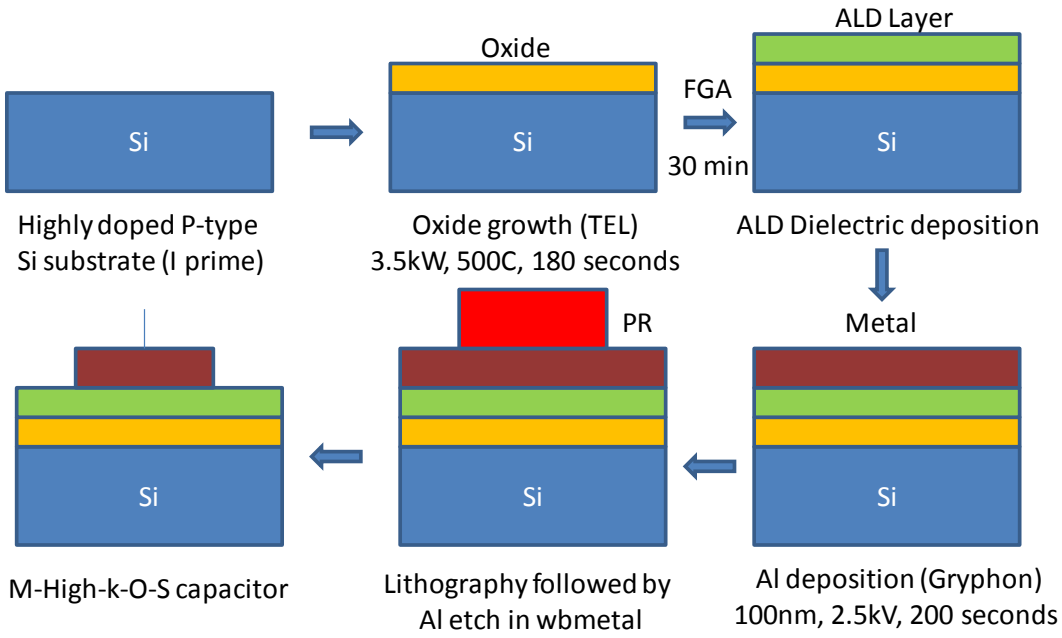


Figure 2: Revised process flow for the MOSCAP device structures

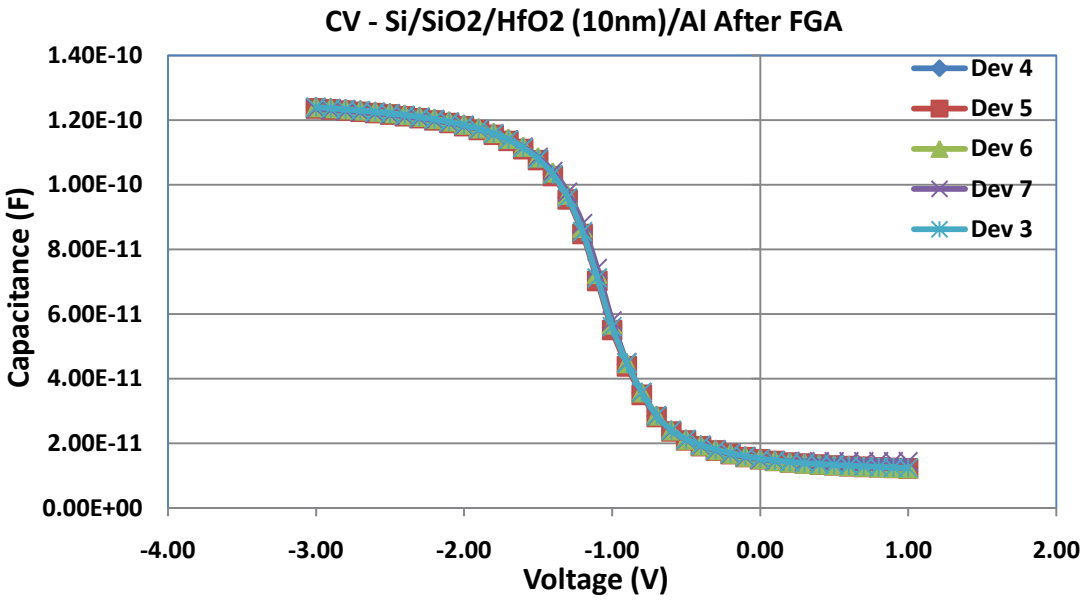


Figure 3: Perfectly overlapped CV curves of arbitrary five devices (from the same wafer) use TEL PECVD, Savannah ALD, and Gryphon metal sputtering system.

Measurements & Setup

The CV measurements were performed in the cascade probing station using the LRC meter in the Test Room (CIS152). Before each measurement session the LCR meter was calibrated and data collection was controlled by National Instruments Labview program which allowed us to control the sweeping speed and data sampling. Before each session the following methodology was followed to obtain data in a consistent fashion.

1. The LCR meter was calibrated using "short" and "open" connections.
2. The bias voltage was swept from the inversion to the accumulation and back to inversion. (This minimizes the error of data obtained in the inversion region due to depletion.)
3. Data was obtained for three frequencies of 1KHz, 100KHz & 1MHz.
4. The bias voltage step was maintained at 0.5V. This value can be changed depending on the need to obtain higher resolution CV curves.
5. The delay between data points was set to 0.5 seconds.

The LCR meter provides the measured data for both capacitance and conductance values. It assumes a model where a capacitor is in parallel with a resistor as provided on the right hand side of figure 4. However in reality the model actually has an extra resistor introduced by the connection lines. Thus the measured value deviated slightly from the real capacitance and depends on the frequency. If the MOSCAP is too leaky, the Gins becomes larger and the measured capacitance will be larger than the expected value from effective oxide thickness (EOT) calculation according to equation 1.

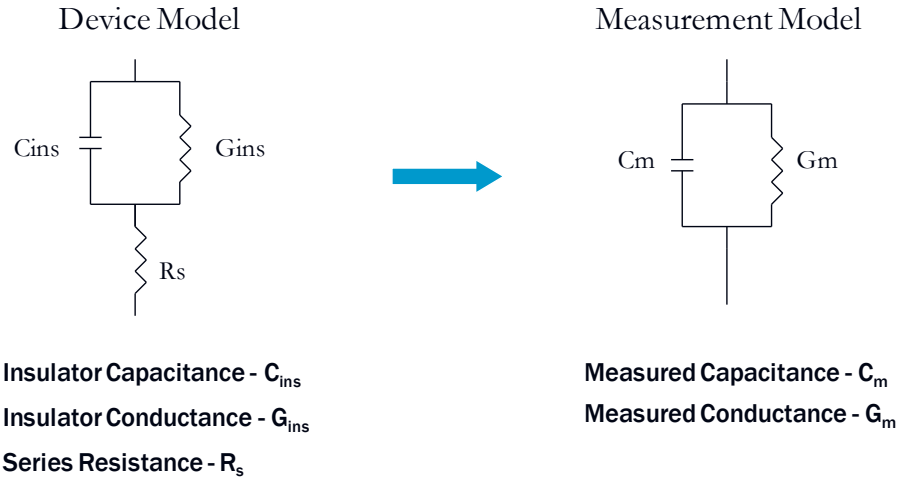


Figure 4: The device model (left) and the measurement model assumed by LCR meter (right)

$$t_{eff} = t_{ox} + \left(\frac{K_{ox}}{K_{high-K}} \right) t_{phy} \qquad \text{--(1)}$$

Since we always knew the thickness and the dielectric constant we could always calculate the EOT and the expected capacitance in accumulation. This way we could avoid measurements of leaky capacitors.

Results & Data

The CV curves of SiO_2 MOSCAPs are shown in figure 3. These curves overlap very well and show negligible hysteresis due to mobile ions. Thus, like in most CV studies in literature we didn't perform an error analysis for those structures.

The MOSCAPs were then fabricated with an additional layer of Al_2O_3 on top of SiO_2. We fabricated devices with three different thicknesses for each material: 50 cycles, 75 cycles and 100 cycles. Figure 5 shows the CV curves of the SiO_2 MOSCAP (reference curve) and the corresponding CV curves with Al_2O_3 for different thicknesses after FGA400 anneal. The curves from the same wafers overlap on top of each other very well. Thus we plot only one device from each wafer in figure 5. In this experiment we obtained a voltage shift of +0.6V due to dipole charge and an average -0.1V shift per every 25 cycles due to the fixed charge after forming gas anneal.

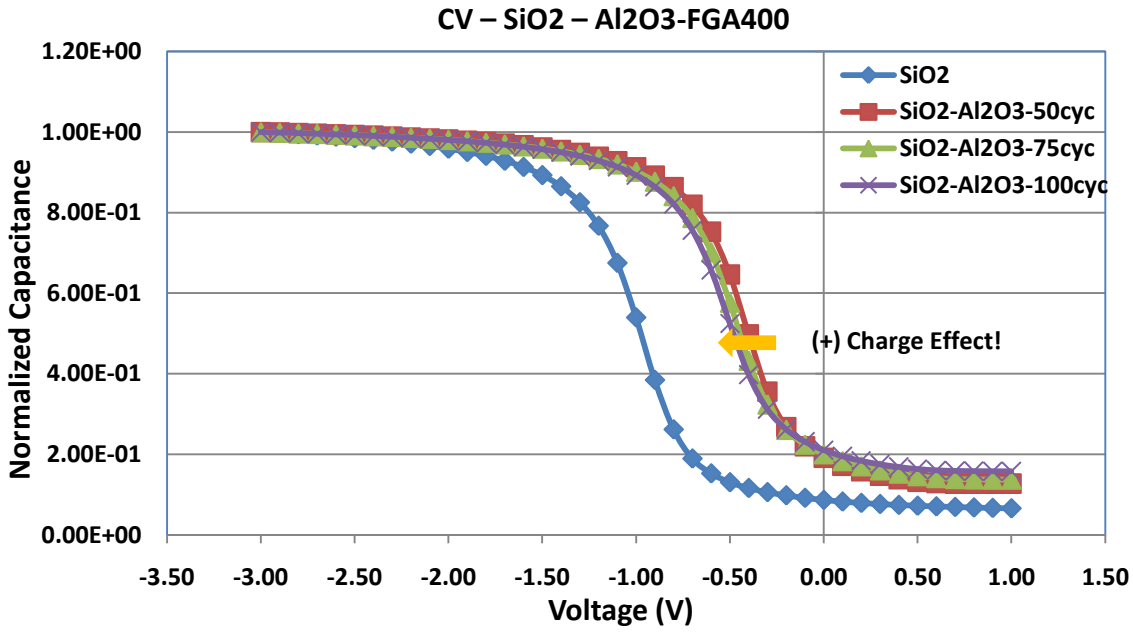


Figure 5: The shifts in the CV curves arise due to different charges at the interface. The major positive shift arises from the SiO_2/Al_2O_3 surface. The secondary negative shifts that depend on ALD thickness arise from the positive fixed charges after FGA anneal.

The same experiment (for the same set of cycles - 50, 75, 100) was repeated for HfO_2 where we obtained similar trends in CV curves (not shown here). Thus in our analysis we could extract the charge density values for both Al_2O_3 and HfO_2. Since we also wanted to study the effects of forming gas annealing conditions on charge density, we repeated this experiment for forming gas anneal at 300C. Furthermore, we also prepared samples without any forming gas anneal as well. In summary, we have extracted and compared the interface charge density for both Al_2O_3 and HfO_2 under following three conditions.

a) Intrinsic charge density at the SiO_2/High-k interface without any forming gas anneals.
b) Forming gas anneals at 300C.
c) Forming gas anneals at 400C.

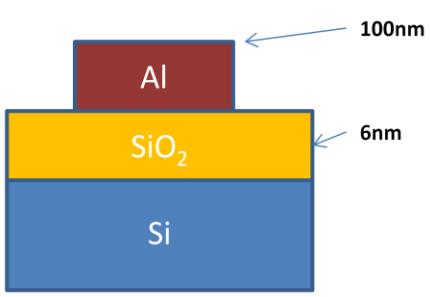
Analysis

The very first task was to extract the charge density at the Si/SiO_2 interface. The ideal flatband voltage is the metal to semiconductor work function difference. Any deviation from this value is a result of charges at the Si/SiO_2 interface according to equation 2 [5], [6], [7]. Thus we extracted the Si/SiO_2 interface charge densities from SiO_2 MOSCAPs using the shift from the ideal CV curve as shown in Table 1.

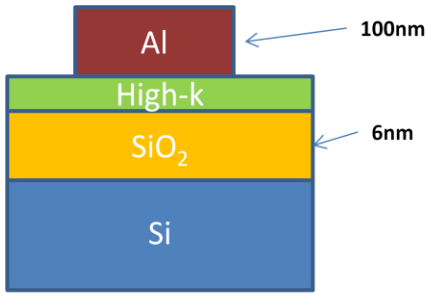
	No FGA (/cm^2)	After FGA (/cm^2)
Si/SiO2	6x10^{11}	3x10^{11}

Table 1: Extracted charge densities for Si/SiO_2 interface for MOSCAPs fabricated using TEL

Our second goal was to extract the charge density between SiO_2/high-k interface. We considered similar capacitive structures with high-k layers on top of SiO_2 layers as shown in Fig 6.



V_{fb} – Measured Flat band



V'_{fb} – Measured Flat band

$$Q_{SiO_2} = C_{SiO_2}\left[\frac{\phi_{MS}}{q} - V_{FB}\right] \quad \text{--(2)}$$

$$Q_{HfO_2} = C_{HfO_2}\left[\frac{\phi_{MS}}{q} - V'_{FB} - \left(\frac{1}{C_{SiO_2}} + \frac{1}{C_{HfO_2}}\right) Q_{SiO_2}\right] \quad \text{--(3)}$$

Figure 6. (Left) MOS Capacitor with SiO_2 as the gate dielectric. (Right) Capacitor structure with both SiO_2 & High-k as gate dielectric. The equations describe the V_{fb} shift due to charges at the interface for respective devices.

Once the high-k layer is introduced, a new secondary sheet of charge will form at the SiO_2/high-k interface. The new faltband voltage can be expressed using equation 3 [8]. Once equation 2 & 3 are combined and rearranged, we can obtain an expression as shown in equation 4, which clearly indicates how the shift depends on the thickness of the high-k layer. We further modified this equation to account for the constant shift caused by the interface dipole charge. Then we extracted the flatband voltage shift for several different dielectric thicknesses and plotted this voltage shift with respect to thickness.

$$V_{fb-Highk} - V_{fb-SiO2} = -\left(\frac{Q_{SiO2} + Q_{High-k}}{\varepsilon_o \varepsilon_{High-k}}\right) \times t_{High-k} + V_{Dipole\_Shift} \quad \text{-----(4)}$$

Our CV curves (Fig. 5) clearly indicate the large positive shifts from the dipole charge. The small negative shifts we observe in Fig 5 arise from the positive charge at the interface. The mathematical equivalent for equation 4 is shown in Fig. 7 where the flat band voltage shift is plotted against the thickness of the ALD layer.

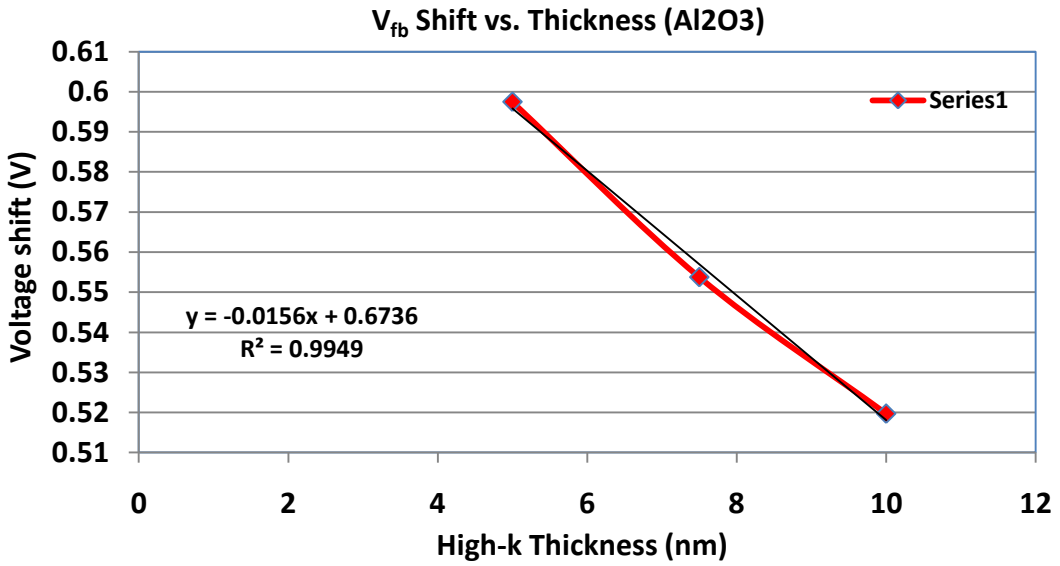


Figure 7: The flatband voltage shift vs. thickness of Al_2O_3 for FGA400 sample. The interface charge density was extracted from the gradient and the dipole shift is the intercept. Data corresponds to the CV curves in Fig. 5.

The charge density was then calculated from the gradient of those curves. The intercept provides the dipole shift due to areal oxygen density difference at the interface. We extracted those values for both the both FGA300 and FGA400 samples for comparison. These values provided in Tables 2, 3 & 4 are very well in agreement with the values we found in literature.

Material	Dipole Shift (V)
Al_2O_3	0.6
HfO_2	0.4

Table 2: Extracted dipole shift from intercept

Non-FGA samples

Material	Charge Density (cm^{-2})
Al_2O_3	$1.2x10^{13}$
HfO_2	$1.6x10^{13}$

Table 3: Charge density for Non-FGA

FGA Samples

Material	FGA300 (cm^{-2})	FGA400 (cm^{-2})
Al_2O_3	$9.6x10^{11}$	$3.4x10^{11}$
HfO_2	$3.5x10^{11}$	$1.2x10^{12}$

Table 4: Charge density for FGA samples

Discussion

The charge density of Si/SiO_2 interface obtained from TEL tool was $6x10^{11}cm^{-2}$. Even after forming gas anneal the charge density did not change much which indicates that TEL tool provides high quality oxide that minimizes the interface charge.

On the contrary, after high-k layer deposition we did observe large negative shifts (~1V per 50cycle) due to interface trap charge and fixed charge. The extracted values for both HfO_2 and Al_2O_3 are in the order of 10^{13} cm^{-2} that agree very well with literature [3] for non-forming gas annealed samples. After forming gas anneal, however, this charge density reduced by two orders of magnitude removing most of the trap charge. Then the dipole charges became the dominant charge and the curves shifted to the right by a constant voltage that depended on the material. The FGA anneal however did not remove the fixed charge completely, which gave rise to a small negative shift in the CV curves with the increase in thickness.

The FGA400 samples proved to be more effective than the FGA300 samples for Al_2O_3 samples. The FGA recipe consists of 95% H_2 and 5% N_2. The higher temperature the higher is the diffusion coefficient for hydrogen which allows it to travel through the high-k layers to negate the trap sites. Thus we expect a lower charge density for FGA400 samples. For HfO_2 samples, the extracted value seemed to be higher than usual and such errors can be introduced to our analysis due to several reasons.

1. The CV curves being unusually close to each other make it difficult to extract the flat band voltage shift.
2. The mobile ions can introduce small amounts of hysteresis in CV curves.
3. The charge density is calculated assuming fixed dielectric constant values for high-k layers (7.5 for Al_2O_3 and 16 for HfO_2). These values may vary under process conditions such as deposition temperature, humidity, annealing conditions etc.

Accounting for such errors can be a study of its own. In our calculations we tried to minimize the error introduced by the above mentioned factors. For example, we utilized a MATLAB program to extract the flatband voltage values in a consistant manner, and minimized hysteresis by using clean and semi-clean tools in our processes. However, despite robust process flow development there is still room for improvement in data analysis and computation of charge density. In terms of material study, a large number of high-k materials have yet to be characterized using the techniques we developed this quarter. In addition our work can be thought of as a stepping stone for any future on cross contamination study which will be a great contribution to the SNF community. We hope future EE412 students will continue and extend our work to characterize new, different dielectric materials and serve this purpose for many years to come.

Acknowledgements

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