Low temperature bonding for neural implant fabrication

Team members

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Mentors

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Phil Barth

Faculty advisor

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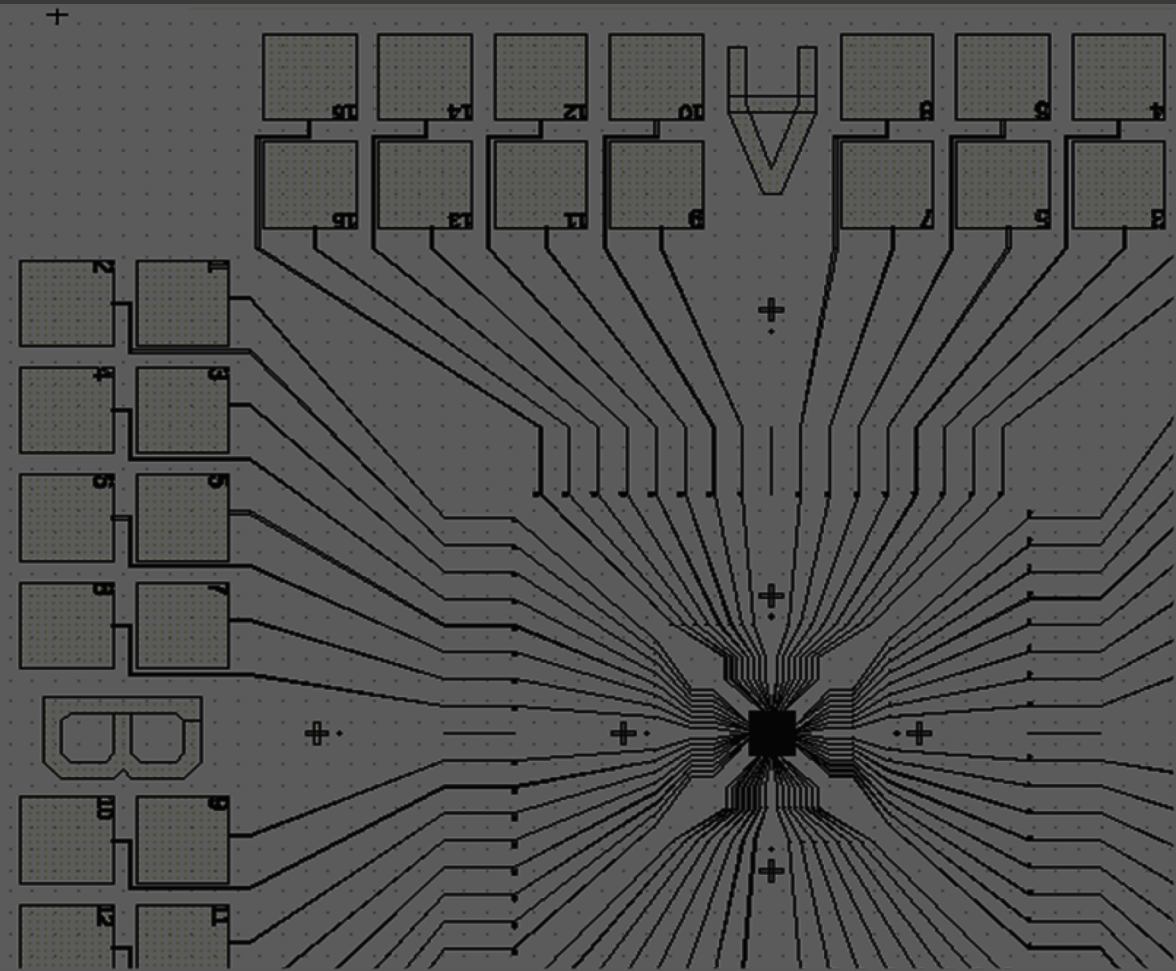
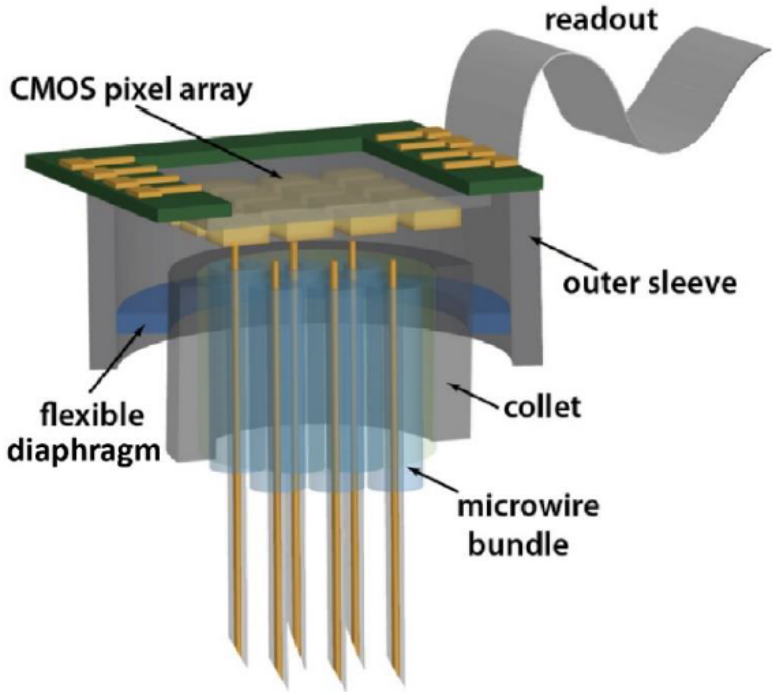


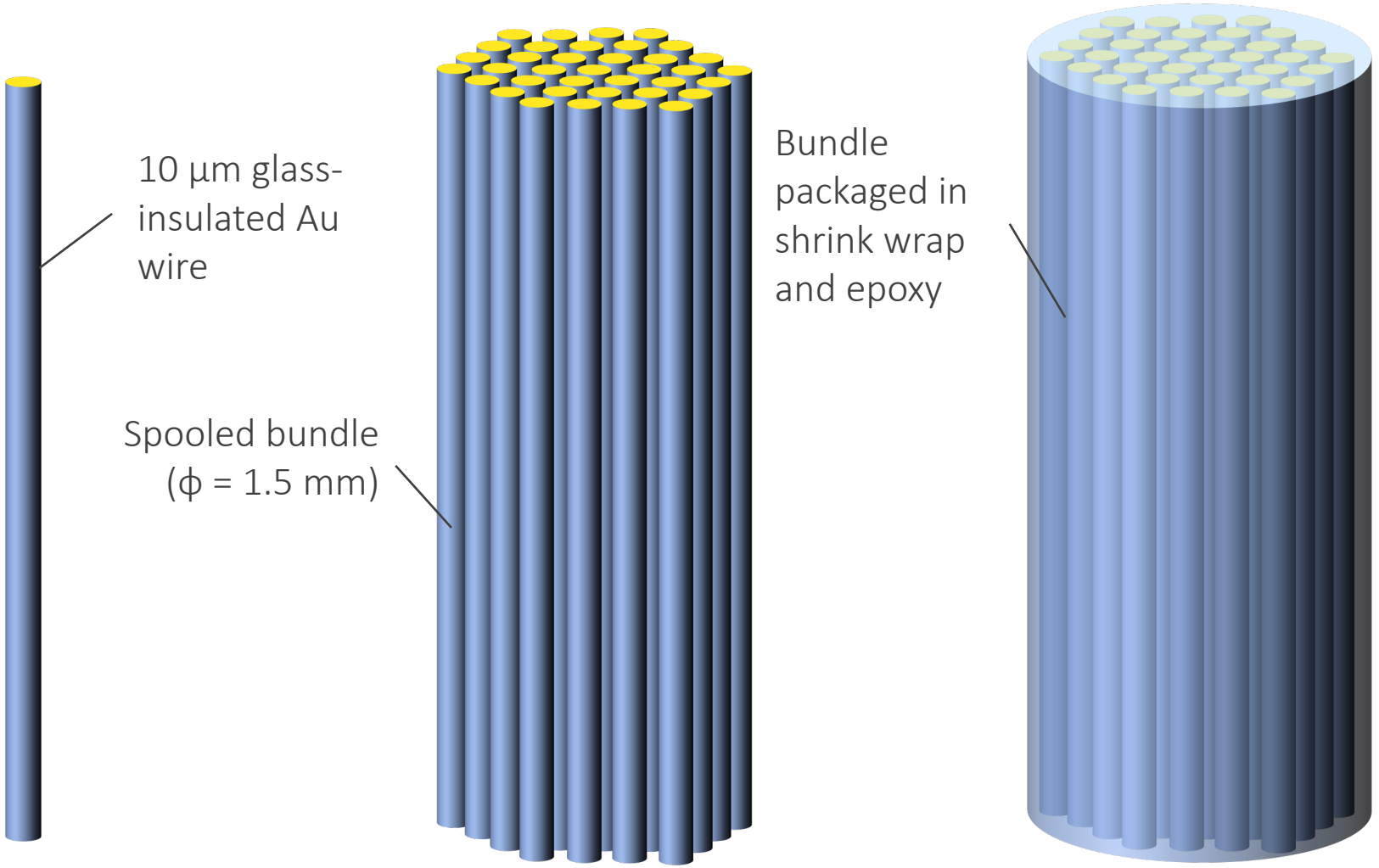
Motivation

- Implantable neural interfacing devices
  - Therapeutic devices for neurological disorder
  - Tools for studying neurological circuits
- Massively parallel microelectrode array for neural implant
  - Microelectrode-CMOS interface
  - Solder bonding for mechanical stability and ohmic contact

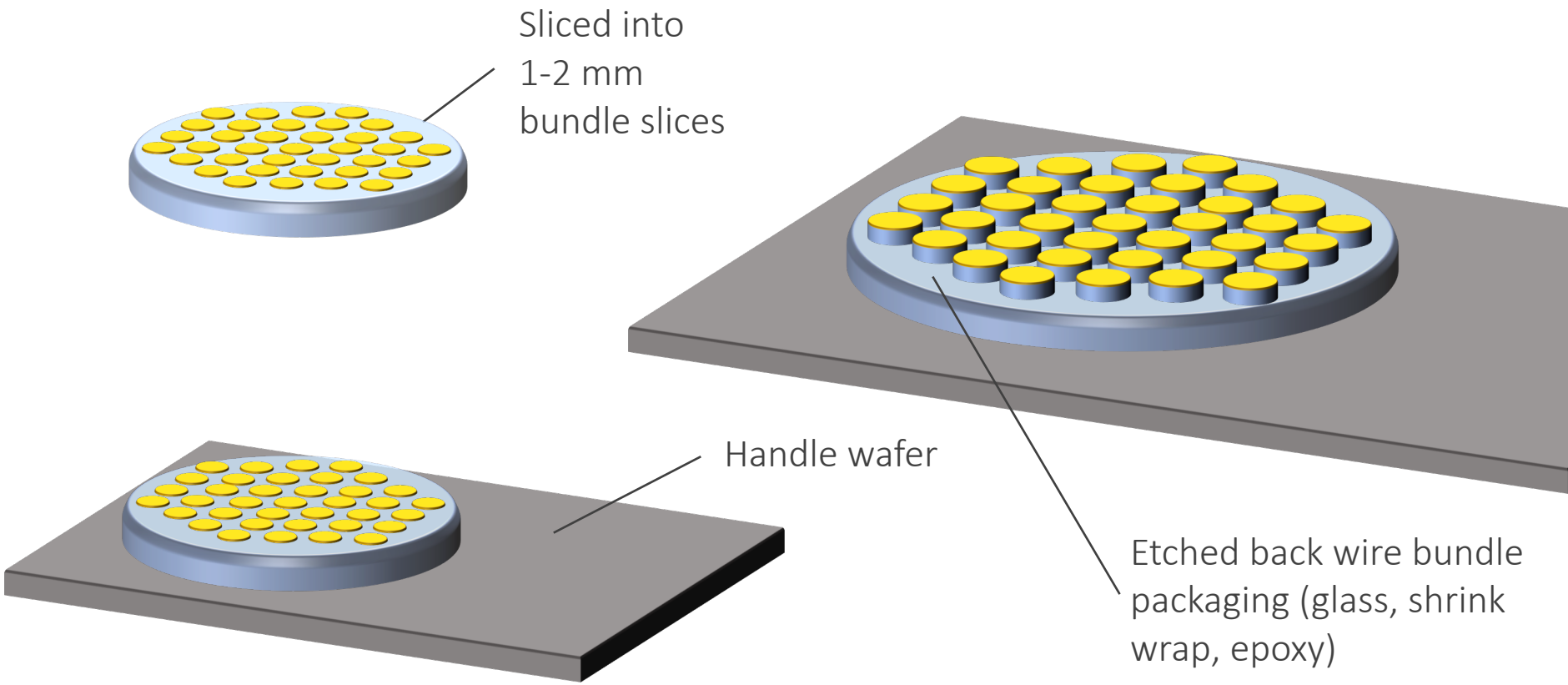


Rivnay, J., Wang, H., Fenno, L., Deisseroth, K. & Malliaras, G. G. Next-generation probes, particles, and proteins for neural interfacing. Sci. Adv. 3, e1601649 (2017)
M.-E. Hanna, "A scalable, practical approach to neural modulation & recording," Stanford University, 2018.

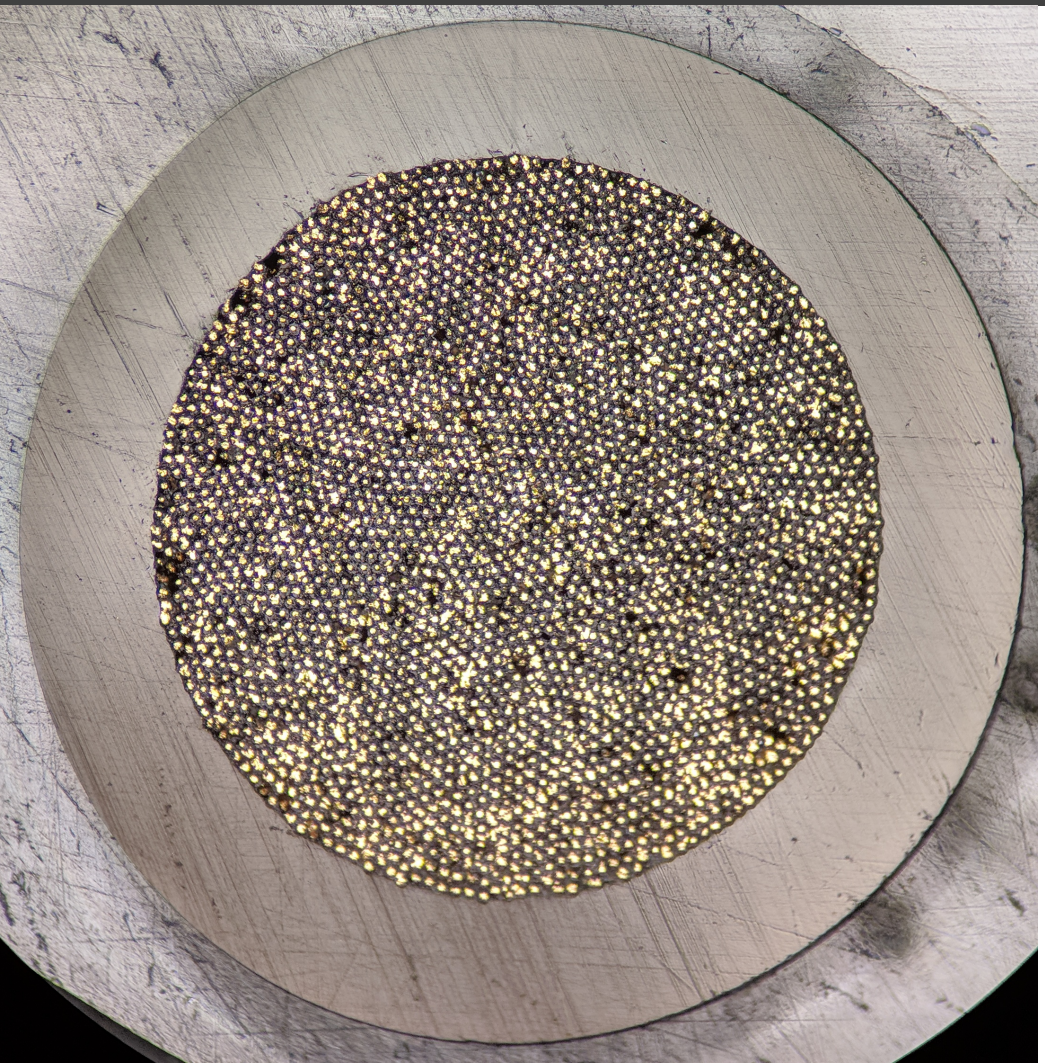
Bundle slice fabrication



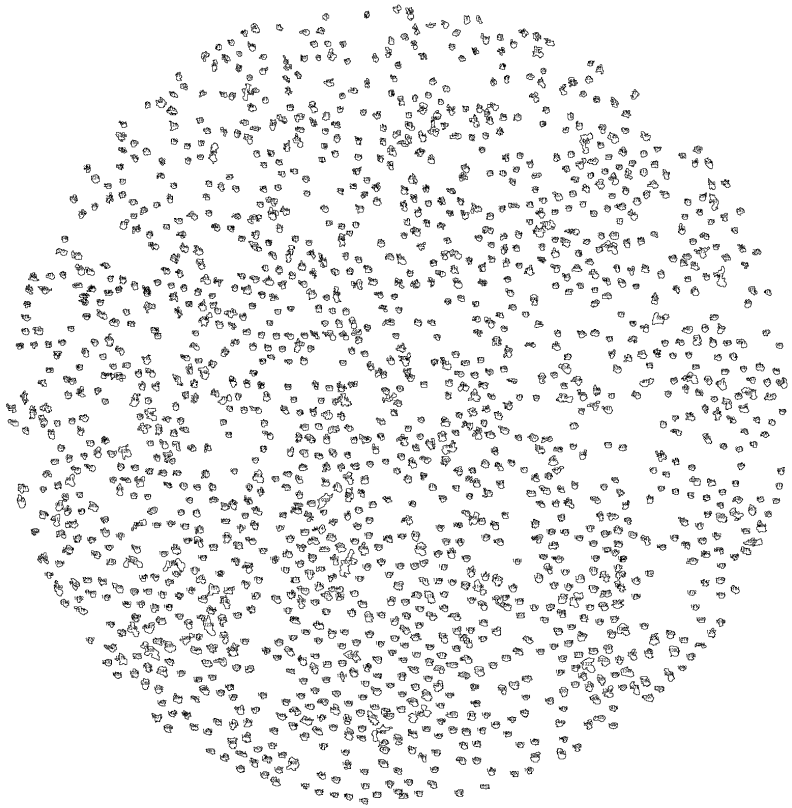
Bundle slice fabrication



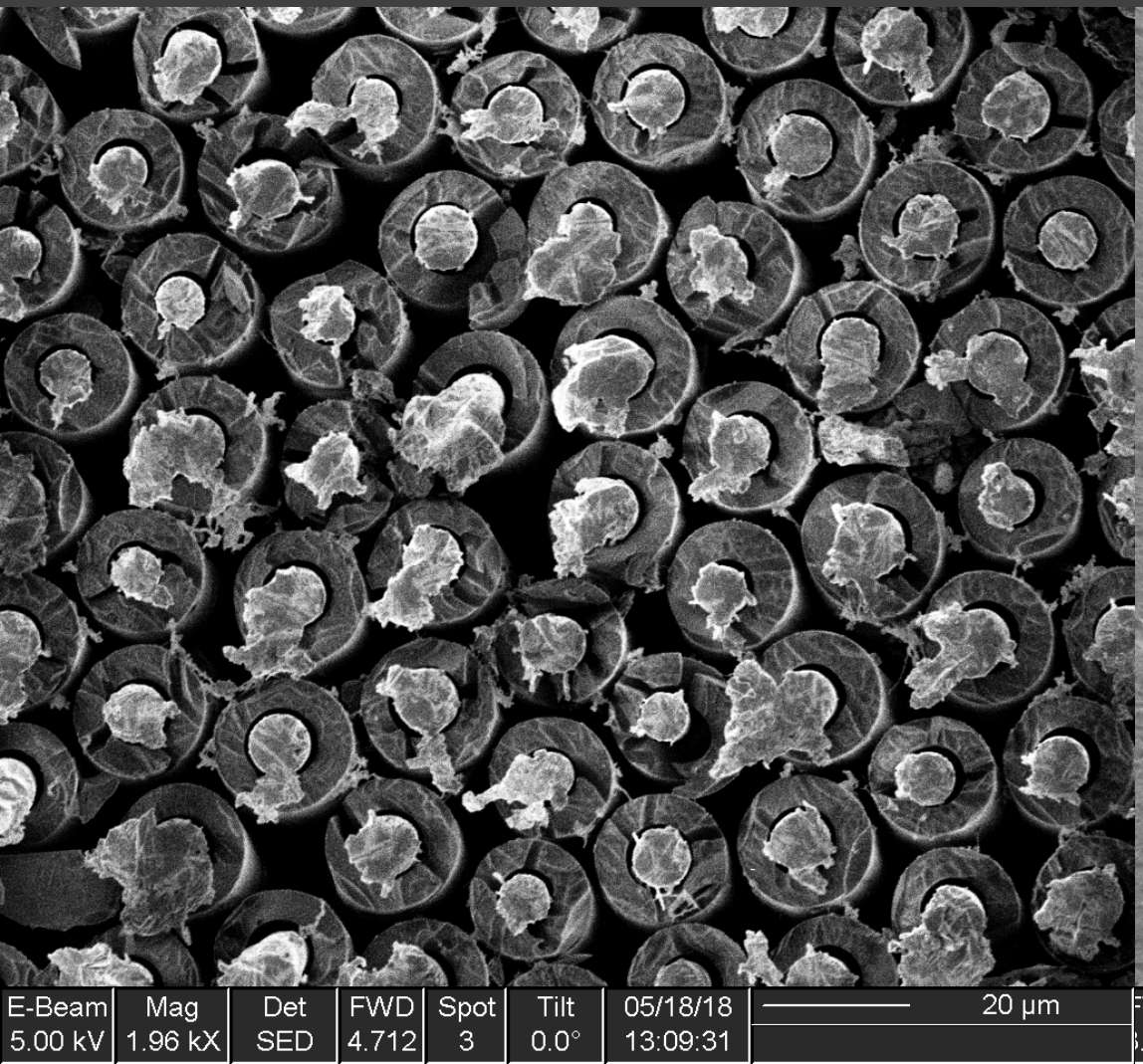
Bundle slice fabrication



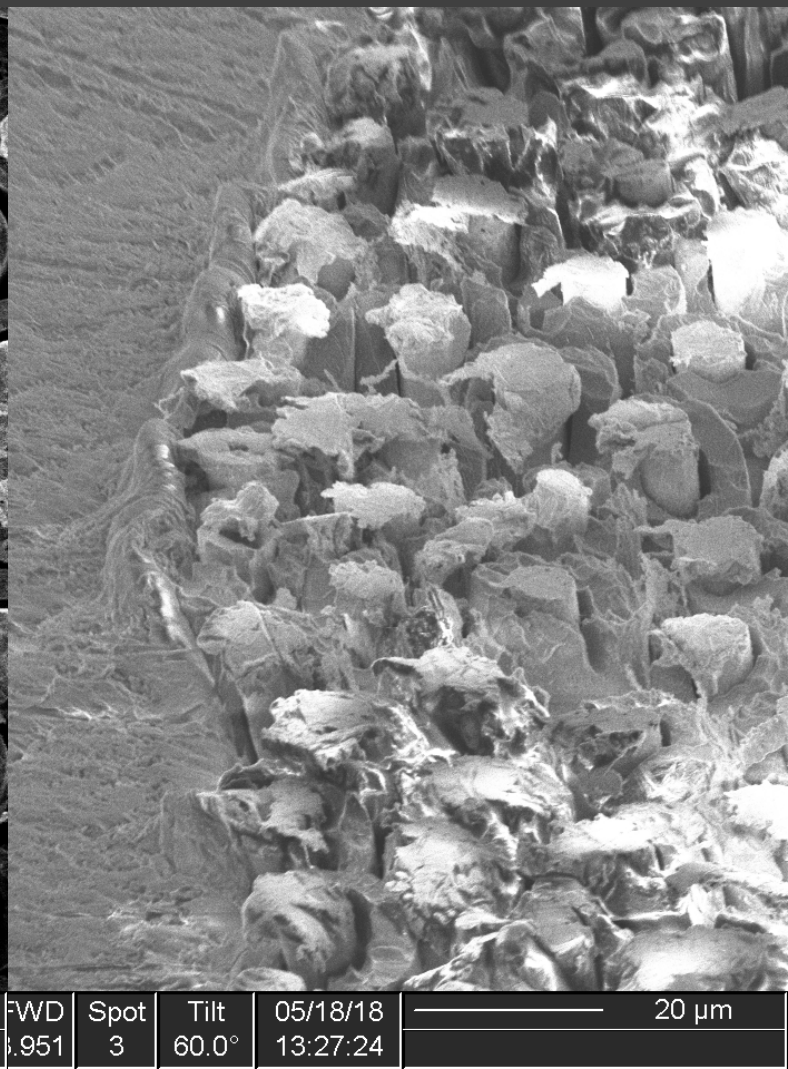
Counted: 1.5k Wires
for 1.5 mm bundle



Bundle slice fabrication



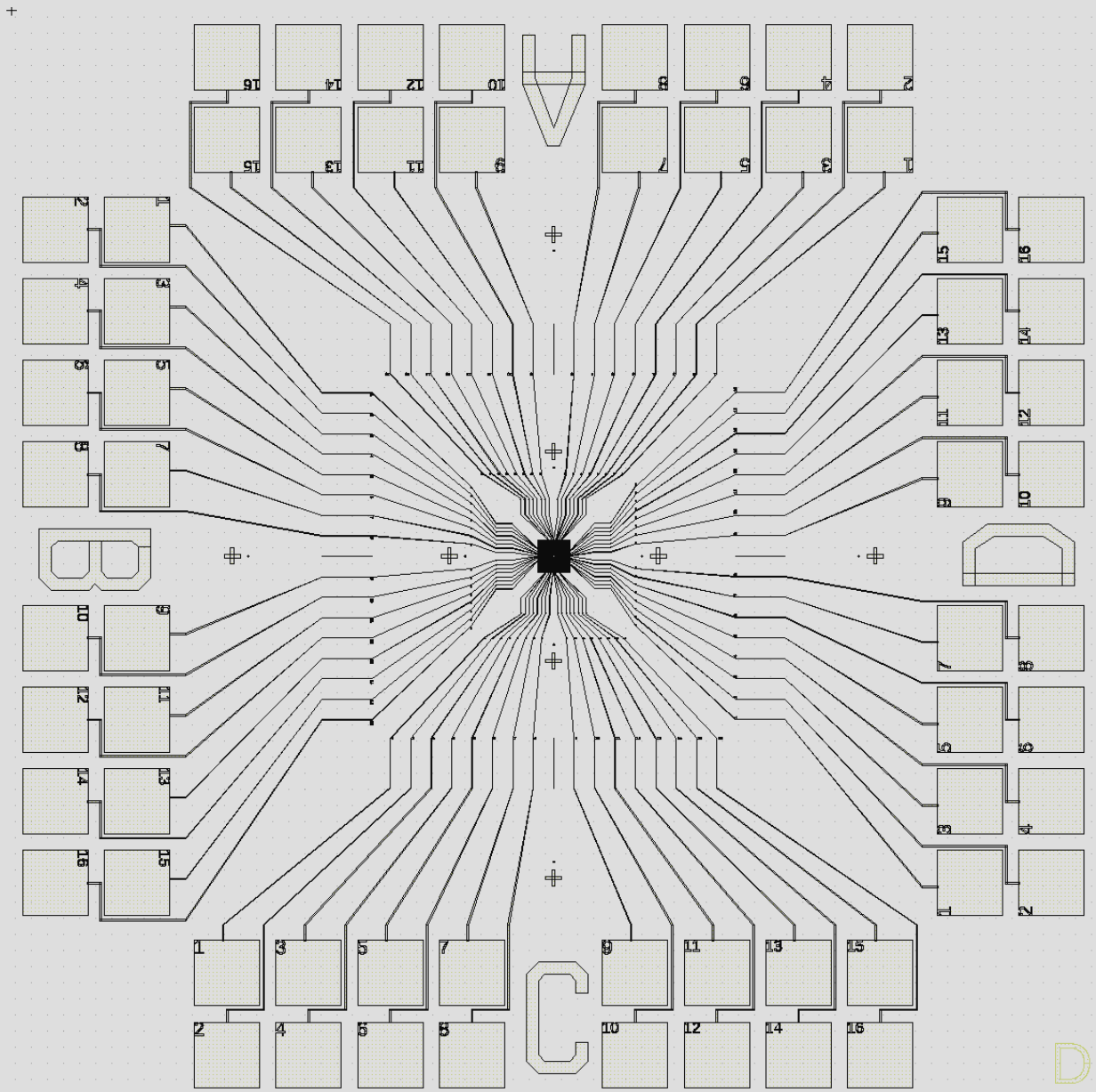
E-Beam	Mag	Det	FWD	Spot	Tilt	05/18/18	20 µm
5.00 kV	1.96 kX	SED	4.712	3	0.0°	13:09:31	



FWD	Spot	Tilt	05/18/18	20 µm
.951	3	60.0°	13:27:24	

Test chip fabrication

- Electrical connection circuit
- Passivation
- Solder patterning



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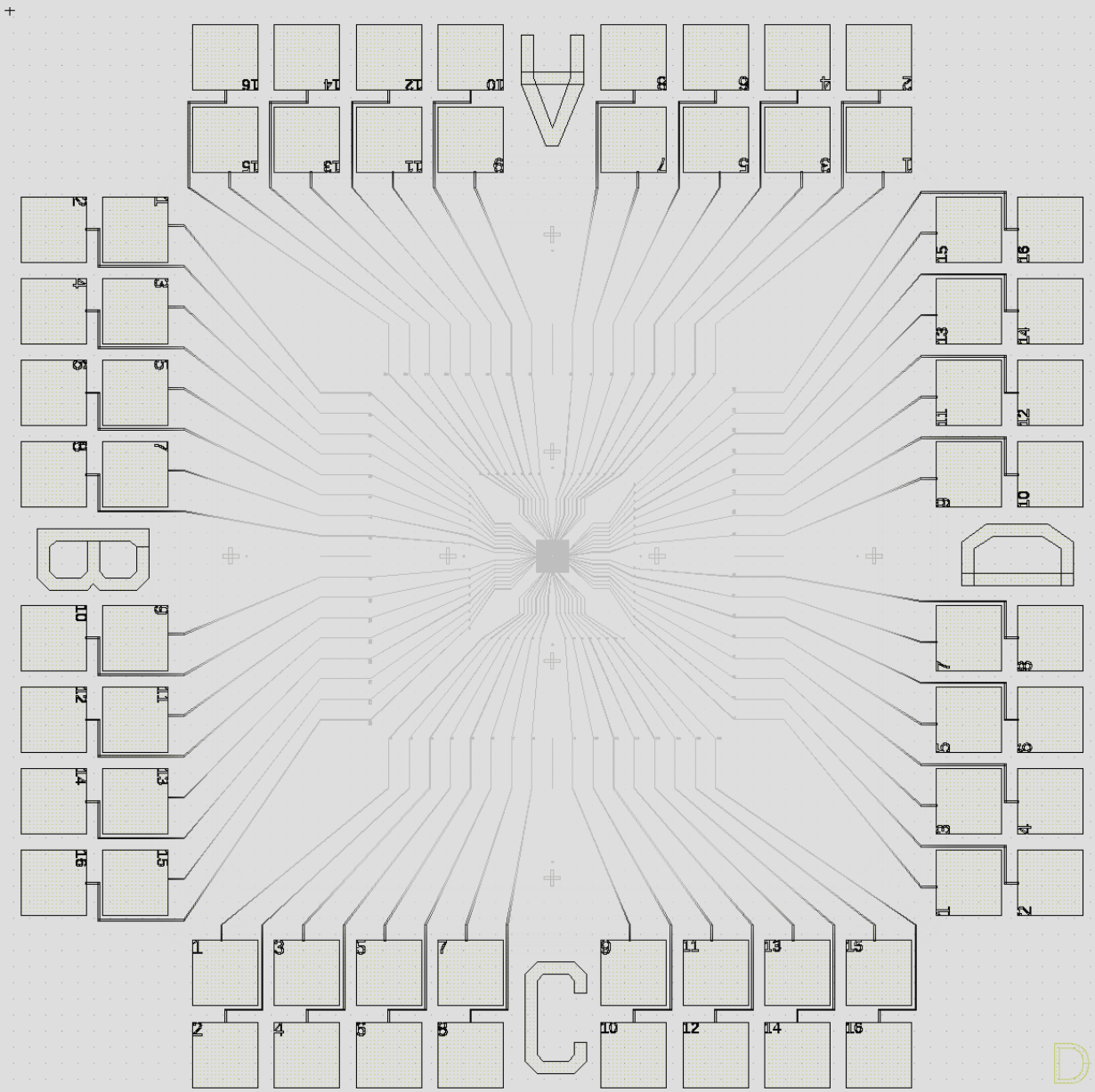
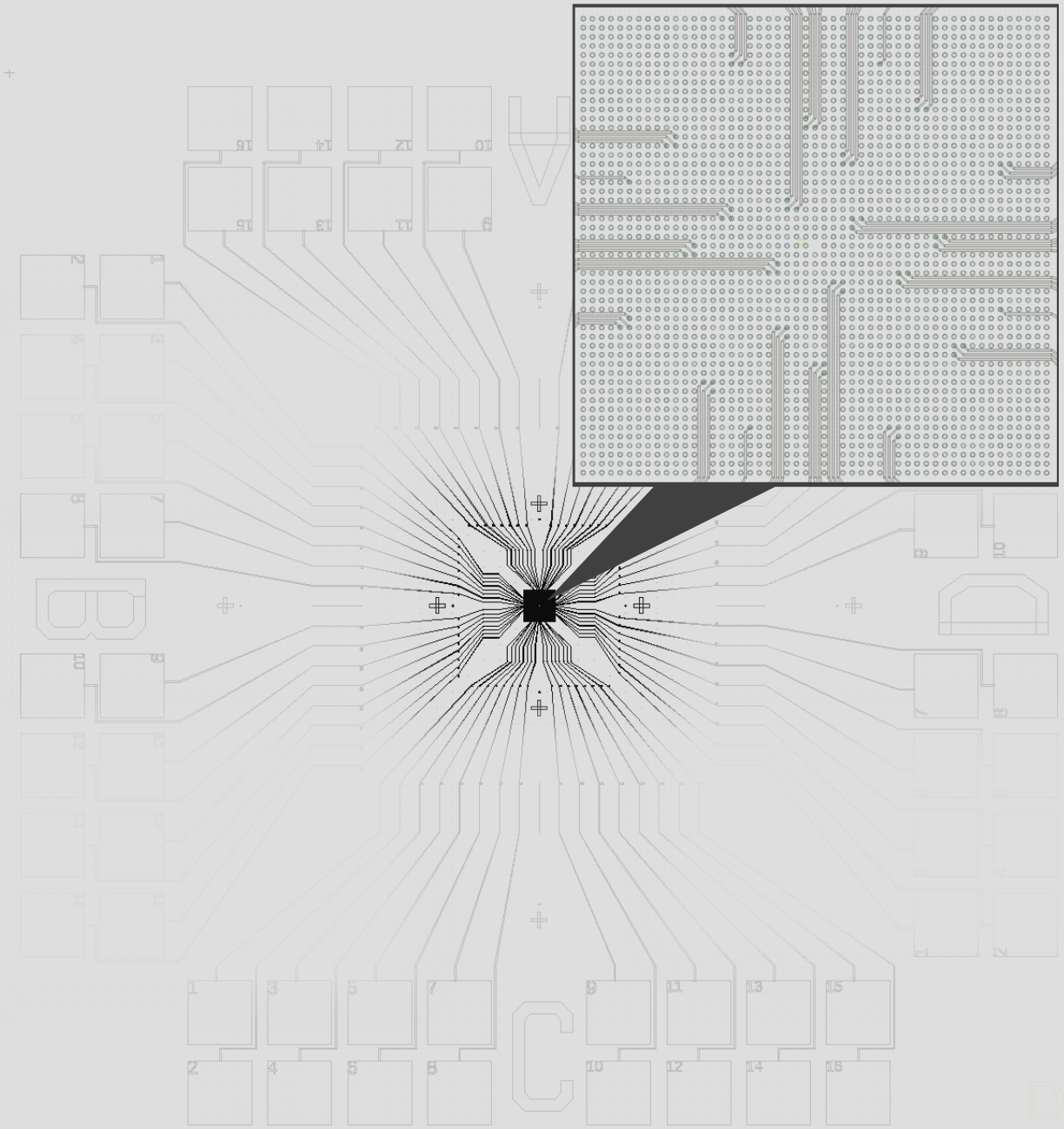


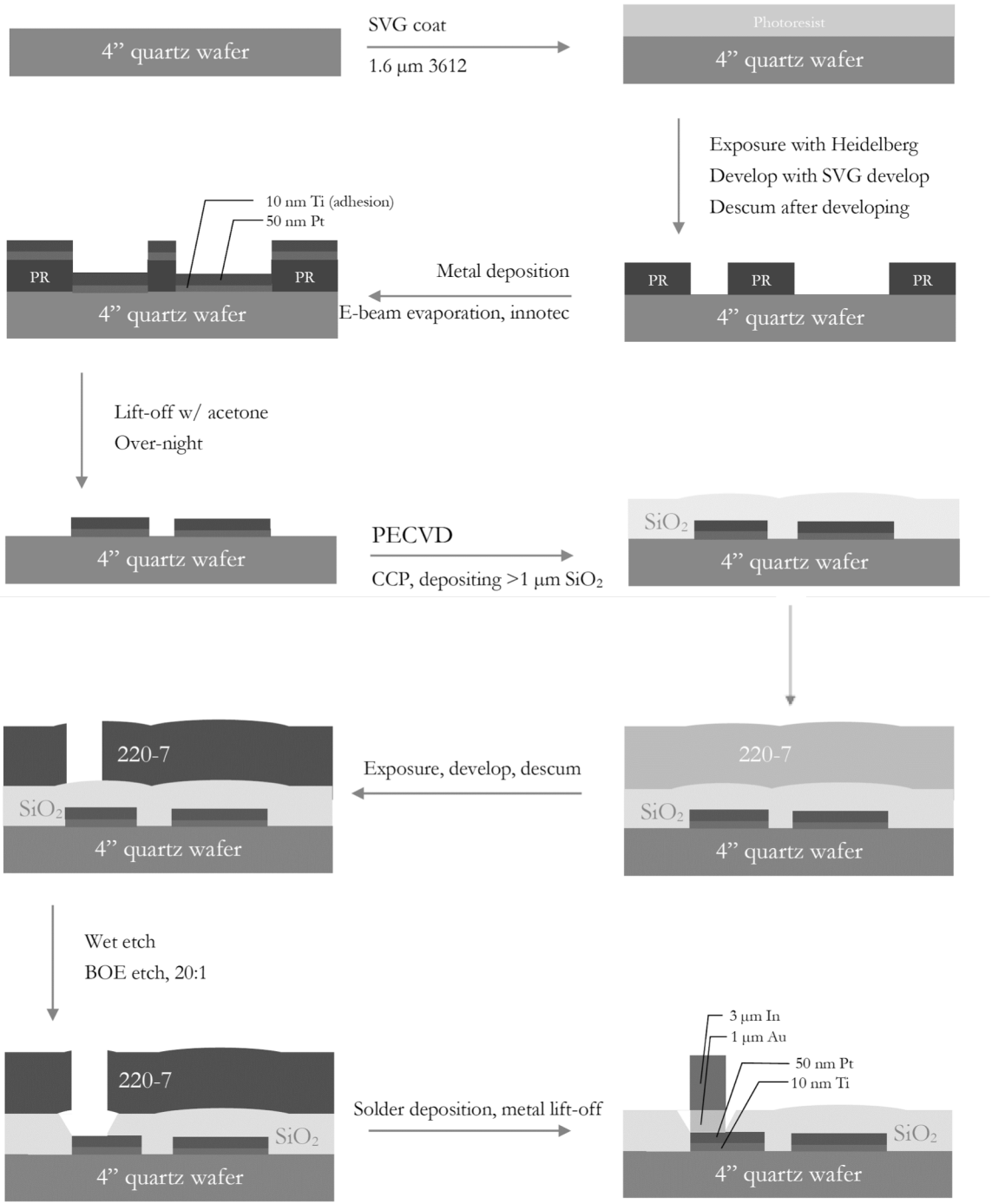
Test chip fabrication

- Electrical connection circuit
- Passivation
- Solder patterning

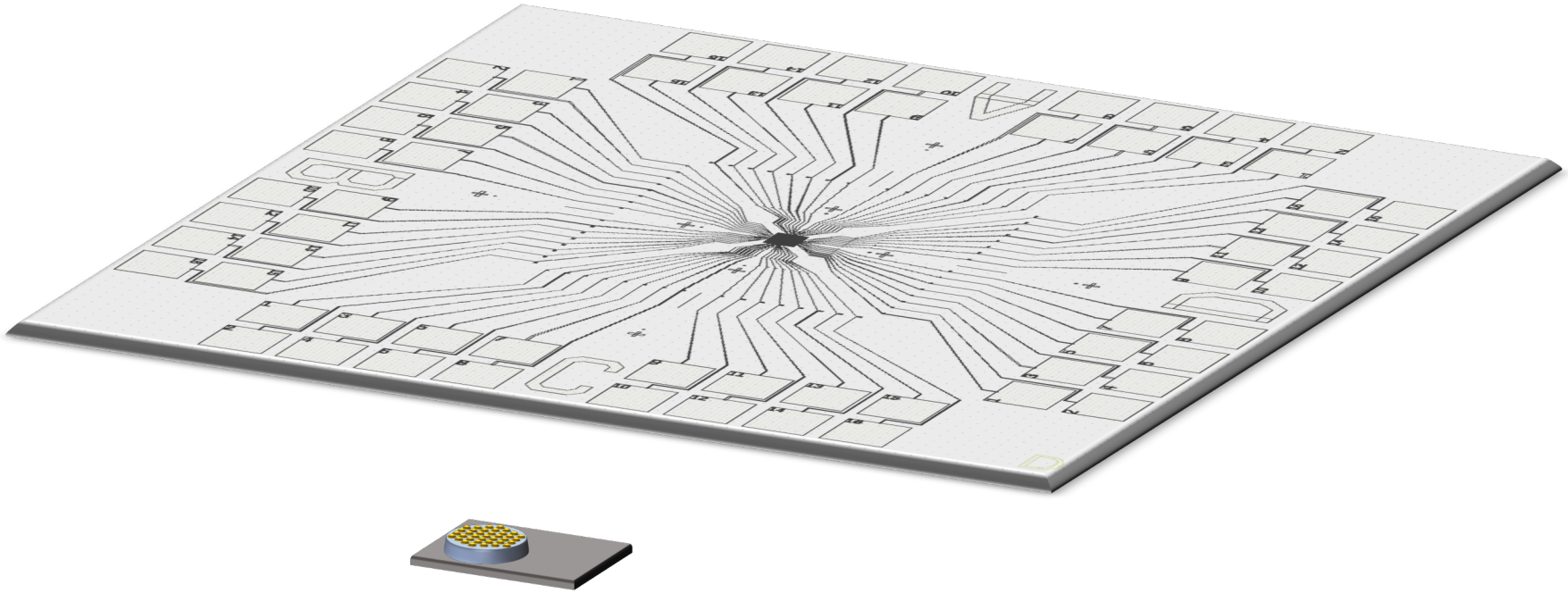


Test chip fabrication

- Electrical connection circuit
- Passivation
- Solder (5 µm In) patterning

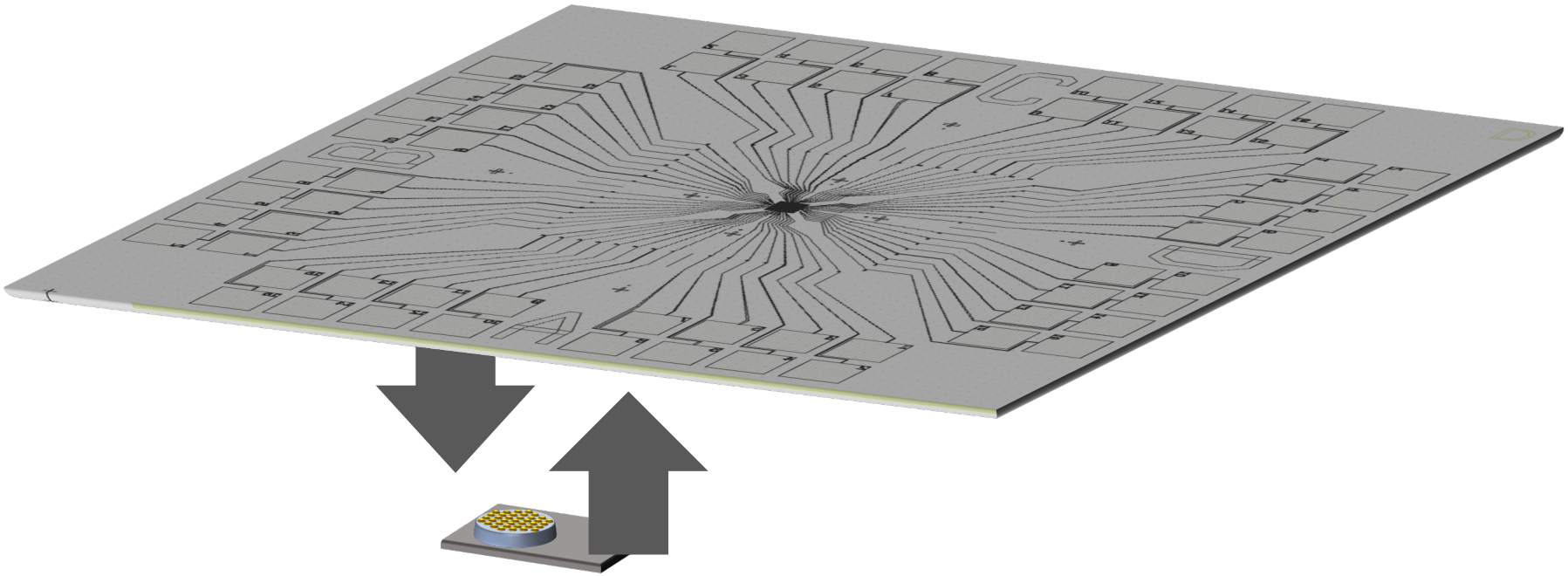


Bonding on Flipchip bonder

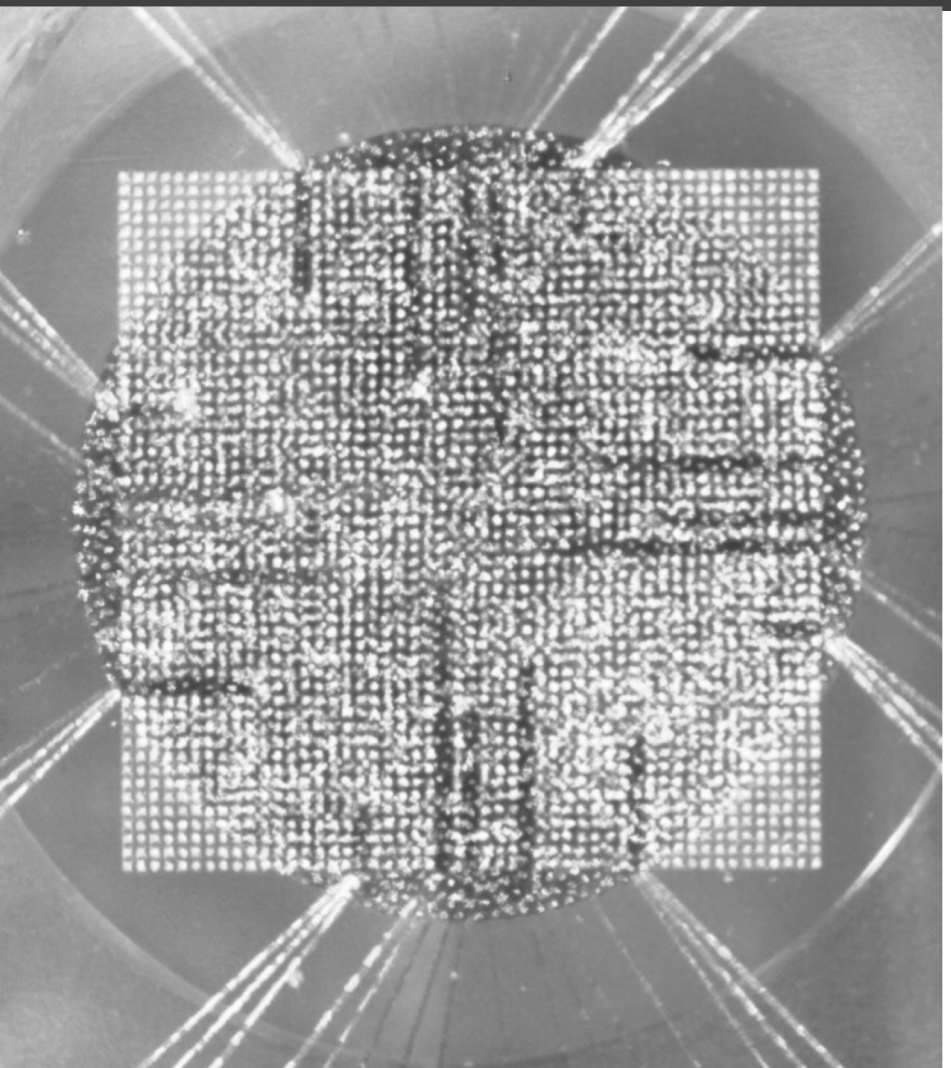


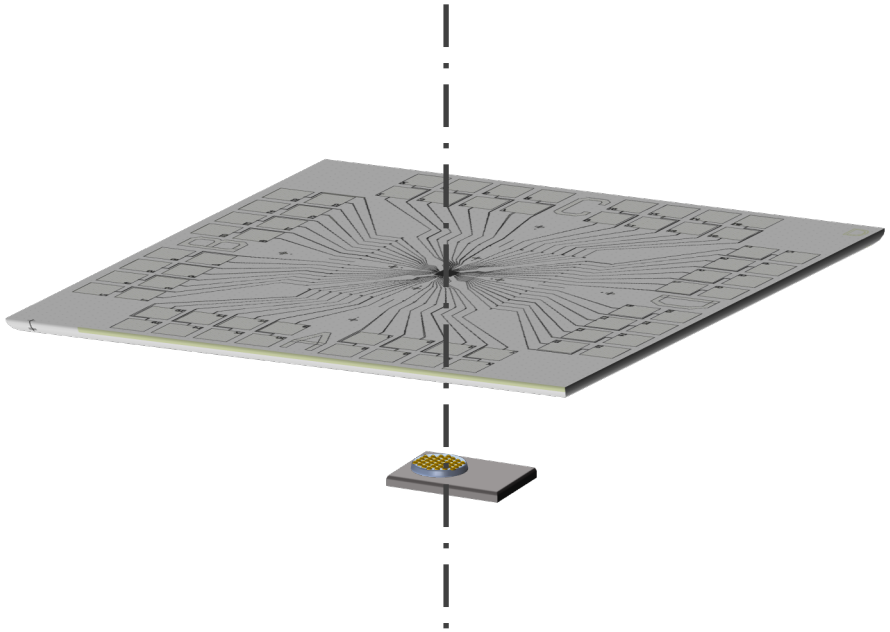
Bonding on Flipchip bonder

Mount to Flipchip arm upside down

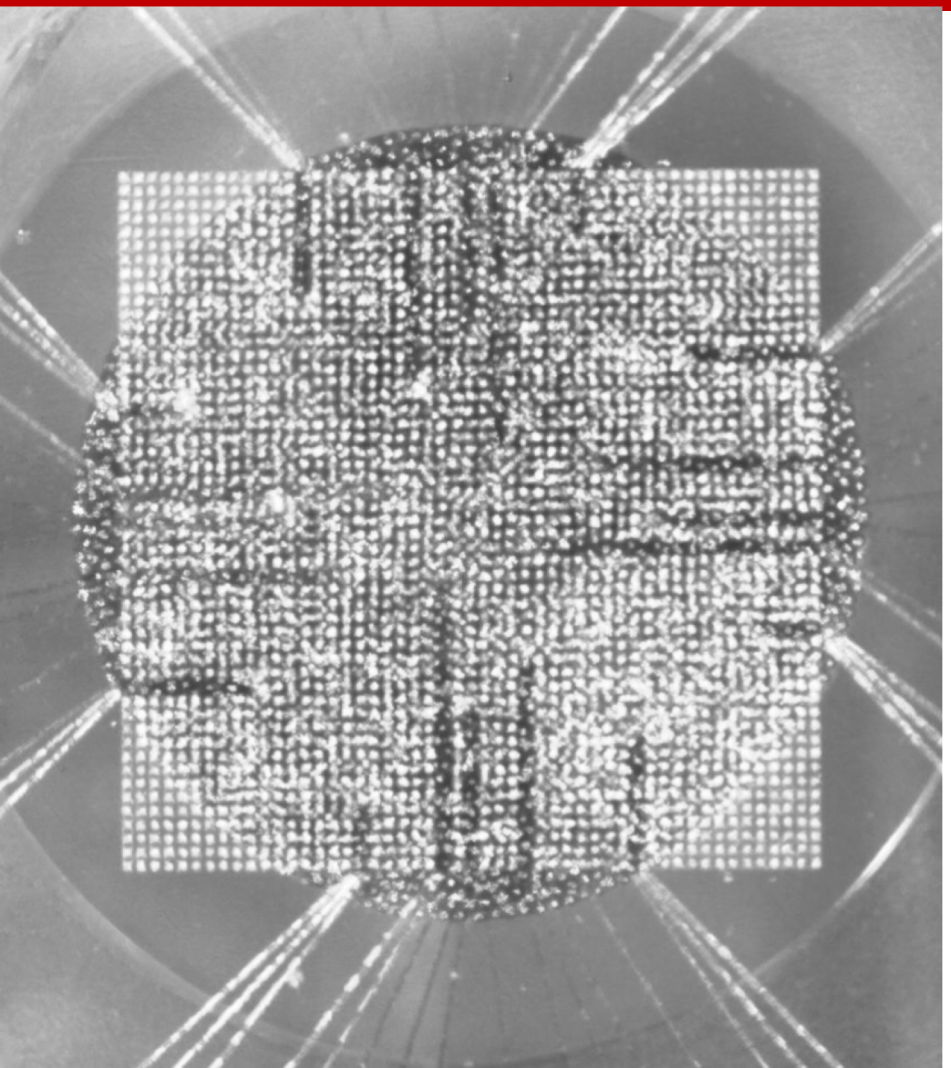


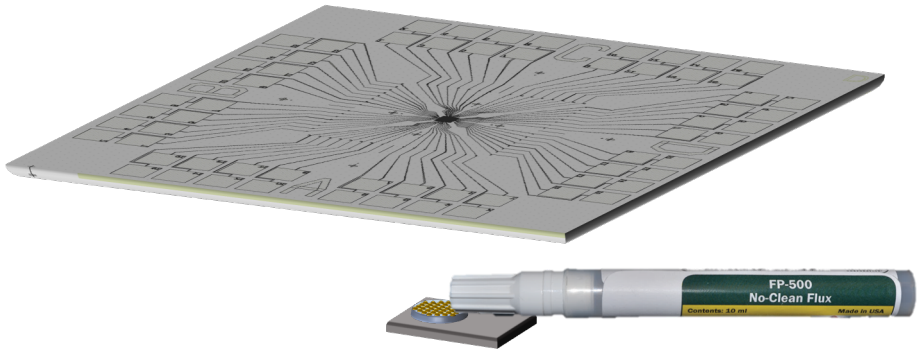
Bonding on Flipchip bonder



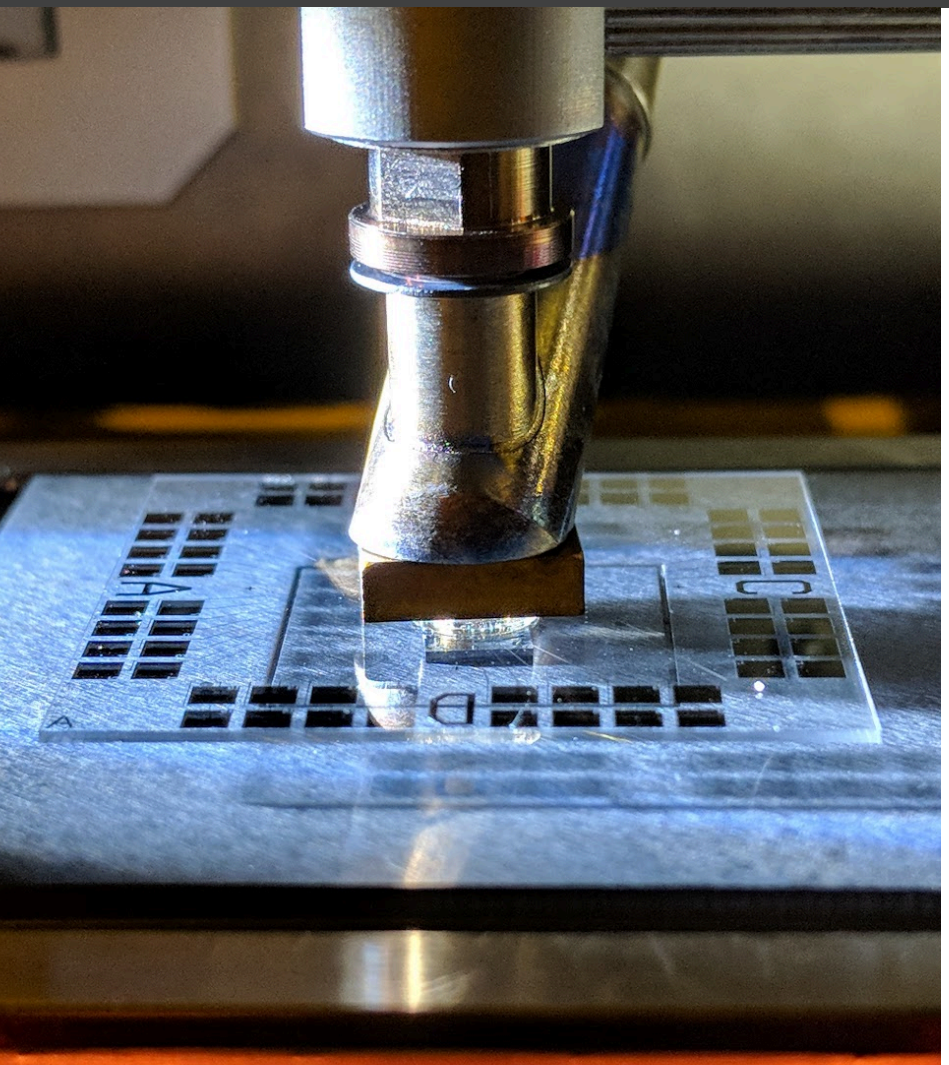


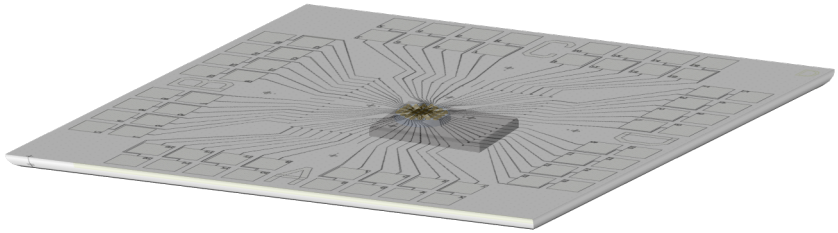
Apply flux before bonding



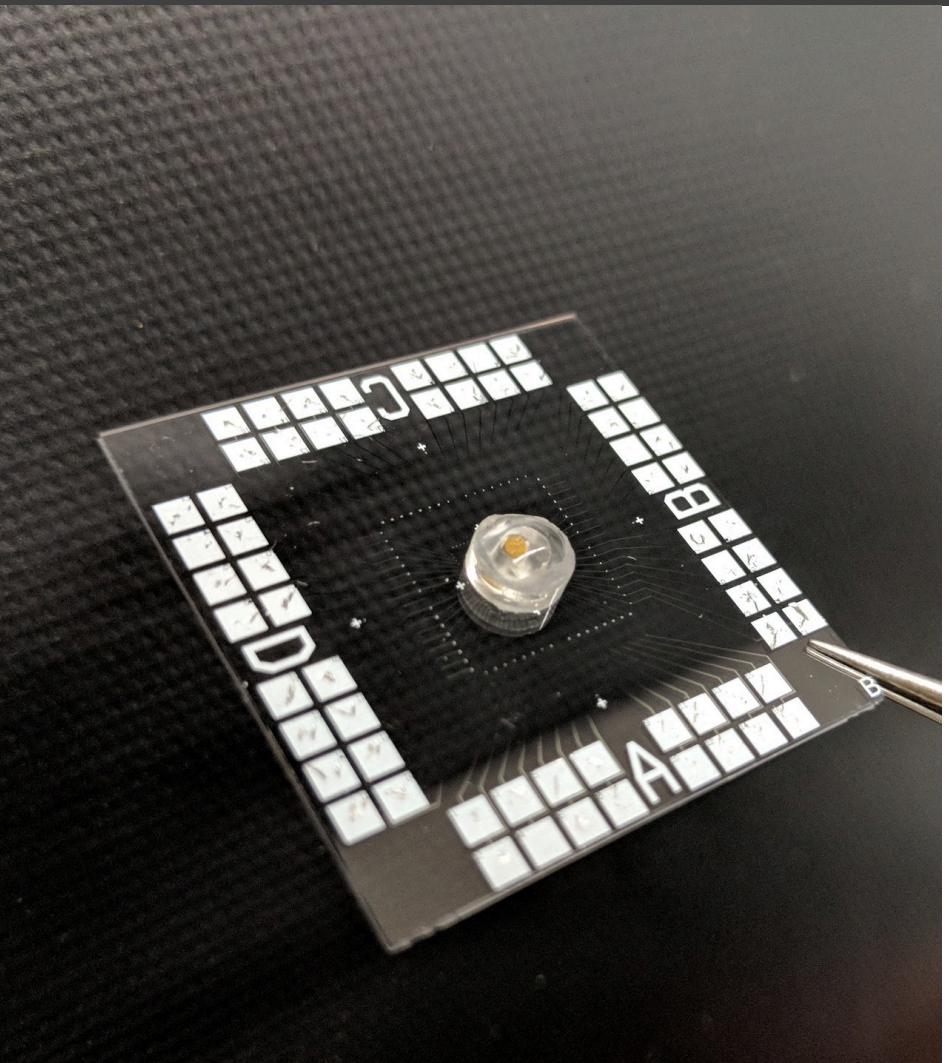


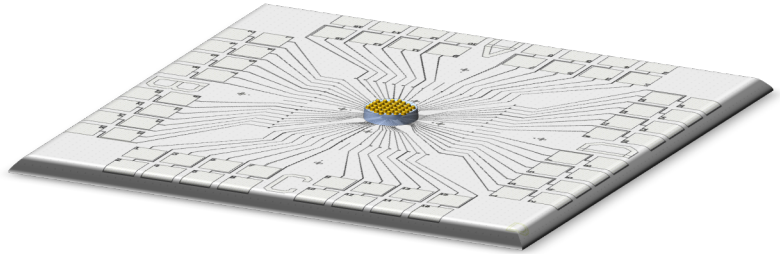
Bonding on Flipchip bonder





Bonding on Flipchip bonder





Bonding conditions DOE

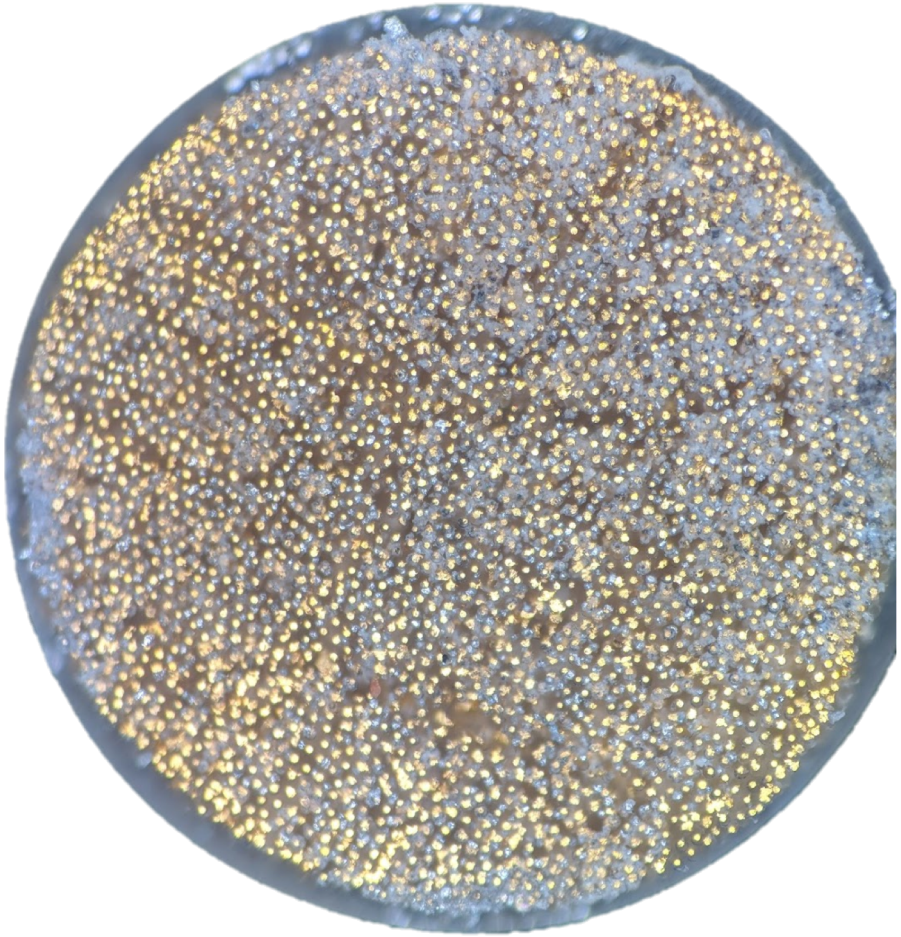
Ramp rate dT/dt (K/sec)	**Bonding temperature T_{bond} (°C)**	**Bonding time t_{bond} (min)**	Bonding force F (N)	Results
6 (solder chip) 20 (bare chip/bundle)	170	3	0	✗
		3	10	✗
		3	25	✗
		3	50	✗
		6	25	✗
		6	50	✓

Bonded assembly

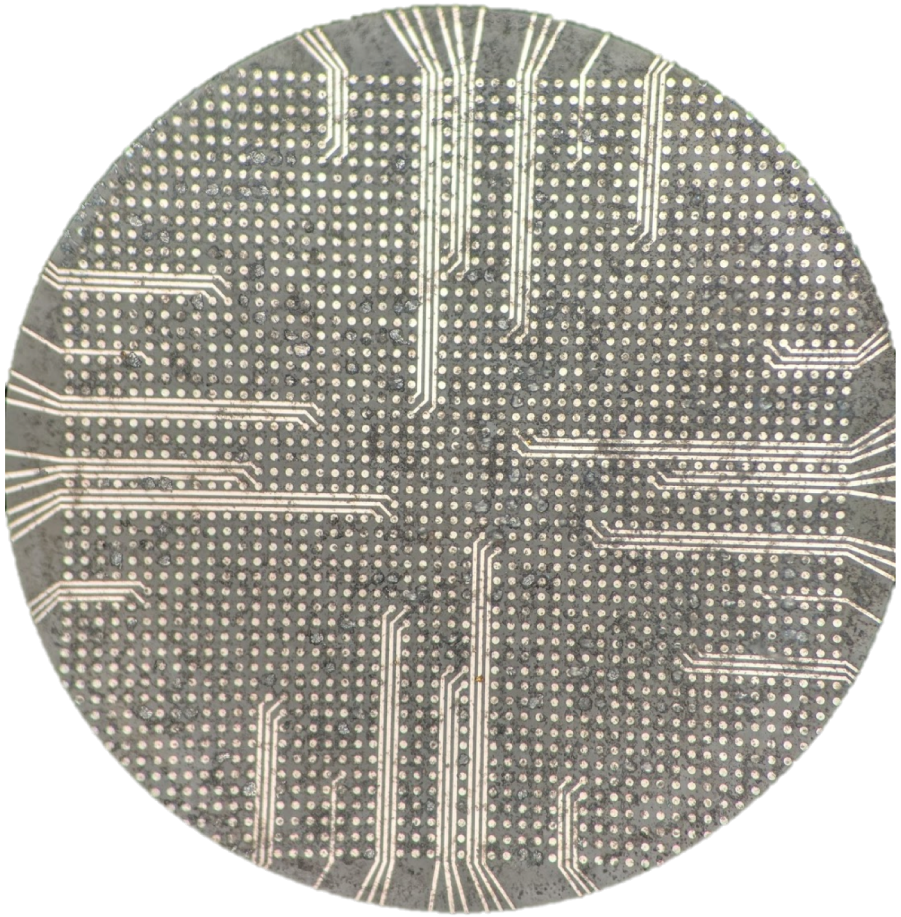
Mechanical Stability Test

Bonded assembly

Post-Bonding Bundle Surface

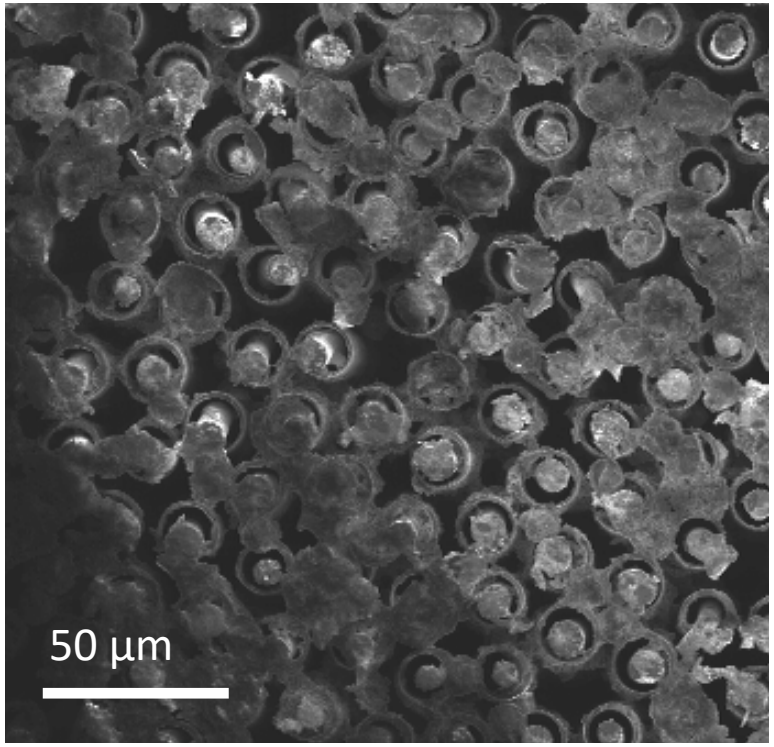


Post-Bonding Test Chip Surface

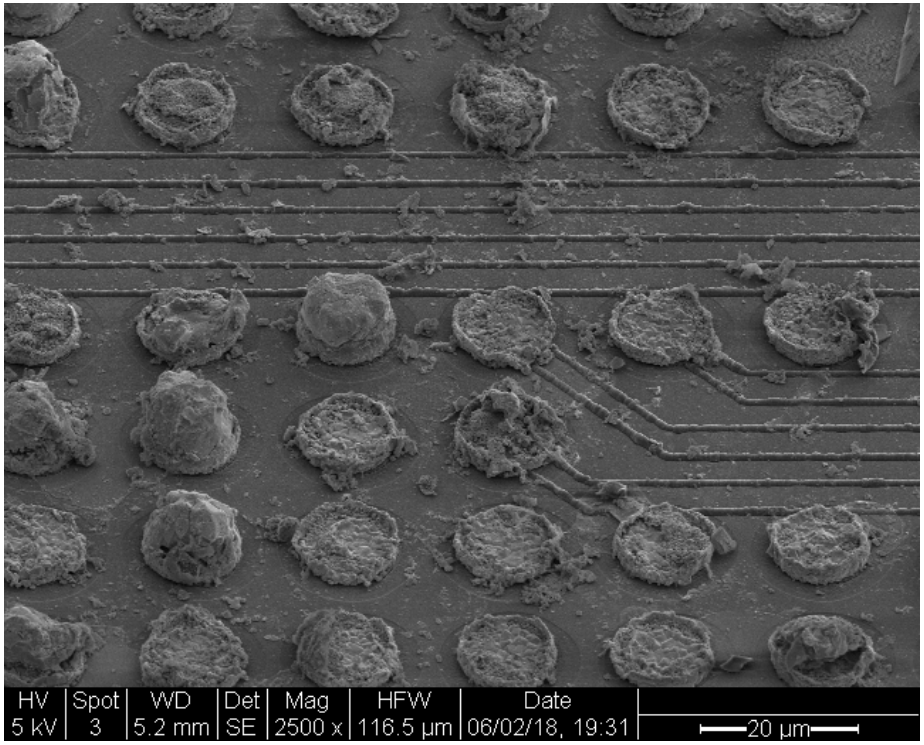


Bonded assembly

Post-Bonding Bundle Surface

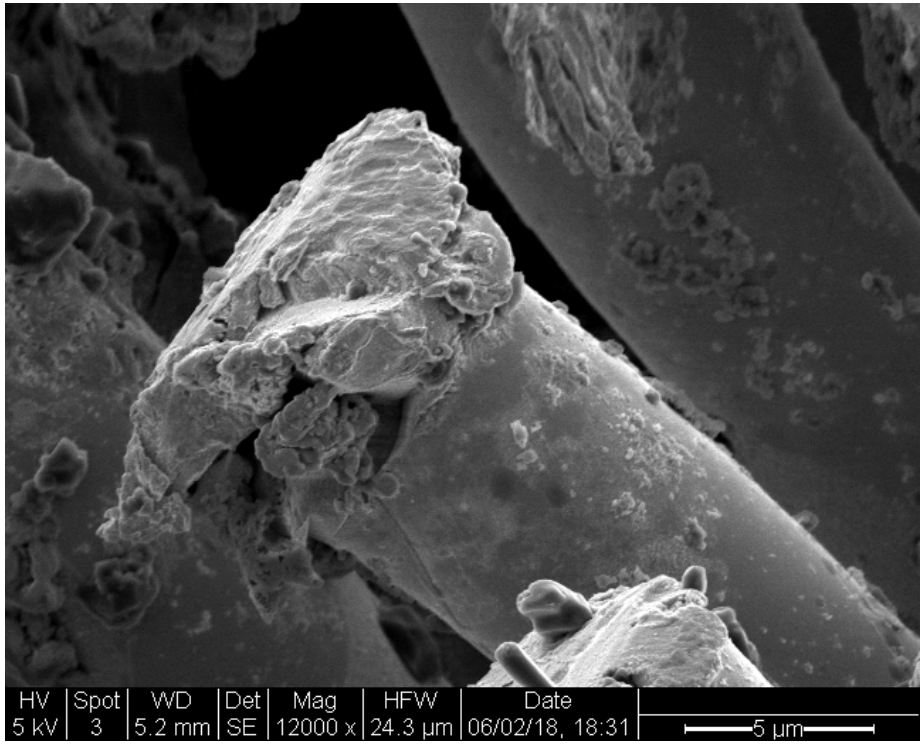


Post-Bonding Test Chip Surface

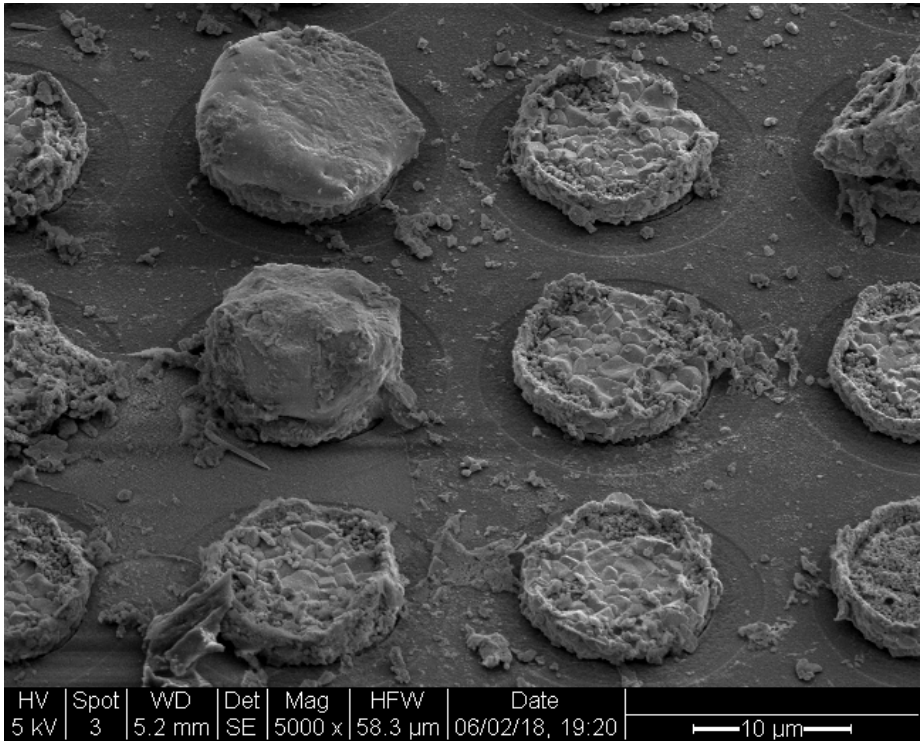


Bonded assembly

Post-Bonding Bundle Surface



Post-Bonding Test Chip Surface



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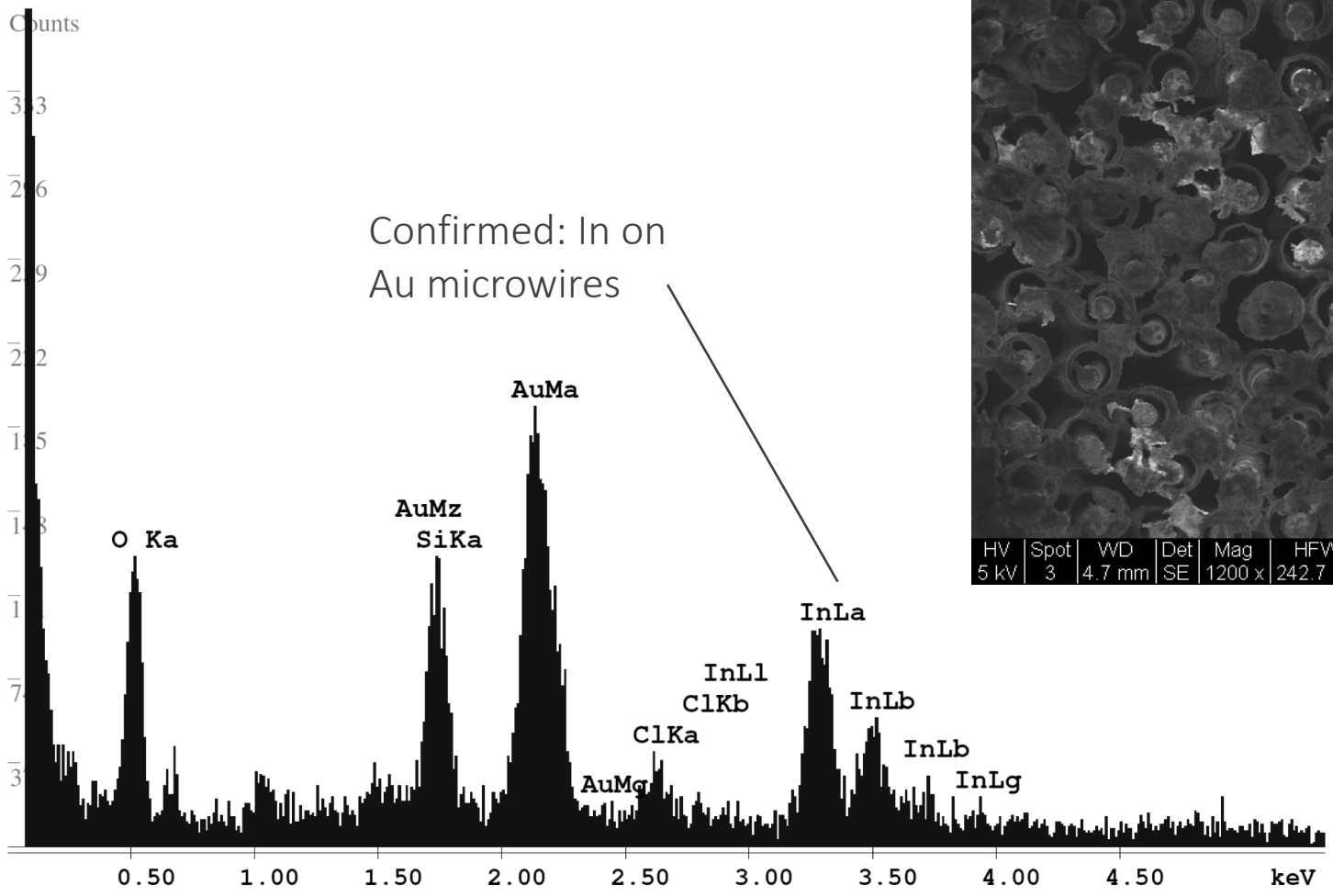

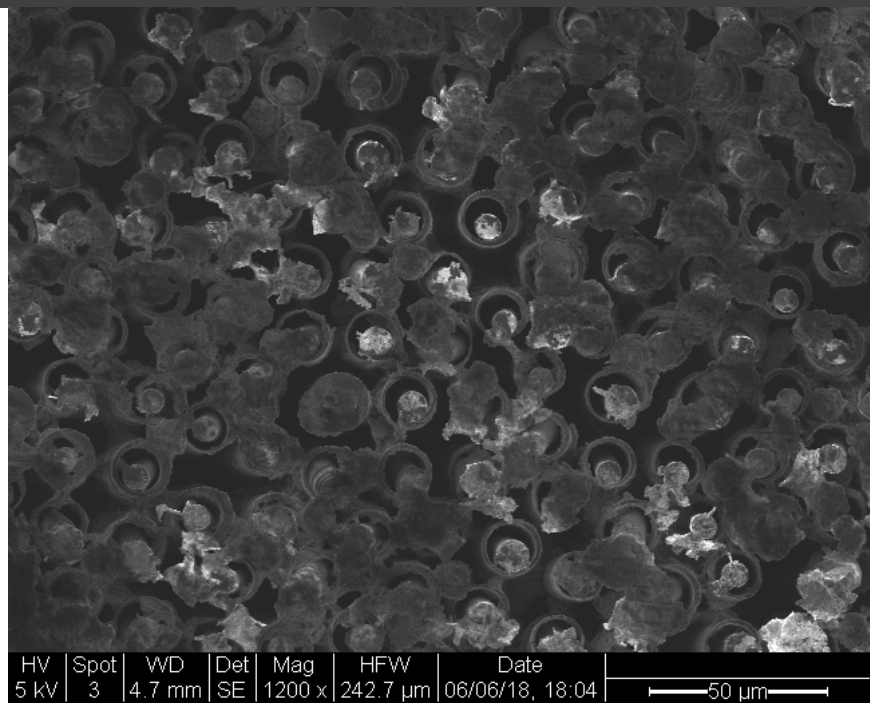

Project Summary

- Successful patterning of 2D array of 5-µm tall solder micro-pillars
- Achieved sub-170 ^{o}C bonding between 10 µm solder pads and microwires, likely with ~400 ^{o}C reflow temperature due to intermetallic formation
- Threshold bonding conditions: bonding time 6 min, bonding force 50 N
- Identified potential upgrades for the Flipchip bonder in ExFab: horizontal levelling, controlled environment, automated flux application

Future Work

- Explore use of forming gas for reducing bonding force/time
- Improve quality control of microwire glass coating for precise etch-back
- Scale up: 64 -> 1000 bonding sites
- Quantifying bonding performance: detailed impedance testing

Acknowledgments

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Thanks to Nick Melosh and fellow group members– Katie, Abdul, Nofar and Marc—for the discussions about test chip design and wire bundle fabrication

Thank you