Smooth sidewall etching in the PT-DSE

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Abstract

Process optimization has been performed in the PlasmaTherm Versaline LL-DSE Deep Silicon Etcher (PT-DSE) in order to achieve high aspect ratio etches with smooth sidewalls. A series of test etches was performed, varying several parameters to achieve a target scallop depth of <10nm. Beginning with a manufacturer suggestion, we have demonstrated significant improvement in sidewall smoothness for micron scale holes and lines.

Introduction

The Bosch process is an important tool in silicon micromachining, allowing for highly anisotropic etching deep into, or even through, wafers by alternating between a plasma polymer deposition (C_4F_8) and isotropic plasma etch (SF_6). Often employed in MEMS fabrication, we have used it for the purpose of creating microphotonic structures. Unfortunately, the Bosch process' alternating steps results in a scalloping along the sidewalls. This scalloping causes variation in transverse dimensions that can severely affect performance of the photonic devices. To deal with this issue in the past, scalloping has been removed through hydrogen annealing; high temperature treatment of silicon in a hydrogen ambient causes the surface to reflow and become much smoother (Figure 1) [1]. There have been problems in the past with maintenance of the tools necessary to complete this process, and therefore we are interested in generating an alternative to achieve the same end. It is also our hope that the smooth sidewalls will result in better mechanical properties.

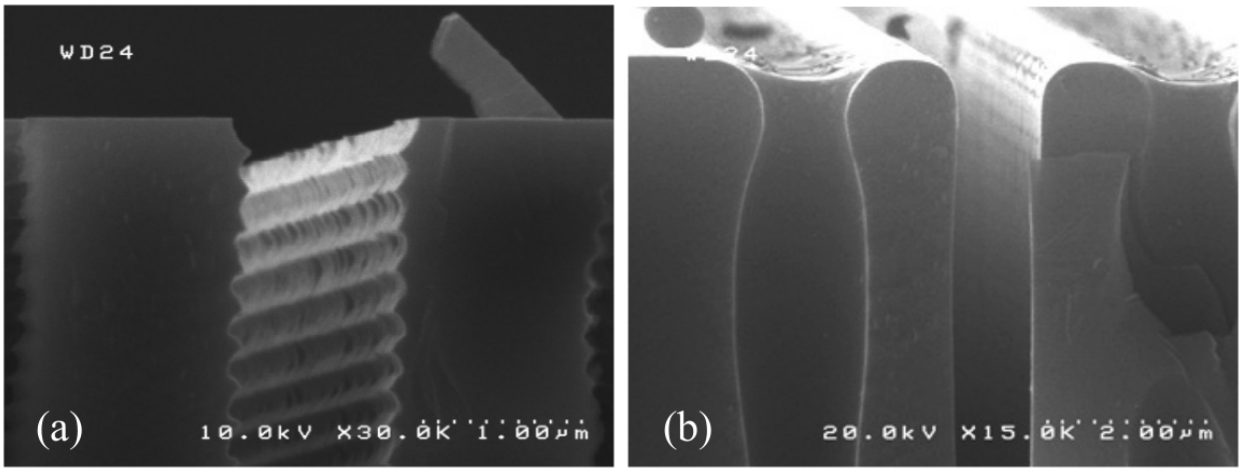

Figure 1: Example of a high aspect ratio microphotonic structure. The etch here is performed in stsetch2 and the sidewalls are smoothed via hydrogen annealing in the epi2.

SNF is home to three deep reactive ion etch (DRIE) tools, stsetch, stsetch2, and PT-DSE. The PlasmaTherm tool is the newest generation system, with several improvements over the older two. The primary difference is short step times, which can be achieved using fast gas switching, ALD-style valves and ICP frequency tuning. Also, a three-step process helps improve the etch profile by separating the etch into a breakthrough step (Etch A) and a normal etch step (Etch B), which can be tuned to achieve a vertical etch with high mask selectivity and smooth sidewalls. In particular, PlasmaTherm reported in a presentation that they were capable of achieving <10nm scallop depth with their fast switching technology, a result we endeavored to replicate through the project [2].

Fabrication

Recipe Development

As noted, our goal was to replicate the results of the tool manufacturer, as shown in a meeting on campus. Toward that end we were able to obtain, with Usha's help, the optimized recipe demonstrated in the presentation, which we call "PT Smooth". We compared PT Smooth to the already existing Nano and DSE FAT recipes to determine what choices had been made. DSE FAT is the standard etch process which achieves high etch rate and selectivity to photoresist, while Nano is optimized for smoother sidewalls [3]. Even so, Nano only achieves scalloping around 50nm. The parameters which differ between the DSE FAT, Nano, and PT Smooth recipes are step times, SF_6 flow (Etch B), pressure, and electrode temperature (Table 1). Due to the myriad possible parameters we could adjust, we selected three among these - temperature, Etch B flow,

and deposition (Dep) time (with Etch B time equal Dep time) - to vary, and focused on a range of values covering the Nano recipe and PT Smooth recipes. Due to the huge difference in process temperature between PT Smooth and recipes already available on the PT-DSE, we were especially interested in the effect that would have on the etch profiles. For those interested see [4, 5] for a better idea of typical DRIE process trends for a wider range of parameters. We employed the JMP statistical software to perform our DOE. We decided on a 2^3+1 full factorial design modeling second order effects.

Table 1: Differences in recipes

Recipe	Time/step (s)	SF6 Flow (sccm)	Pressure (mTorr)	Electrode Temp (C)
DSE FAT	2.5-1.5-3.0	150-150-300	25-40-75	15
Nano	1.0-1.0-1.0	150-150-50	30-35-25	15
PT Smooth	1.0-1.0-1.0	150-150-100	30-35-40	-20

Process Flow

We decided to utilize a thermal oxide mask despite the fact that the DSE can achieve high selectivity etches using a photoresist mask with the default recipes (>100:1). This choice was to preemptively mitigate any problems with selectivity that could have arisen in our final recipe. Therefore, our process began with thermal oxidation of standard B-prime wafers to grow approximately a 1um film. SPR 955 resist was spun to 0.7um thickness after a piranha clean, singe, and HMDS application. Thanks to special help from Mahnaz, we patterned the wafer with the ASML resolution mask to give us a standard test pattern for use across our experiments. The pattern was developed and then etched in amtetcher to clear away the oxide and then the resist removed in the Gasonics plasma asher. Finally, the etch is performed in the PT-DSE and the wafer is cleaved and examined under an SEM for characterization. Before beginning to etch our own wafers, we performed a 10 minute oxygen plasma clean followed by a 100 cycle chamber conditioning. SEM images were captured with cleaved samples mounted in a 90^o holder with a set screw and measurements performed in the Fiji (ImageJ) software package. We etched and analyzed 9 wafers, 8 for the full factorial plus 1 center point.

Mask Design

The resolution mask used provides a variety of features, including of isolated lines, lines and spaces, and holes of dimensions from 1um down to 0.2um. There are also larger feature providing open spaces for characterization of a wide range of structures. The smallest resolved feature on the wafer were larger than the minimum feature sizes on the mask, and different for each class of feature. Figure 2 demonstrates the layout of the features and resolution limit for lines.

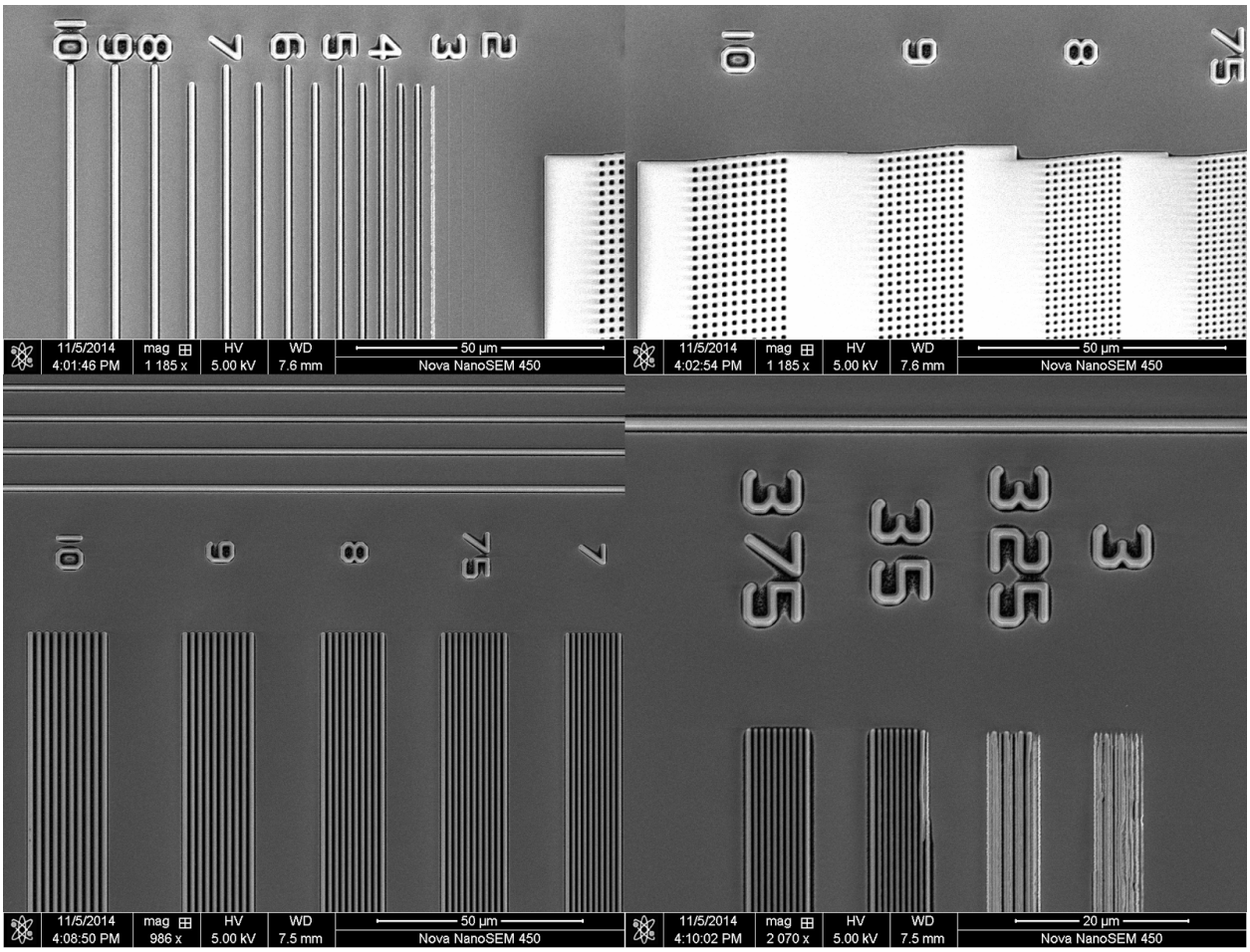

Figure 2: SEM images of the features of interest on the resolution mask. Clockwise from top left: isolated lines, arrays of holes, the smallest group of lines of spaces resolved in the lithography, and the largest lines and spaces. Feature sizes range from 200nm to 1.0um, with the smallest features actually resolved at 350nm for isolated lines and line and spaces, and 450nm for holes.

Challenges

We ran into two major difficulties with getting the PT Smooth recipe to work. Due to time limitations, we only developed workarounds and were not able to completely troubleshoot the issues. First, increasing the Etch B gas flow resulted in a reflected

power problem part way through the etch above a flow of about 80 sccm SF_6. This issue disappeared almost entirely if we loaded the wafer in maintenance mode and allowed it to remain in the chamber for five minutes before performing the etch. Also, when running processes at low temperature, the loading and unloading of the wafer resulted in mishandling of the wafer, and often breakage of the wafer or ceramic clamp. Lowering the temperature after loading the wafer and then raising it back to standard before unloading eliminated this problem entirely.

Results

Using JMP, we analyzed the results of the etches, and compiled the more interesting results below. Scallop depth was measured at different locations for each etch, near the top, middle and bottom, as were the undercut of the mask and sidewall slope. The scalloping was measured in three locations because they each exhibit different characteristics within a sample but shared each section characteristics across all samples. For example, the scalloping near the top was most severe in every case, then the middle region was quite smooth in most cases, with the scallops slightly more noticeable at the bottom. We also examined trends for the undercut. Sidewall slope was generally very small and not significantly affected by varying our chosen parameters.

PT Smooth

Figure 3 demonstrates the PT Smooth recipe results. Notice the smooth vertical sidewalls and only slight undercut at the top. The results are already very close to what we had hoped to achieve, but there are different optimal recipes for different types of features, as indicated below.

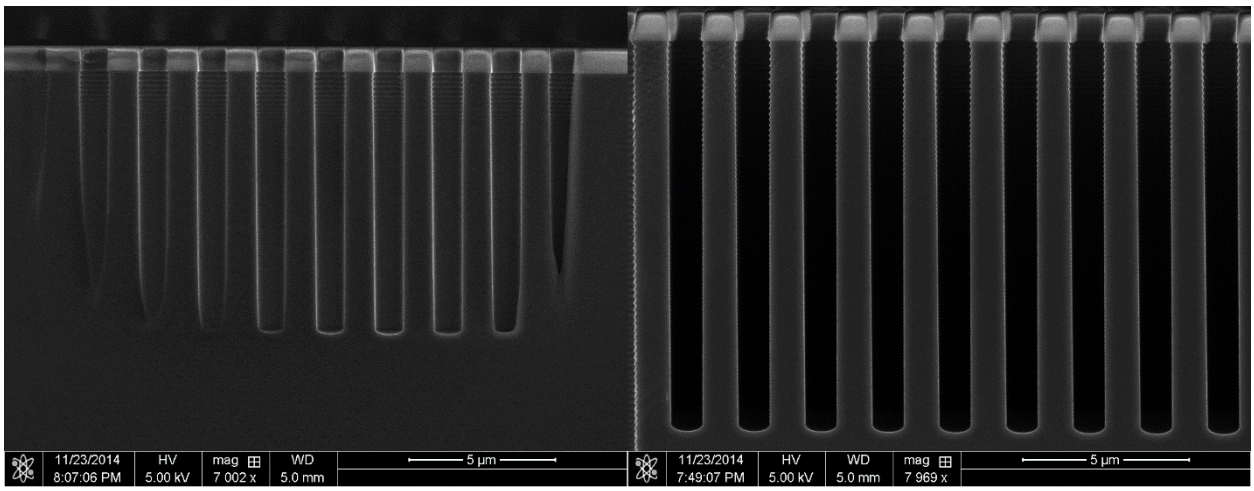

Figure 3: Etch results of the recipe closest to that provided by PlasmaTherm (90sccm SF6, -20C, 1s Dep time), for 1um holes left, and 1um lines and spaces.

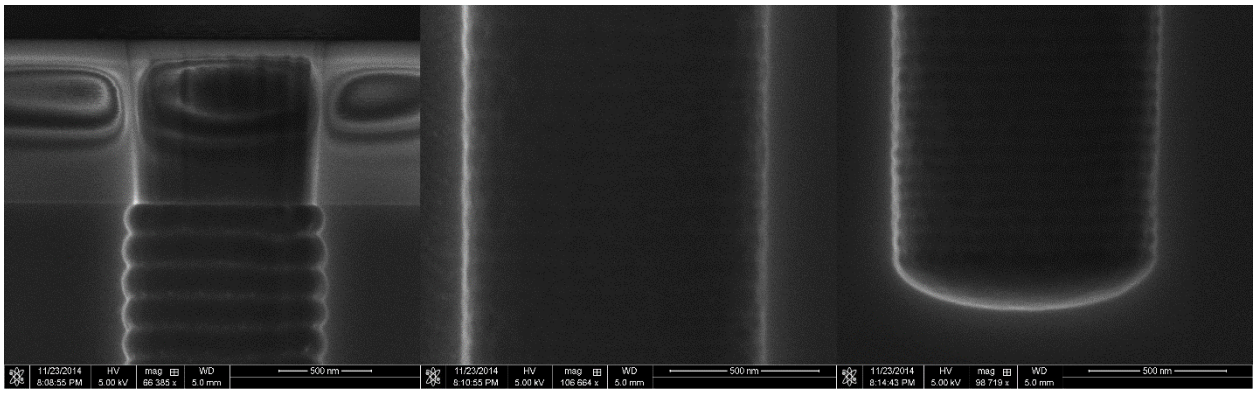

Figure 4: Magnified images of various sections of the etch profile in a 1um hole.

1um Lines

The 1um lines showed several significant trends. For the scalloping, we examined the top and bottom sections because the middle was so smooth that any measurements would be on the order of the pixel error. Both sections showed that a lower deposition and etch a times resulted in less scalloping with a strong statistical significance (p value = 0.034 top and 0.044 bottom). This result is as expected. The etches are isotropic, so lowering the time lowers the etch distance in all directions. There also appears to be a weak but somewhat significant evidence for dependence on temperature (p value = 0.075 top and 0.095 bottom). However, these trends are in opposite directions and so there is no optimal temperature for minimal scalloping. Therefore, sidewall roughness does not explain the choice of significantly lower temperature in the PT Smooth recipe. Electrode temperature does greatly affect the undercut (p value = .0035), with their being practically no undercut at -20 C. This result is likely due to improved initial polymer deposition at the lower temperature. SF6 flow showed no measured statistical

significance to the scalloping or undercut. This lack of effect suggests that were optimizing etch gas flow within a saturated regime. Since the higher SF6 flow increased reflected power failure rate, the lowest possible SF6 flow is preferable for any recipe.

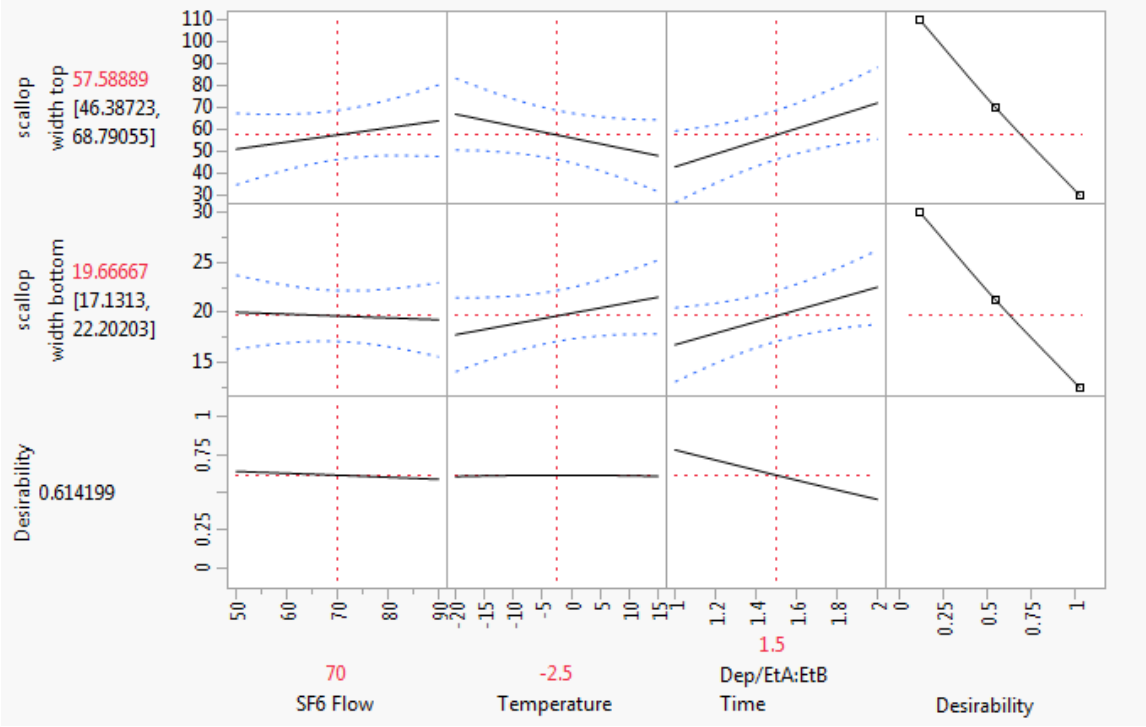

Figure 5: 1 um line scalloping prediction and desirability profiles

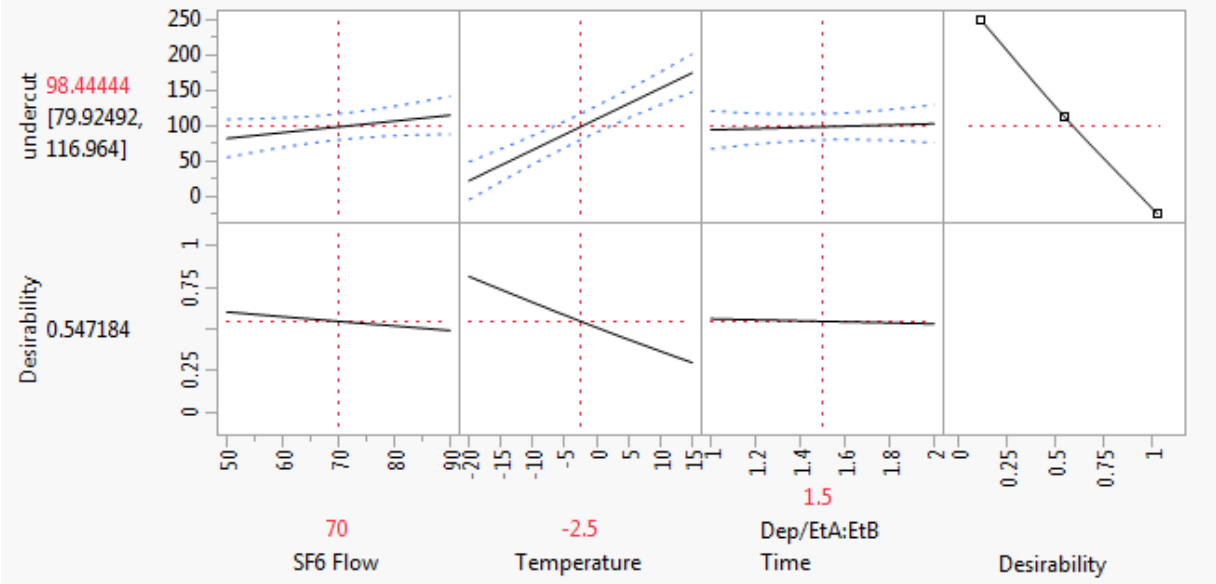

Figure 6: 1 um line undercut prediction and desirability profiles

Based on these results, the best recipe to minimize scalloping and undercut would have electrode temperature -20C, deposition and etch times 1s each, and SF6 Flow at 50 sccm.

1um Holes

The holes showed similar trends to the lines. The top scalloping still seems to be affected by deposition and etch times, though less significantly (p-value = 0.059 for times, 0.086 for temperature). There appears to be no statistically significant trends among the parameters for the bottom scalloping. Most likely the etch profile is severely affected by limited transport of plasma species down to the bottom through a small aperture. We would not expect our parameter space to alter the transport condition, and therefore this result is in line with expectations. Undercut is still heavily influenced by the lower electrode temperature (p-value = 0.016).

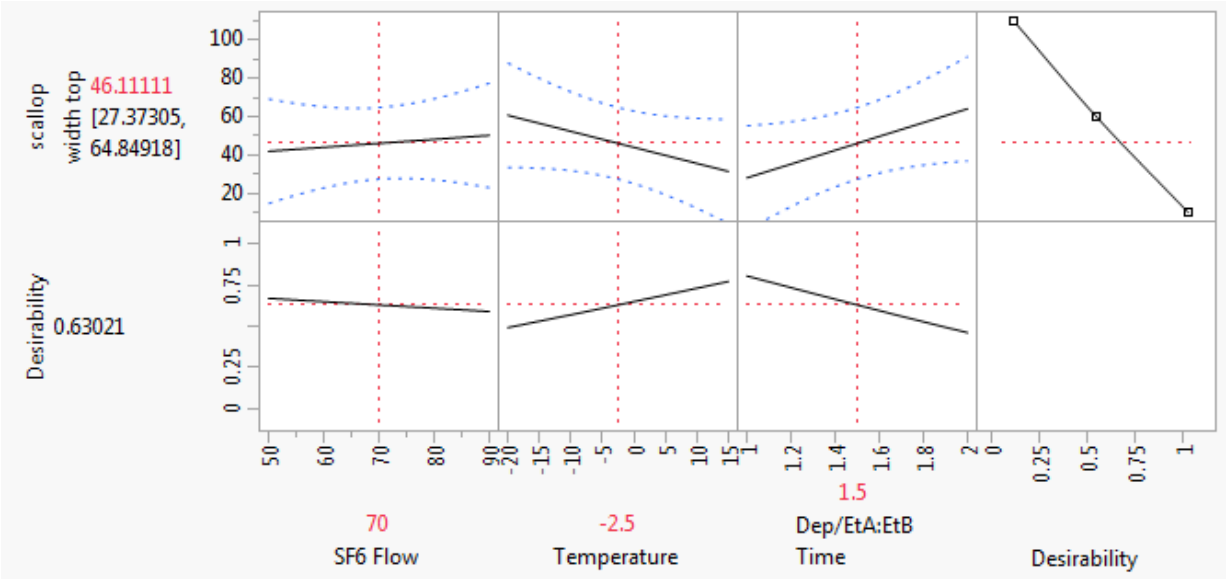

Figure 7: 1 um hole scalloping prediction and desirability profiles

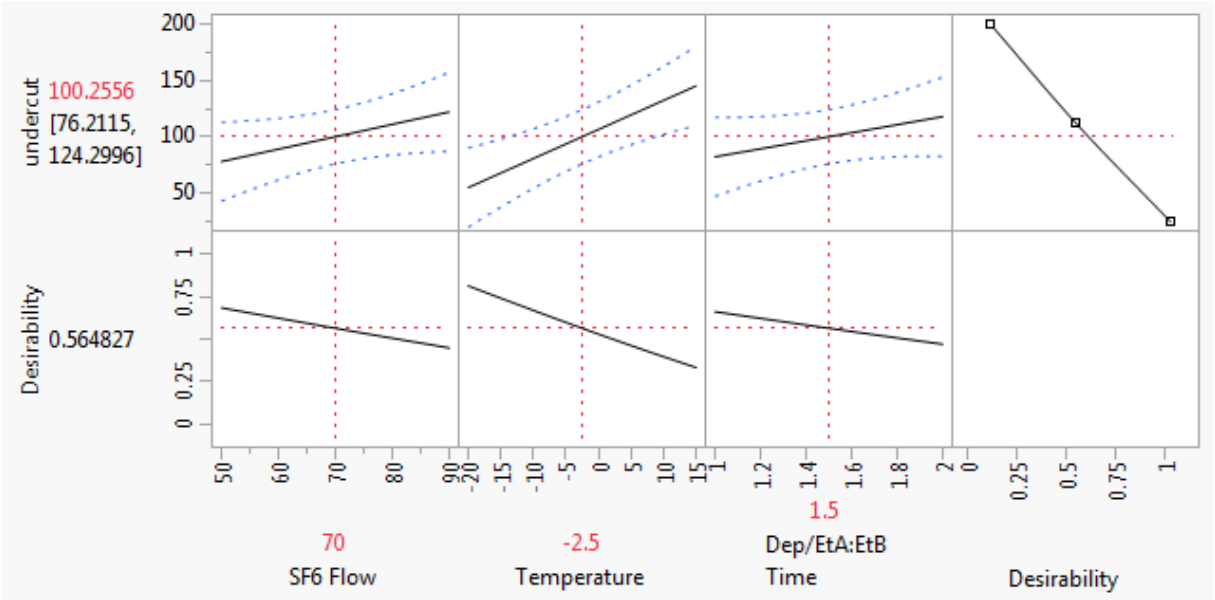

Figure 8: 1 um line undercut prediction and desirability profiles

Again, the best recipe to minimize scalloping and undercut in the 1um holes based on these results would have electrode temperature -20C, deposition and etch times 1s each, and SF6 Flow at 50 sccm. However, the fact that these trends are only seen strongly at the top suggests that the small feature size causes transport issues, and so other parameters should be investigated to optimize small feature recipes.

Conclusion

Our work demonstrates promise of the PT-DSE for achieving high aspect ratio etches with smooth sidewalls. We have only covered a small part of the parameter space over the course of our investigation, but already we have achieved results similar to the manufacturer's example. Future experiments should include process parameters which promote transport of plasma species to the bottom of trenches and holes, such as electrode bias, and especially morphing. Additionally, the deposition could be increased initially to reduce scalloping near the top of features, for example through a longer light step, or an initial few-cycle loop with longer deposition step time.

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References

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2. "Deep Silicon Etch (DSE™) for MEMS and Packaging," PlasmaTherm
3. "Stanford University Deep Silicon Etch," PlasmaTherm,
4. Jeong, J. "High Aspect Ratio Si Etching in STS2" EE412 report
5. McVittie, J. "Suggested Parameter Changes to Improve STS2 Etch Profiles", SNF Wiki
6. Harrison, K., "Vertical Sidewall Etch Search," May 14, 2013

Appendices

Appendix A - Detailed Process Flow

1. wbclean: sc1 → HF → sc2
2. thermco: wet oxide, 1100C, 2.25hr (~1um film)
3. yes oven
4. svgcoat2: 0.7um 955, no VP, 2mm EBR
5. ASML: ASML resolution mask
6. svgdev: 9321
7. 110C oven: 2hr hard bake
8. amtetcher: program 3, 40 min
9. gasonics: 016
10. pt-dse: 10min clean and 100cy season at start, 100cy per recipe variation
11. Nova SEM measurements

Appendix B - Recipe Details

	Pattern	SF6 Flow	Temperature	Dep/EtA:EtB Time
1	+++	90	15	2
2	000	70	-2.5	1.5
3	+−+	90	-20	2
4	−−−	50	-20	1
5	−−+	50	-20	2
6	−+−	50	15	1
7	+−−	90	-20	1
8	++−	90	15	1
9	−++	50	15	2

Figure 9: Sequence of experiment runs determined using JMP statistical software.

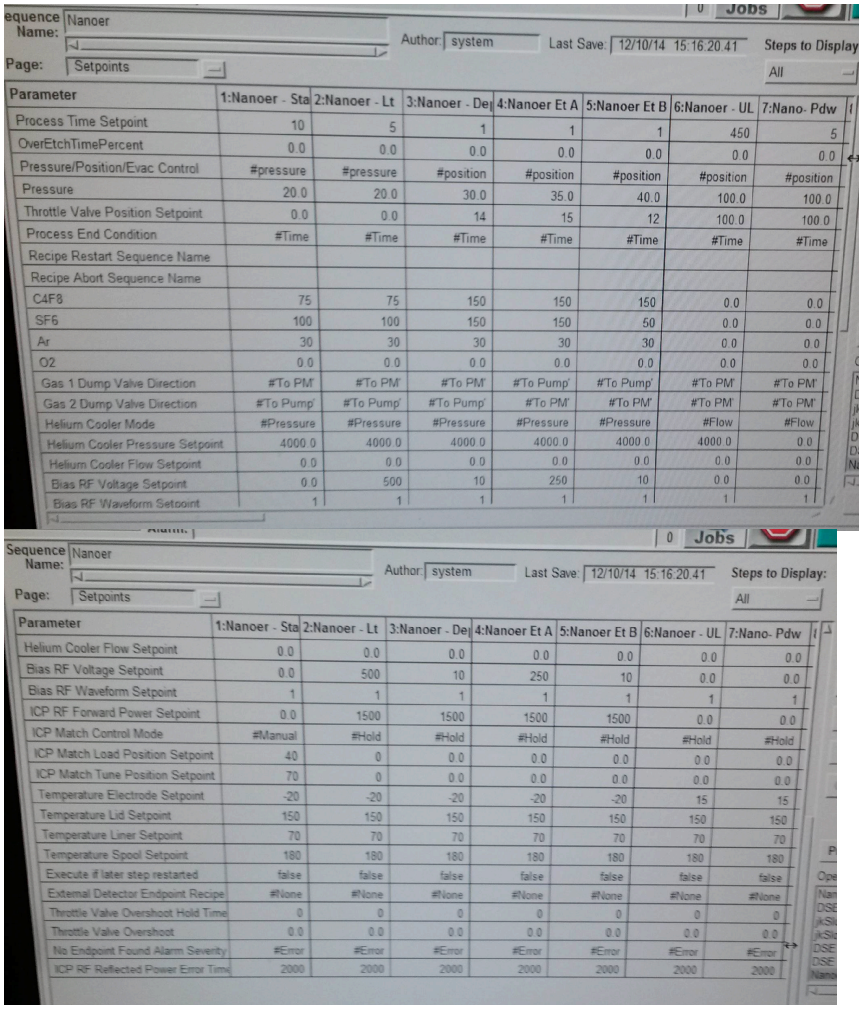

Figure 10: Full list of process parameters for each step of the experimental recipe. No morphing was added for any parameter and recipes were run for 100 cycles.