Characterization of TMDs and Contact schemes for Photovoltaic Applications

ENGR 241 Project
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Aravindh Kumar, Koosha Nassiri Nazif

SNF Mentor:
Michelle Rincon

Industry Mentors:
Hye Ryoung Lee
Archana Kumar

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1. Project objective

This project seeks two main objectives: 1. To develop an optimal process for transition metal dichalcogenides (TMDs) solar cells and 2. A systematic study of various contact schemes to TMD, for use both for TMD transistors and TMD solar cells. WSe_2 and WS_2 are chosen as the TMDs to study in this project, since they have optimal bandgaps (1.2 eV and 1.57 eV respectively) for use as a single junction solar cells or in parallel with Si in a TMD/SI tandem solar cell respectively.

The first goal involves a) characterizing the method for exfoliating the TMD flakes on an SiO_2 substrate, b) characterization of an etch recipe for shaping TMD flakes and c) a reliable and reproducible flake transfer method from an SiO_2 substrate to a metallic substrate for vertical contacts.

Since a reliable growth method for bulk (~100 nm) TMDs is not yet available at Stanford, we are exfoliating TMD flakes from a CVT-grown TMD crystal on a SIO_2 substrate. There are various parameters involved in this process which are extensively studied in this project using a formal design of experiment (DOE) method. This part of the project is framed as the exfoliation study.

The exfoliated TMD flakes come in random shapes and thicknesses. Even one flake can have various thicknesses. One mini goal of this project is to find the optimum contacts to WSe_2 and WS_2 for photovoltaic applications. In order to make a fair comparison between two different sets of contacts, we need to test them on a single, symmetric flake with uniform thickness. In order to do so, an etch recipe for WSe_2 and WS_2 is needs to be developed, which is done during this project.

Due to higher electric fields achieved in vertical (top-bottom) contact schemes compared to (lateral) both-top contact schemes, a higher efficiency is expected from TMD solar cells with top vertical contacts. We are going to make both lateral and vertical contact solar cells in this project. To make a vertical contact solar cell, we need to transfer the shaped flake to another substrate with the bottom contact already in place (a metallic substrate). This section of the project is called substrate-to-substrate transfer of TMDs.

Second, as part of the systematic study of the contacts, we investigate where the various metals' fermi levels pin, when interfaced by the TMDs. This is called the pinning study. We also plan to try out different interlayers between the metals and the TMDs (an structure known as Metal-Interlayer-Semiconductor - MIS) to de-pin the fermi level and obtain better contact characteristics.

Benefits to the SNF community: During this project, we developed 1. A better method to exfoliate TMD flakes onto SiO_2 substrates, 2. A recipe to etch bulk TMDs (WSe_2 and WS_2), 3. A method to transfer TMD flakes from SiO_2 substrates onto metallic substrates and also 4. provide optimum choices for n-type, p-type and solar contacts to WSe_2 and WS_2.

2. Project Methods and Results

2.1. Exfoliation Study

2.1.1. Exfoliation Study (Methods)

In this study we investigated the conditions that would lead to maximum number of exfoliated flakes with desired characteristics, which mean thick and wide flakes for the solar cells and thin and wide flakes for the contact study.

Reviewing the literature, we came up with four potentially important variables: 1. O_2 plasma descum on the substrate that we are exfoliating the flakes on (using Drytek2), 2. Substrate forming gas anneal (FGA) at 400ºC for 30 minutes (Using RTA), 3. Hot plate anneal (HPA) at 90ºC for 2 minutes during the exfoliation (using a hot plate), 4. Using blue tape vs. gel films for the exfoliation

We ran a formal design of experiment (DoE) analysis using the JMP software on the first three parameters (since it took about 3 weeks for the gel films to be shipped and delivered to us; therefore we fixed the fourth parameter to blue tape). From the color of the flakes, we can approximate the flakes thickness, as explained in [1]. DoE reduced the number of required screening experiments from $2^3 = 8$ to the following 4 experiments:

Table 1. DoE parameters of the exfoliation study done on the blue tape

#	O_2 Descum	FGA	HPA
1	X	X	X
2	X	-	-
3	-	X	-
4	-	-	X

2.1.2. Exfoliation Study (Results)

The results of WSe_2 and WS_2 exfoliation DoE study done on blue tape is shown in the tables 2 and 3.

Table 2. Result of DoE screening experiments on WSe_2 exfoliation

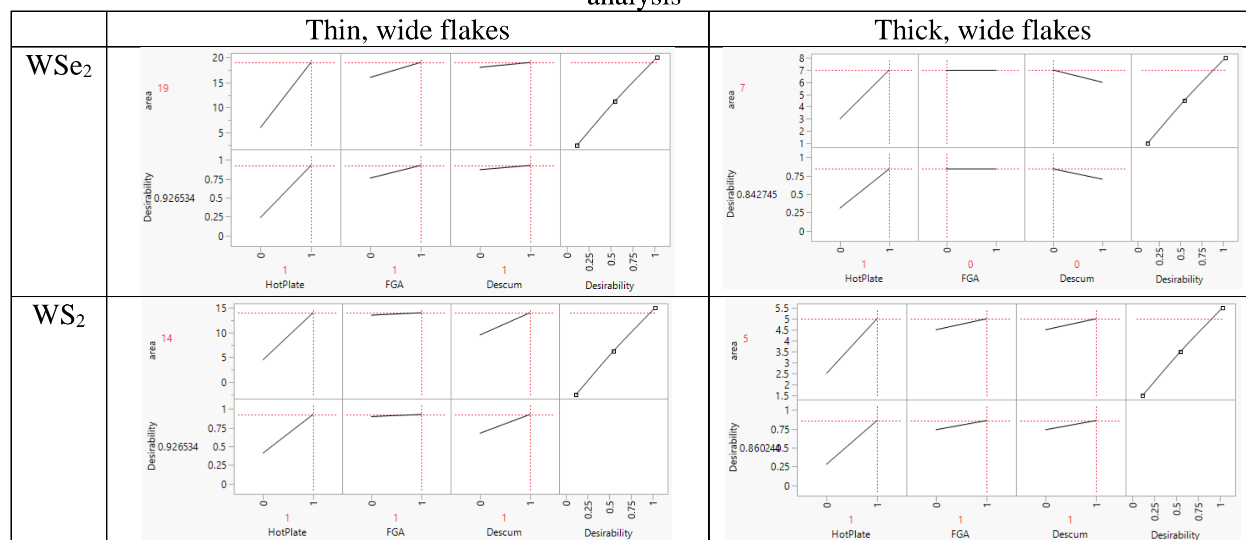
#	O_2 Descum	FGA	HPA	# of thin wide WSe_2 flakes	# of thick wide WSe_2 flakes
1	X	X	X	19	6
2	X	-	-	3	2
3	-	X	-	5	3
4	-	-	X	19	7

Table 3. Result of DoE screening experiments on WS_2 exfoliation

#	O_2 Descum	FGA	HPA	# of thin wide WS_2 flakes	# of thick wide WS_2 flakes
1	X	X	X	14	5
2	X	-	-	4	2
3	-	X	-	0	2
4	-	-	X	9	4

Looking at the table above, we can infer that HPA has the most significance among the three parameters. The reason HPA is so important is that it increases the area of sticking between the blue tape and substrate and this increases the number and size of flakes left behind on the substrate. Both O_2 descum and FGA seem to be inconsequential.
Running a maximum desirability JMP analysis on the results above, we came up with the following optimal conditions:

Table 4. Optimal conditions to exfoliate WSe_2 and WS_2 flakes using blue tape. Done by JMP DoE analysis



Therefore the optimal exfoliation conditions when using a blue tape would be:

Table 5. Optimal conditions to exfoliate WSe_2 and WS_2 flakes using blue tape (summary)

	O_2 Descum	FGA	HPA	Expected # of thin wide flakes	Expected # of thick wide flakes
WSe_2	**X**	**X**	**X**	**19**	**N/A**
	-	**-**	**X**	**N/A**	**7**
WS_2	**X**	**X**	**X**	**14**	**5**

With the gel films, we did a simple exfoliation (without O_2 descum, FGA and HPA). Since O_2 descum and FGA (processes done on the substrate before the exfoliation) turned out insignificant we omitted them from the study. We also did not do HPA because we leveraged weak adhesion of the gel film and hot plate anneal would counteract this.

Gel film resulted in significantly larger number of thin and wide flakes compared to blue tape but roughly similar number of thick flakes. This larger number of thin wide flakes can be attributed to the weak adhesion of the gel-film. When exfoliating using blue tape, when peeling off the blue tape, the strong adhesion of the blue tape leads to breakage of flakes, leading to thin flakes which are very small. We avoid this problem by using a gel-film. The final optimal conditions to get thin/thick, wide flakes is as follows.

Table 6. Optimal conditions to exfoliate WSe_2 and WS_2 flakes (summary)

	O_2 Descum	FGA	HPA	blue tape vs. gel film	Expected # of thin wide flakes	Expected # of thick wide flakes
WSe_2	**X**	**X**	**X**	**Gel film**	**25**	**N/A**
	-	**-**	**X**	**Either**	**N/A**	**7**
WS_2	**X**	**X**	**X**	**Gel film**	**20**	**N/A**
	X	**X**	**X**	**Either**	**N/A**	**14**

2.2. Etching Characterization

2.2.1. Etching Characterization (Methods)

There has been no recipe in the SNF that can be used to etch the multilayer TMDs fast. The best we have had was an oxygen plasma etch using the MRC tool which etches the TMDs layer by layer and is very slow.

In this project we made and characterized an etch recipe for the PlasmaTherm Metal Etcher in the SNF (PT-MTL) that can etch multilayer TMDs both at a fast and slow etch rates. For patterning, we simply used the photoresist as the mask.

Consulting with our in-house etching expert, Dr. Usha Raghuram, we came up with an starting recipe which we characterized and modified afterwards to achieve the fast and slow etch rates which we desire.

2.2.2. Etching Characterization (Results)

The starting etch recipe is as follows:

Table 6. Starting Etch Recipe

Etch Recipe				
Tool Used	Chemistry	Pressure	ICP Power	Bias Power
PT-MTL	SF_6/Ar	30 mTorr	600 W	50 W

Which resulted in an etch rate of 25.2 nm/s for WSe_2 which is too fast, considering the range of thicknesses we are dealing with – 5-200 nm. The main two knobs that we have to decrease the etch rate are the ICP power and the bias power. Decreasing them both, we came up with the following etch rates.

Table 6. Various etch recipes along with their etch rates

Chemistry	**Pressure**	**ICP Power**	**Bias Power**	**Etch Rate**
SF_6/Ar	30 mTorr	600 W	50 W	25.2 nm/s

SF_6/Ar	30 mTorr	600 W	30 W	20.3 nm/s
SF_6/Ar	30 mTorr	200 W	30 W	17.5 nm/s
SF_6/Ar	30 mTorr	0 W	30 W	11.2 nm/s

We tested the final two recipes on three samples and confirmed the reliability and repeatability of the etching recipe – etch rate variability of 1%. Approximately similar results should apply to WS_2 which we will confirm at the beginning of the second (winter) quarter, before we start fabricating the WS_2 solar cells.

Recipe details can be found on pt-mtl under the name "Koosha_SF6". An example etch done on an WSe_2 flake is shown in the Fig 1.

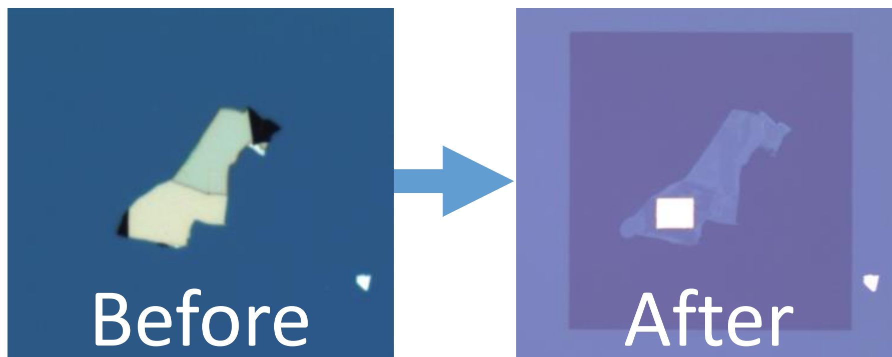


Fig 1. WSe_2 flake before and after the etch

2.3. Transfer Study

2.3.1. Transfer Study (Methods)

In order to make vertical contacts, we need to transfer the etched flakes to another substrate with the bottom contacts already in place. This process was done in glovebox located in room 155A.

As shown in the process flow in figure 2, we first bring in to contact the PPC/PDMS stack on the WS_2 or WSe_2 flake at 55°C. Note that the PDMS is prepared by combining a base and curing agent and PPC is spin coated on top of that. This stack is then mounted on a glass slide using Kapton tape. More information on the process flow is provided in the SOP section.

Leaving the PPC in contact with the flake for a few second, we then pull up the glass slide which would hopefully pick up the flake from the substrate (the yield is low and still needs to be improved).

Third, we move to the second substrate and lay the flake/PPC/PDMS stack on top of the bottom contact (metallic substrate) and increase the temperature to 90°C such that the PPC-PDMS bonding becomes weak enough for the PPC to peel off from the PDMS and stay on the new substrate, along with the flake underneath.

Finally, after the transfer is done, the substrate is put in Acetone for two hours such that all the PPC is dissolved and removed from the substrate, leaving us with a clean surface, ready for top contact deposition.

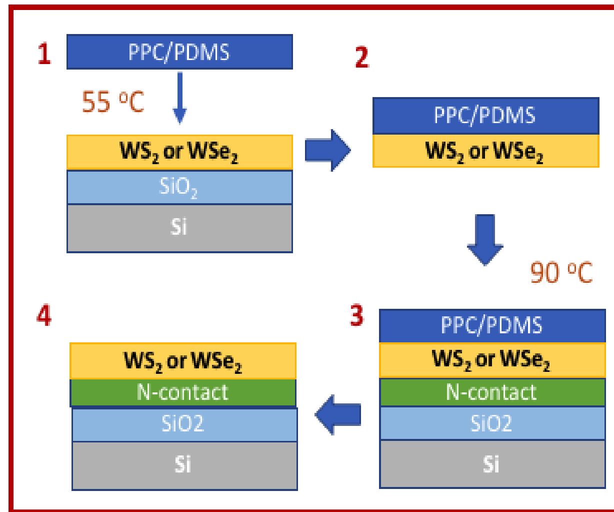


Fig 2. schematics of substrate-to-substrate transfer process flow

2.3.2. Transfer Study (Results)

Although the yield to transfer the large, randomly shaped flakes was 100% - in some cases we had to try to pick up the flakes a couple of times – the yield for the etched flakes was almost zero. The potential reasons are 1. The etched flakes are too small to pick up, 2. The backing done during the lithography process as well as the heating during the etching process makes the flakes bond stronger to the substrate and thus harder to pick up.

We are still troubleshooting this process and will hopefully address this issue by the second (winter) quarter. Our candidate solution is to split the etching time into shorter times so that the sample does not heat up too much during etching. If not successful, we will switch the order of the transfer and etching processes. The only possible risk is that etching after the transfer might etch the bottom contact – depending on what metal we are using. However this can be solved by redepositing metal on the areas where the metal has been etched off.

2.4. Pinning Study

2.4.1. Pinning Study (Methods)

At a metal-semiconductor interface, the work-function of the metal is modified due to interface states, dipole, defects and/or gap states. It's observed that the metal workfunction is "pinned" at a certain level and this pinning is a function of the semiconductor material and its quality. At MoS_2, the metals pin near the conduction band irrespective of their work-functions, thereby resulting in n-type contacts. However, we need both n-type and p-type contacts to make an efficient photovoltaic cell since it must split an electron hole pair in order to generate power.

While the pinning of metal contacts to MoS_2 is well-known, no comprehensive study of pinning to WS_2 and WSe_2 has been carried out yet, even though it's shown in literature that it's easier to obtain n-type to WS_2 and p-type contacts to WSe_2. We aim to study the pinning of metals to WS_2 and WSe_2 which would help us identify the best n-type and p-type contacts to WS_2 and WSe_2. This would also lead to the next phase of the project where we aim to de-pin the metals using a WoO_x or NiO_x interlayer for n-type and p-type contacts respectively.

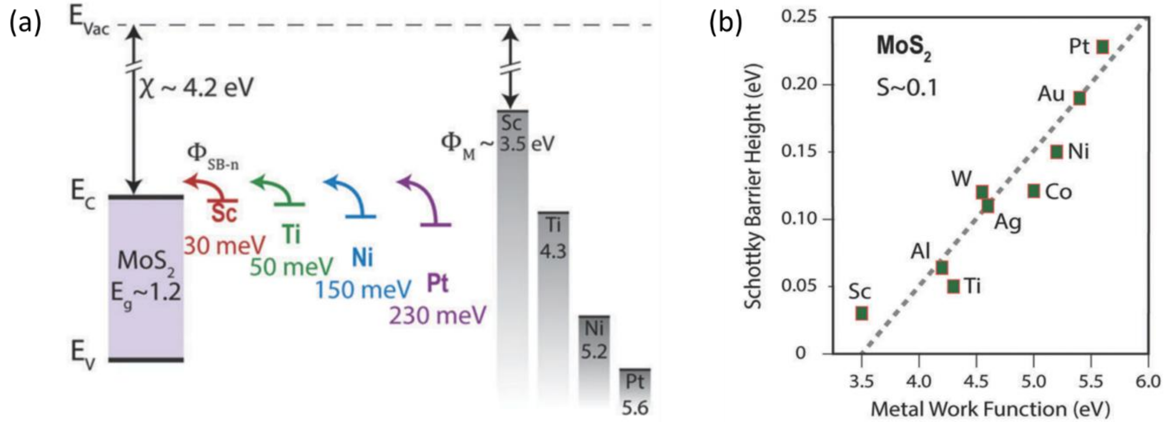


Fig 3. (a) Band-diagram showing the pinning of the metals near the conduction band of MoS2; (b) Pinning of various metals at MoS_2 and the resulting pinning factor [2]

Pinning of metals is studied by extracting the Schottky barrier heights of each metal-semiconductor contact. This is done by measuring the temperature-dependent Id-Vg characteristics of transistors using each contact scheme. We carry out Id-Vg measurements at the temperatures of 200K, 250K, 293K, 350K and 400K. For each gate bias voltage (Vg), we then obtain an Id vs T plot, from which we can extract the effective Schottky Barrier Height using the equation,

$$I_{DS} = AT^2 \exp(-q\phi_B/(k_B T))(1 - \exp(-qV_{DS}/(k_B T)))$$

This effective Schottky barrier height depends on Vg since the current also includes some direct tunneling as well as Fowler-Nordheim tunneling components. Plotting the effective Schottky Barrier Height versus the gate bias voltage, we can obtain the true Schottky Barrier Height in the flat-band condition as shown below.

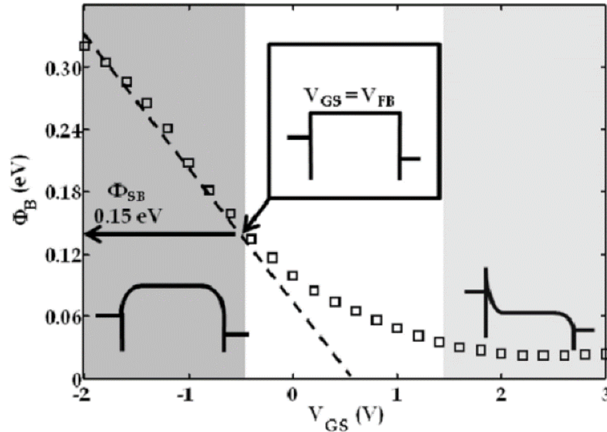


Fig 4. Effective Schottky Barrier Height for different gate bias – flat-band conditions occur at the point where the plot deviates from the linear trend [3].

Figure 4 shows the general behavior of the extracted effective Schottky Barrier height versus the gate bias. The point at which the curve deviates from the linear trend is where the device is at flat-band condition and the extracted barrier matches the true Schottky Barrier height. For our experiments, we perform Id-Vg measurements at the Janis probe station in Allen 152. The Janis can reach a medium to high vacuum ambient and can go down in temperature to 77K. We measured our devices at 200K, 250K, 293K, 350K and 400K.

2.4.1.1. Process flow for back-gated transistors

For our study, we fabricate back-gated transistors shown in Fig 5 (a) using the process flow described in Fig 5 (b).

1) Grow 90nm dry thermal oxide on p++ Si wafers.
2) Pattern alignment markers which would be used to make masks on the exfoliated flakes and to align those masks in later lithography steps.
    a. Spin coat LOL2000 at 3000 rpm for 60 seconds at Headway. Bake on a hotplate at 200°C for 5 minutes.
    b. Spin coat SPR3612 at 5500 rpm for 30 seconds at Headway. Bake on a hotplate at 90°C for 60 seconds.
    c. The alignment grid pattern is exposed using 90/-2 (dose/defoc) in Heidelberg.
    d. Post-exposure bake at 115C for 60seconds
    e. Develop for 35seconds in MF-26A
    f. Post-develop bake at 115C for 60seconds
    g. Ti/Au (5nm/40nm) is deposited in AJA evaporator.
    h. Lift-off is done by letting the samples sit in Remover PG overnight.
3) Exfoliate WS_2 or WSe_2 flakes either using blue-tape or gel-film and take optical images of the desired flakes.
4) Make device masks by aligning the optical images on the alignment grid mask.
5) Pattern the contact pads and coarse contact lines using the same steps as in (2) except that we deposit Ti/Metal instead of Ti/Au depending on the metal contact we want to study.
6) Pattern the fine contact lines using the same steps as in (2) except that we deposit only the metal whose contact we want to study. This 2-step lithography is used to avoid adhesion issues which we faced when study relatively non-reactive metals like Au, Pd and Pt.

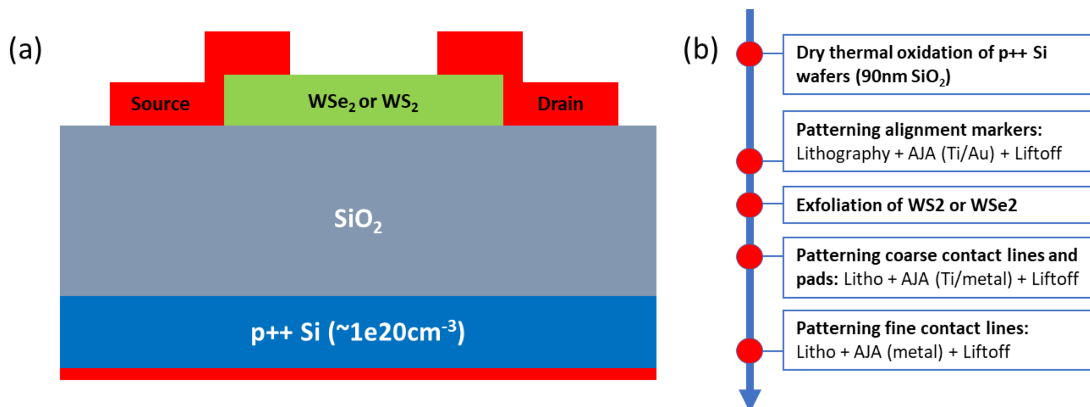


Fig 5. (a) Schematic of our back-gated transistor devices, (b) Process flow for our transistor devices

2.4.2. Pinning Study (Results)

We made devices with the following contact metals – Al, Cu, Ag, Ni, Au and Pd. Optical images of Pd/WSe_2 devices are shown in Fig 6. In our 1st run we used 1-step lithography to define our contacts. The devices with Al or Ni contacts showed no Id-Vg response. This could possibly be due to reaction between the metal and WSe_2 or WS_2. XPS would be required to confirm this hypothesis. We also faced lot of adhesion issues with Pd and Au. This led us to adopt the 2-step lithography process which incorporates a Ti adhesion layer underneath the contact pads and coarse lines. For the case of Cu/WSe_2, the copper metal completely lifted off, leaving behind just the WSe_2. This could be due to adhesion issues with Cu. However,

Cu/WS_2 process succeeded and the results of the Id-Vg measurements are shown in Fig. 7. We extract a Schottky barrier height of 253meV for Cu/WS_2

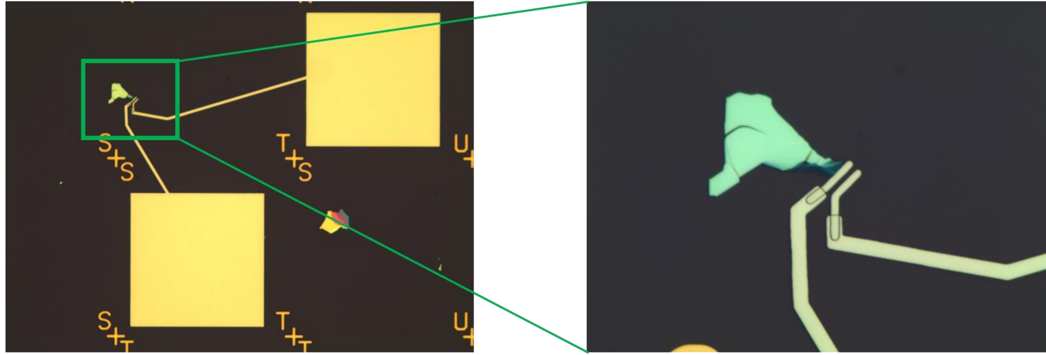


Fig 6. 20x and 50x optical images of a Pd/WSe_2 device with 1.5um channel length

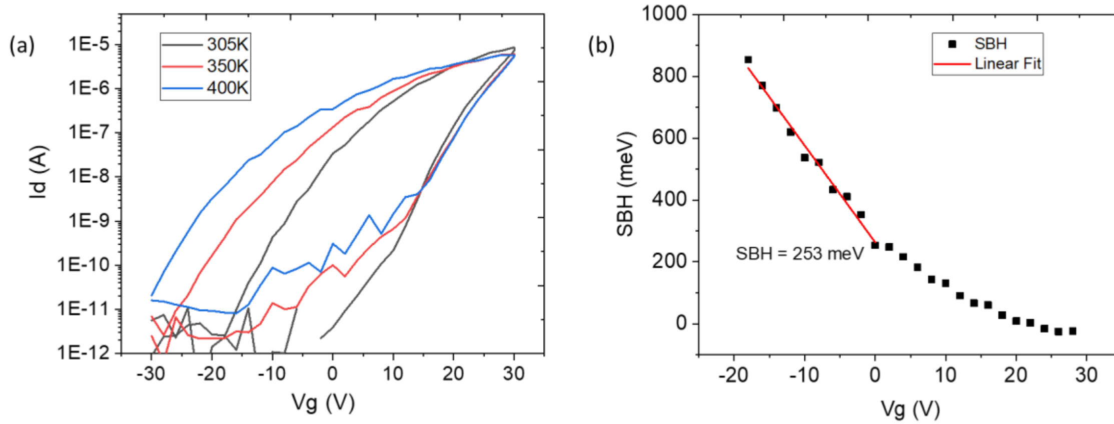


Fig 7. (a) Temperature dependent Id-Vg of Cu/WS_2 for 305K, 350K and 400K, (b) Extracted effective Schottky Barrier height versus gate bias

The case of Pd/WS_2 is interesting. We see the expected temperature-dependent behavior in the Id-Vg measurements. The Id-Vg and the Schottky barrier height as a function of gate bias are shown in Fig 7(a) and (b) respectively. The extracted SBH is 119meV which is lower than the value extracted from Cu/WS_2. This goes against our understanding of fermi-level pinning because a higher work-function metal would pin closer to the valence band. This intriguing result could be due to some reaction or organic residue at the interface, or just an artifact of the measurement system since the Id-Vg looks very noisy.

Another intriguing result we obtained was the anomalous temperature dependence of all WSe_2 transistors. Typically, you would expect the threshold voltage to reduce with temperature, since (1) the thermal generation of carriers in the semiconductor increases with temperature and (2) the Schottky contacts inject carriers through Schottky emission (see equation 1). In other words, for a given gate bias, the drain current should increase with temperature. However, we find that the drain current decreases with temperature for a given gate bias for all WSe_2 transistors. The Id-Vg of Au/WSe_2, shown in Fig 9, illustrates this. This anomalous phenomenon could be due to mobility degradation in the channel due to increased phonon scattering at higher temperatures.

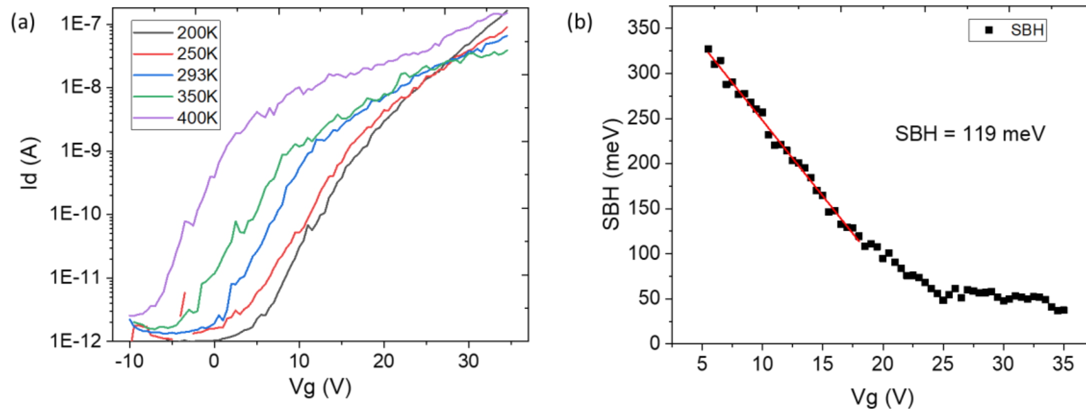


Fig 8. (a) Temperature dependent Id-Vg of Pd/WS_2 for 305K, 350K and 400K, (b) Extracted effective Schottky Barrier height versus gate bias

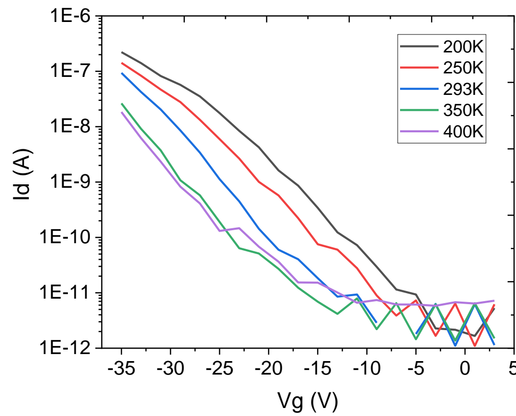


Fig 9. Anomalous temperature dependence of Id-Vg in Au/WSe_2 transistors.

Overall, we identify Ag to be the best n-type contact for WS_2 and Pd to be the best p-type contact to WSe_2. We were unable to show p-type conduction in WS_2 or n-type conduction in WSe_2. This is due to the strong pinning of metals in both semiconductors. This shows the importance of the next phase of our project where we would aim to de-pin the metal contacts using oxide interlayers – NiOx for p-type contacts and WoOx or ITO or ZnO for n-type contacts.

3. SOP

3.1. SOP Objective

The standard operating procedures for 1. Optimal TMD exfoliation on SiO_2 substrate, 2. Etching of TMD flakes, 3. Transfer from TMD flakes from SiO_2 substrate to a metallic substrate are explained in details.

All these SOPs are extremely useful for the growing group of SNF members who work on TMDs.

3.2. SOP Description

3.2.1. Optimal TMD exfoliation on SiO_2 substrate

The SNF instruction manual for Drytek2 and RTA explains all the procedures on how to use these tools. Hot plate is also very straightforward to use. Here, we will explain how to do the exfoliation using the blue tape or the gel film.

3.2.1.1. Exfoliation using blue tape (Figure 11)

1. Place the TMD crystal on a blue tape to exfoliate layers of TMD on top of the blue tape.
2. Place the SiO_2 substrate (face down) on top of a blue tape which has the TMD flakes on it.
3. Place a clean blue tape on top of the stack to fix the substrate in place. Your substrate is not fixed between two blue tapes.
4. Flip over the stack and gently press down on the flakes on the front face of the substrate.
5. In case you are doing hot plate anneal, place the stack on top of the hot plate (90°C) and let is stay for 2 minutes.
6. Very gently peel off the front-face blue tape. You will see some flakes being left on the substrate surface.
7. Cap the blue tape, which still has the flakes, with another similar-sized flake for use in the future.

Fig 10. A blue exfoliation tape containing WSe_2 crystals, prepared from a bulk WSe_2 crystal

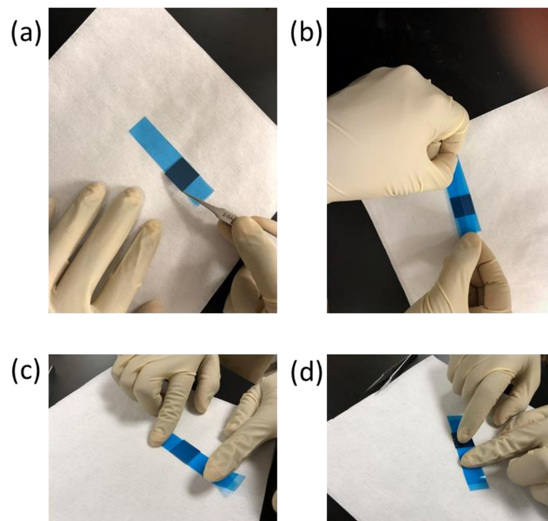


Fig 11. Step-by-step procedure for exfoliating using blue tape (a) Placing the substrate on the crystals on blue tape, (b) Sticking another strip of blue tape on the back side of the substrate, (c) Gently press using fingers around the edges of the substrate, (d) Flip over the substrate and very gently press on the substrate.

3.2.1.2. Exfoliation using gel film (Figure 12)

1. Peel off the plastic cover from the gel-film.
2. Place the blue tape containing TMD crystals onto the gel-film and gently press.
3. Remove the blue tape from the gel film – some crystals will be transferred onto the gel-film
4. Gently drop the gel-film onto the substrate and gently poke at one corner with a tweezer – the gel-film sticks onto the substrate through gravity and adhesion.

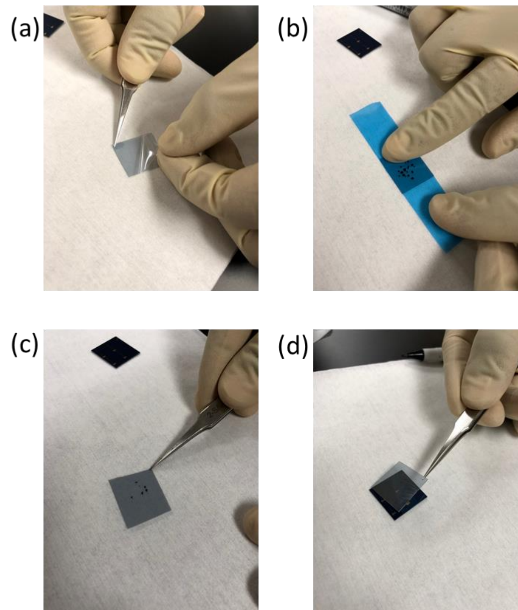


Fig 12. Step-by-step procedure for exfoliating using blue tape (a) Peeling off the plastic cover from the gel-film, (b) Placing the blue tape containing TMD crystals onto the gel-film and gently pressing, (c) The gel-film after removing the blue tape – some crystals have transferred onto the gel-film, (d) Gently drop the gel-film onto the substrate and gently poke at one corner with a tweezer – the gel-film sticks onto the substrate through gravity and adhesion.

3.2.2. Etching of TMD flakes

Etching process consist of a lithography (using Heidelberg) to define the etch patterns followed by an etch done at the pt-mtl.

For the lithography we followed the following steps:

- Resist Coating:
  - LOL 2000 (3000 rpm, 60 seconds on Headway)
  - 5 minute bake at 200°C
  - 3612 (5500 rpm, 30 seconds on Headway, resulting in a 1-um thick resist)
  - 1 minute bake at 90°C
- Exposure
  - Heidelberg (Dose: 70 J/cm^2, defocus: 0)
- Post-exposure bake
  - 1 minute bake at 115°C

- Develop
  - 1 minute in MF 26A solution
  - At least 1 minute in deionized water

The SNF instruction manual for pt-mtl explains all the procedures on how to use the pt-mtl. The recipe details can be found on table 6. For more information, please check out Koosha_SF6 recipe at pt-mtl.

Note that we are dealing with pieces rather than 4 inch wafers. In order to use pt-mtl, we need to mount the pieces on top of a carrier wafer using Kapton tape (figure 12). The use of Kapton tape is to physically and thermally attached the piece to the carrier wafer.

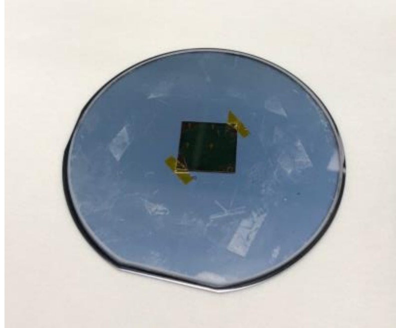


Fig 13. Using a 4 inch carrier wafer in order to etching on a piece using pt-mtl

3.2.3. Transfer from TMD flakes from SiO_2 substrate to a metallic substrate

This part is mainly adopted from the previous work done by Victoria Chen and Connor Bailey on SiO_2 substrate to SiO_2 substrate transfer of TMDs, with modifications tailored to our specific process.

1. Refill the load lock (LL) with N_2 and load samples. Close the LL and evacuate, ensuring the decrease of the LL pressure. Refill again (without opening) and evacuate again. Repeat this process 10x to ensure that as much oxygen is purged as possible. Never open both the evacuation and refill valve at the same time. In other words, cycle through: Open evac. valve→ wait to pump down→ close evac. valve→ open refill valve→ wait for pressure to rise→ close refill valve→ open evac. valve. (Repeat).

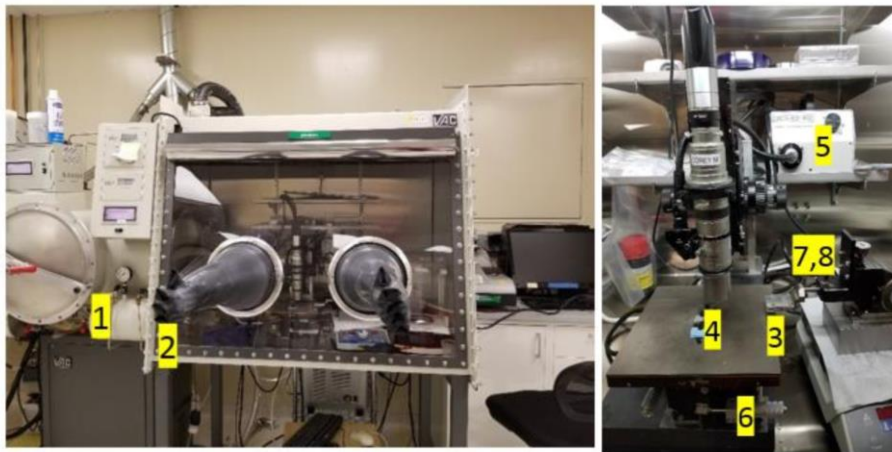


Fig 14. Glovebox components mentioned in the instructions

2. With the LL refilled and both valves closed, open the LL from the inside of the glovebox and take samples in. Close the LL and keep it evacuated.
3. Mount the glass slide/PDMS/PPC material onto the micromanipulator with the desired material facing down (towards the stage).
4. Place the first substrate onto the stage under the microscope.
5. Turn on the microscope light. The view will be displayed on the monitor on the table to the right of the glovebox.
6. Adjust the stage and micromanipulator in the x-y plane until the material is over the target substrate in the desired place – target flake.
7. Carefully lower the micromanipulator arm until the stamp is in contact with the target substrate.
8. Turn on heat if desired. Heater controls are located underneath the glovebox, and will heat the microscope stage if turned on. A typical value may be 55°C, and will depend on your target substrate and PPC.
9. After a few seconds, pull up the slide/PDMS/PPC stack. The target flake is expected to be attached to this stack.
10. Place the second substrate onto the stage under the microscope.
11. Adjust the stage and micromanipulator in the x-y plane until the material is over the target substrate in the desired place.
12. Carefully lower the micromanipulator arm until the stamp is in contact with the target substrate.
13. Turn on heat if desired. Heater controls are located underneath the glovebox, and will heat the microscope stage if turned on. A typical value may be 90°C, and will depend on your target substrate and PPC. A typical time to heat is 5 minutes, but will vary on your conditions.
14. After heating, the PPC should easily release and the stamp can be raised from the substrate, leaving behind the desired material onto the target substrate.
15. Unload the sample though the LL, making sure that the inside of the glovebox is never exposed to ambient. Always leave the LL evacuated.

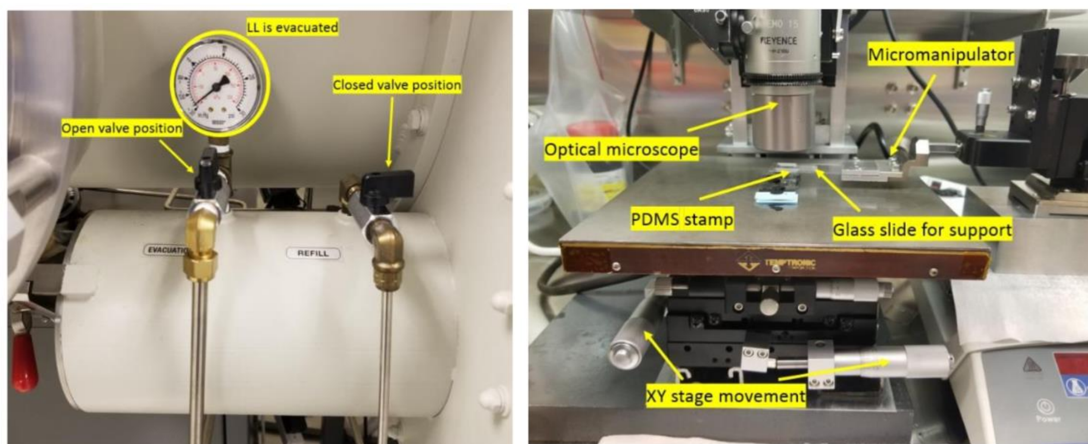


Fig 15. Various components of the glovebox

Additional notes:

- Retracting your arms from the gloves while the stamp is down will cause a pressure differential which will lead to vibrations in the glovebox that can hurt the transfer.
- Keep an eye on the oxygen and trace moisture levels in the glovebox. They are typically measured in ppm but at very high levels will be measured in %.
- The glovebox can be purged by opening the N2 valve located on top.
- If they remain at high levels for too long, samples inside the glovebox may degrade and a regen may be necessary.
- Solvents must be loaded in the solvent transfer container (with a pinhole on the lid).

- If solvents are used in the glovebox, make sure to close the inlet and outlet valves in the back of the glovebox to prevent catalyst damage.
- Always clean up when you are done using the glovebox, and do not heat materials on the stage that could melt.

4. Contributions

Although both students were involved in all the processes, the exfoliation and pinning study was mainly done by Aravindh Kumar while the etching and transfer studies were mainly carried out by Koosha Nassiri Nazif. The authors would like to most sincerely thank their mentors Hye Ryoung Lee, Archana Kumar and Michelle Rincon, the E241 teaching team, mentors and class for the valuable feedback and advice.

5. Finances

A summary of finances is listed in the table 7.

Table 7. Project Expenses

SNF	\$2383.51
XFab	\$1935.75
Ordered Materials	\$695
Total	\$5014.26
Requested Budget	\$5420.00

6. References

1. Li, H. et al. Rapid and reliable thickness identification of two-dimensional nanosheets using optical microscopy. ACS Nano **7,** 10344–10353 (2013).
2. Schulman, D. S., Arnold, A. J. & Das, S. Contact engineering for 2D materials and devices. Chem. Soc. Rev. 47, 3037–3058 (2018).
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