Chip-Scale Hermetically Sealed Photonic Devices

ENGR 241 Spring 2025
Final Report

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Table of Contents

1 Introduction

1.1 Motivations

Silicon photonics devices, and in particular optomechanical devices, are a promising platform for investigating novel quantum phenomena. The performance of these devices hinges largely on good confinement of light. Material quality is thus critical to the fabrication of performant silicon photonics devices.

A major limitation facing silicon photonics is that device exposure to the atmosphere results in slow oxidation of silicon surfaces, thereby forming a thin layer of uneven oxide. This induces scattering of light, resulting in devices with low quality factors. Furthermore, this process can also induce resonant wavelength shifts for on-chip photonic cavities, rendering them unusable for frequency-selective applications after extended periods of atmospheric exposure.

Traditional solutions are not always applicable - whereas silicon waveguides may sometimes be passivated by introducing a cladding layer, resulting in a lower index contrast between the waveguide and the cladding, causing a larger mode overlap with the cladding. Passivation via cladding is also antithetical to the creation of good optomechanical devices, since these devices must support free, undamped vibrations of the waveguide material over an extended region.

Here, we propose and develop a fabrication process to construct hermetically sealed encapsulations for silicon photonics devices. This seeks to address the above-mentioned issue of silicon oxidation by preventing device contact with the atmosphere entirely and storing the devices in a stable vacuum package.

1.2 Objectives & Schedule

Week	Milestones
1	● Version 1 of CAD (all masks). ○ Create nominal test structures. ● Tool trainings: ○ HDPCVD. ○ PT-Ox.
2	● Characterization of etch and deposition rates. ○ HDPCVD: Silicon dioxide deposition rate. ○ Headway 3 spinner: SPR-3612 resist spin thickness. ● Calibration preparation. ○ Test chip dicing.
3	● Version 2 of CAD (all masks). ○ Add new test structures. ● Optical lithography. ○ Determine Heidelberg 2 SOP for surface preparation. ● Characterization of etch and deposition rates. ○ PT-Ox: SPR-3612 resist etch rate. ● **Wafer 1**. ○ HDPCVD: Silicon dioxide deposition. ○ Heidelberg 2: Attempt M1 optical lithography.
4	● Characterization of etch and deposition rates. ○ PT-Ox: Silicon dioxide etch rate. ● **Wafer 1**. ○ Heidelberg 2: Complete M1 optical lithography. ○ PT-Ox: M1 oxide etch.
5	● Characterization of etch and deposition rates. ○ HDPCVD: Amorphous silicon deposition rate. ○ Ox-35: Amorphous silicon etch rate. ○ Headway 3 spinner: SPR-220-3 resist spin thickness. ● Tool trainings: ○ SVG Coat & Develop Tracks. ○ Gemini SEM. ● **Wafer 1 (PANDORAS01)**. ○ Dice into 4 quadrants: PANDORAS01 Q1-Q4. ○ HDPCVD: Amorphous silicon deposition of varying thicknesses. ○ Heidelberg 2: Complete M2 optical lithography. ● **Wafer 2 (PANDORAS02)**. ○ HDPCVD: Silicon dioxide deposition.

	○ Heidelberg 2: Complete M1 optical lithography. ○ PT-Ox: M1 oxide etch.
6	● Heidelberg 2 optical lithography calibration. ○ Dose & defocus matrix. ● **Wafer 1 (PANDORAS01)**. ○ Ox-35: M2 amorphous silicon patterns. ○ Wet etch (49% HF): Attempt to release amorphous silicon cap. Unsuccessful. ● **Wafer 2 (PANDORAS02)**. ○ Dice into 4 quadrants: W2Q1-W2Q4. ● **Wafer 3 (PANDORAS03)**. ○ HDPCVD: Silicon dioxide deposition. Opted not to continue with this film thickness.
7	● Version 3 of CAD (all masks). ○ Introduce refinements to preserve structural integrity. ● **Wafer 4 (PANDORAS04)**. ○ HDPCVD: Silicon dioxide deposition. ○ Heidelberg 2: Complete M1 optical lithography. ○ PT-Ox: M1 oxide etch. ○ HDPCVD: Amorphous silicon deposition.
8	● **Wafer 4 (PANDORAS04)**. ○ Heidelberg 2: Complete M2 optical lithography. ○ Ox-35: M2 oxide etch. ○ Wet etch (6:1 BOE): Attempt to release amorphous silicon cap. Unsuccessful. ● **Wafer 5; already prepped with thermal oxide (PANDORAS05)**. ○ Heidelberg 2: Complete M1 optical lithography. ○ PT-Ox: M1 oxide etch. ● Tool trainings: ○ LPCVD. ○ Corrosives wet bench.
9	● **Wafer 5 (PANDORAS05)**. ○ LPCVD: Polysilicon deposition. ○ Heidelberg 2: Complete M2 optical lithography. ○ Ox-35: M2 oxide etch. ○ Dice into 4 quadrants: PANDORAS05 Q1-Q4. ○ Dice Q1 into 7 chips. ○ Wet etch (20:1 BOE): Attempt to release amorphous silicon cap on Q1Chip2. Successful. ○ Wet etch (6:1 BOE): Attempt to release amorphous silicon cap on Q1Chip6. Successful.

10	● Imaging and confirmation of results. ○ SEM imaging of released structures.

The ENGR 241 class provided an excellent opportunity to develop a new encapsulation process tailored to the requirements of silicon photonics. Taking inspiration from prior works in the MEMS community in encapsulating devices [1-3], our process is based on an airtight Si sealing cap (more details in Section 2). Acknowledging the 10-week schedule constraint, we centered our efforts on creating the encapsulation structure instead of full optical device integration.

2 Fabrication Process Development

We dubbed our project “Photonic-Acoustic Nano-Device (film) Overlay for Robust Airtight Sealing” (PANDORAS), reflecting our goal of building a chip-scale structure that encapsulates optomechanical devices in a vacuum environment and is never exposed to the atmosphere.

Over the quarter, we had five fab iterations in total, denoted PANDORAS01 to PANDORAS05, in chronological order. PANDORAS05 is the last iteration of the quarter; in this run, we successfully realized a self-supported encapsulation structure with oxide fully released after multiple wet etch attempts, achieving our project objective and deliverables.

In this Section, we will first introduce our finalized process and provide intuitions on the design. Then, we will dive into our development process in chronological order. We will elaborate on the intended process for each iteration, the difficulties we encountered, and how we overcame the bottlenecks and improved our process in the following iteration.

For explicit fabrication details and steps, please refer to our Standard Operating Procedure (SOP) in the Appendix.

2.1 Overview of Finalized Process

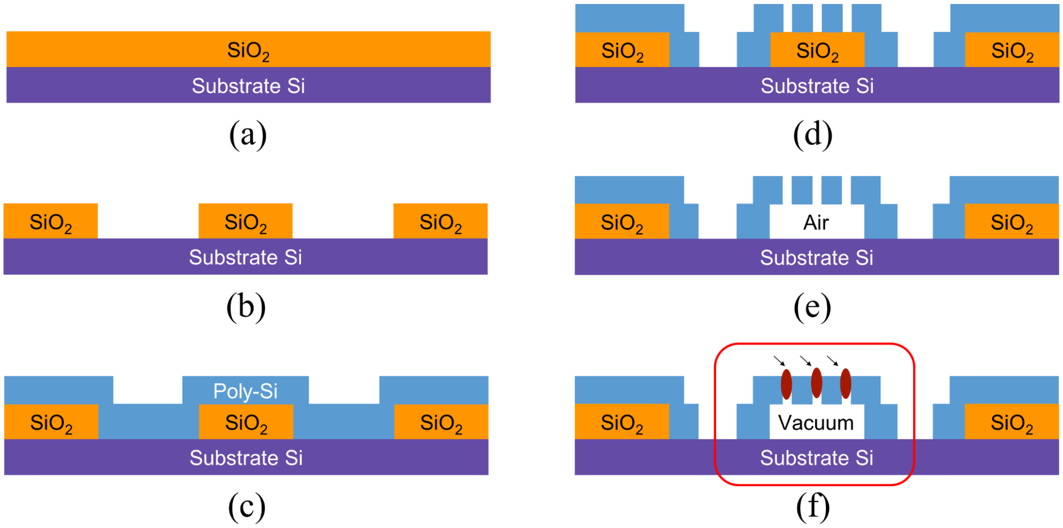


Fig. 2.1-1 Finalized process flow realized in the PANDORAS05 fab run.

a. Deposit a thin film of sacrificial silicon dioxide on the substrate Si.
b. Pattern and etch mask 1 (M1) in the silicon dioxide layer.
c. Deposit a thin film of polysilicon (poly-Si) to form the cap layer.
d. Pattern and etch mask 2 (M2) perforations and trenches in the poly-Si layer.
e. Release encapsulation structure using HF-based wet etch.
f. Angled deposition of metal to hermetically seal encapsulation. (This step was not attempted during the 10-week class session.)

2.2 Mask Design

Version 1 Nominal Design

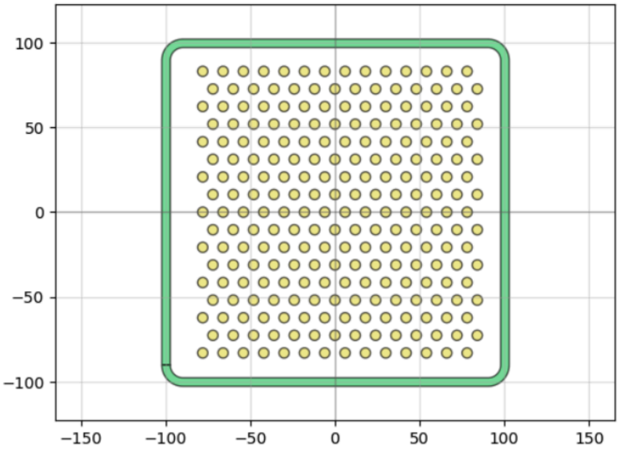


Figure 2.2-1 Version 1 CAD for nominal encapsulation structure.
Green: silicon dioxide etch (M1). Yellow: cap silicon etch (M2).

Features:

- M1: Silicon dioxide etch corresponds to step (b) in the process.
- M2: Cap silicon etch corresponds to step (d) in the process.

Version 3 Finalized Nominal Design

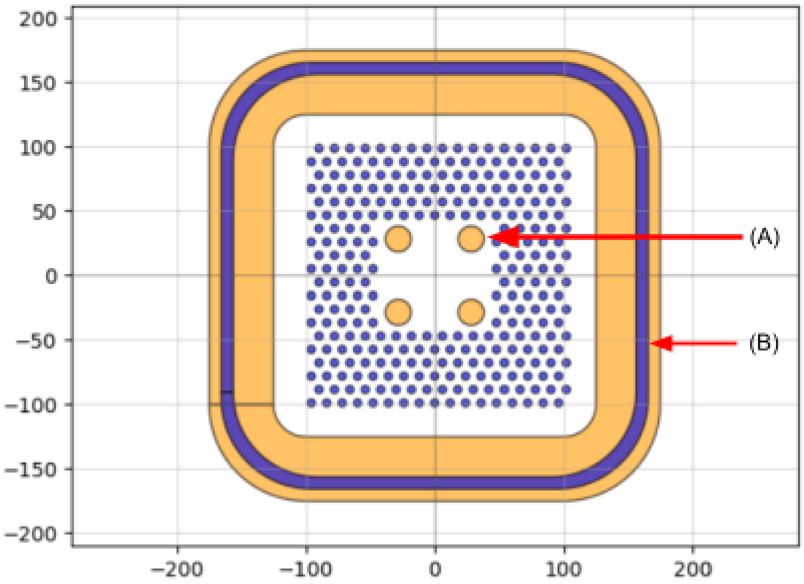


Fig. 2.2-2 Version 3 CAD for nominal encapsulation structure.
Deep yellow: silicon dioxide etch. Purple: cap silicon etch.

Revisions:

- Label (A): Addition of silicon dioxide etch holes for cap supports.
    - Enables LPCVD polysilicon to come into contact with the substrate, forming a supporting element for the suspended encapsulation structure after HF release.
- Label (B): Addition of film-stress release trench feature.
    - During the fabrication of wafer 1 & wafer 4, we noticed that the amorphous Si film delaminated during the HF release step. Our hypothesis for this was that the poor adhesion of the Si film in one region of the wafer allowed the film to be lifted by the HF. Subsequently, the film stress may have propagated across the wafer and led to the delamination of the cap Si for all the test structures, as seen in Fig. 2.2-3 below.
- Wider trenches.
    - Larger contact patch between cap Si and substrate Si enables better film adhesion.

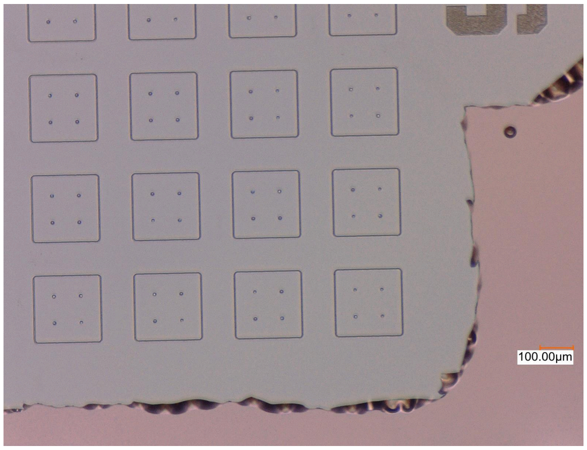


Fig. 2.2-3 Delaminated cap Si layer following 49% HF release of structures.

Design Variations for Parameter Sweeps

In addition to the nominal encapsulation structures shown above, we designed variations of the encapsulation to assess the effect of different parameters on our process.
These other structures include:

- Long bar structures.
    - These facilitate easy access to cross-sectional profiling of the deposited layers.
- Hatched / circular perforations - varied length and width.
    - We anticipate that perforations with larger areas facilitate better access of wet etchant to the sacrificial oxide layer, but at the cost of lowering the cap's structural rigidity.

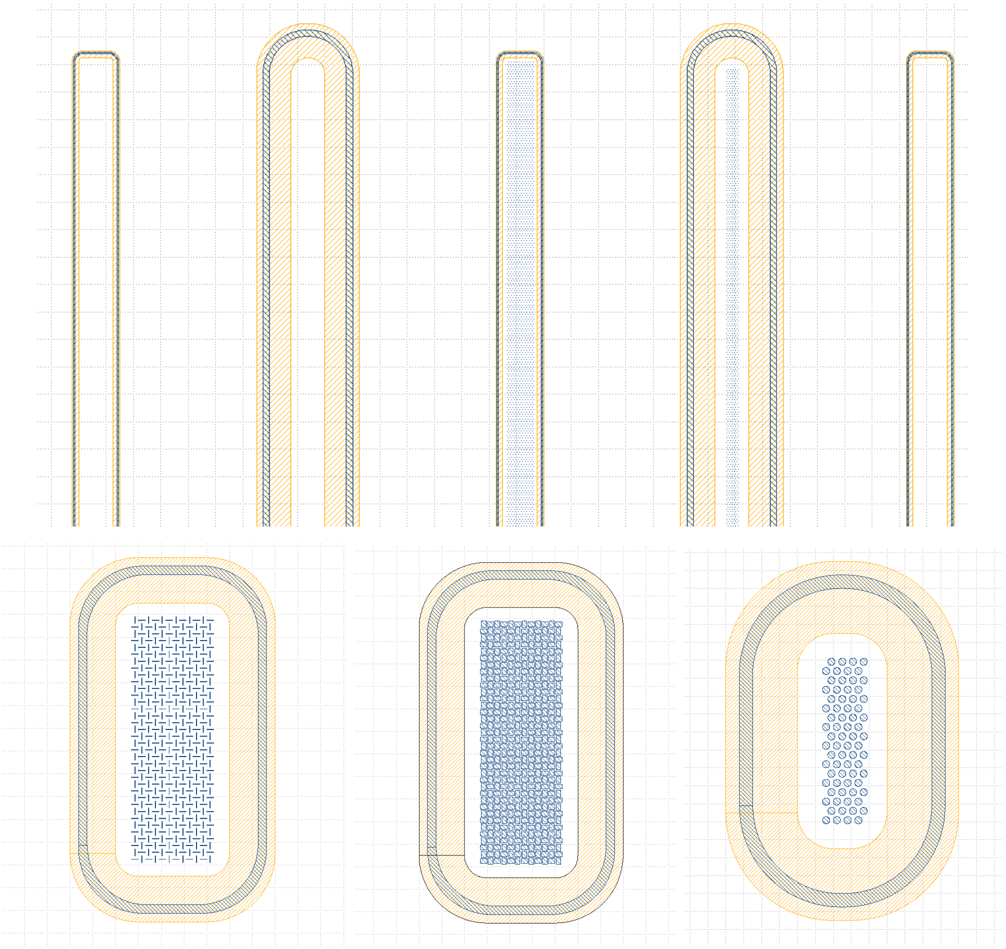


Fig. 2.2-4 CAD of varied structures.
Top: Upper section of long bars, with and without cap perforations.
Bottom, left: Hatched perforations, thin. Bottom, middle: Hatched perforations, wide.
Bottom, left: Circular perforations, wide.

2.3 Methods - Determining Etch and Deposition Rates

As material thicknesses were integral to the success of our project, we opted to characterize various material deposition and etch rates prior to running the process on our wafer samples. Our characterization process was the following:

1. Gather 4x chips of preferred substrate material.
    a. For characterizing silicon dioxide, the substrate material must be opaque - we opted for Si chips of size 6mm by 9mm.
    b. For characterizing silicon, the substrate material must be transparent - we opted for fused silica chips of size 10mm by 10mm.
2. Place one chip on a carrier wafer and begin a 1-minute deposition process in the chosen tool.
3. Remove the carrier wafer and chip from the tool. Characterize deposition thickness using a preferred measurement tool across at least 4 points on the surface of the chip.
    a. For characterizing silicon dioxide, we used Nanospec and Filmetrics to optically determine the deposited material thickness.
    b. For characterizing silicon, we used a Woollam ellipsometer.
4. Place the same chip on a carrier wafer and begin a 30s etch process in the chosen tool.
5. Remove the carrier wafer and chip from the tool. Measure remaining material thickness using the preferred tool, across at least 4 different points on the test chip. Average this and subtract it from the original thickness. This gives the etch depth.
6. Repeat steps 3 to 5 with varying deposition and etch times, and plot graphs with linear fit of deposition thickness/etch depth against time.
    a. N.B. It is recommended to randomize the order in which etch and deposition times are swept in experiments. This reduces the likelihood of correlated errors between successive experiments.

The results of these experiments are outlined in Section 3.2.

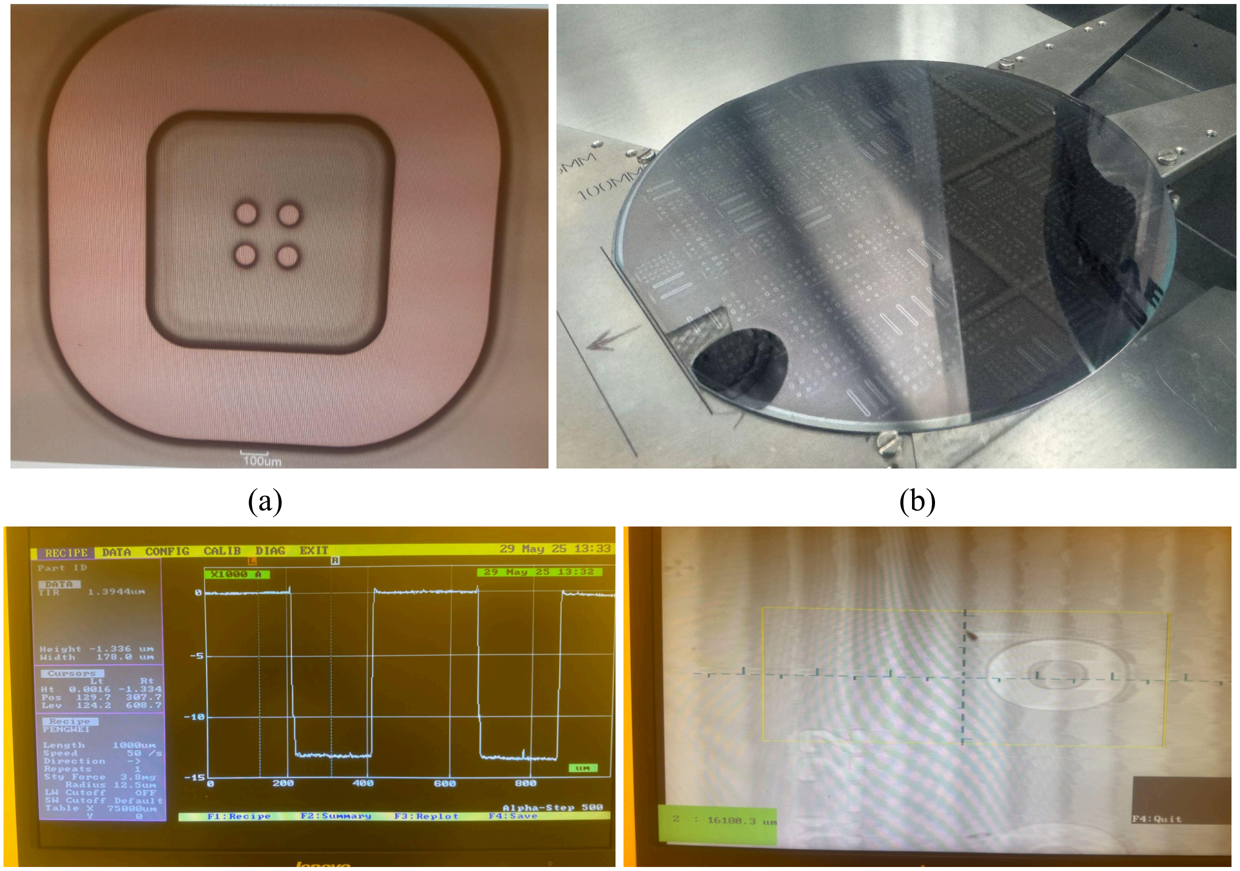
3 Results and Discussion

In this Section, we will elaborate on the process characterizations of the PANDORAS05 fab run, which is the final run and the first successful complete run in this quarter.

3.1 Process Verification and Characterization Pre-Oxide Release

We start with the thermal oxide-on-Si wafer supported by SNF staff members Neel Mehta and Rachelle Salmani. The thermal oxide was annealed in the Tystar Bank 3 Tube 9 furnace with a target thickness of 1 µm. We measured the oxide thickness to be 1.06 µm using Nanospec.

M1 Optical Lithography – Process Step (b)



```
29 May 25 13:33
Part ID
DATA
TIR      1.3944um

Height -1.336 um
Width   178.0 um

Cursors
       Lt      Rt
Ht  0.0016  -1.334
Pos  129.7   307.7
Lev  124.2   608.7

Recipe
PENGWEI

Length      1000um
Speed        50 /s
Direction     ->
Repeats       1
Sty Force   3.8mg
   Radius  12.5um
LW Cutoff      OFF
SW Cutoff  Default
Table X    75000um
      Y         0

29 May 25 13:32
```

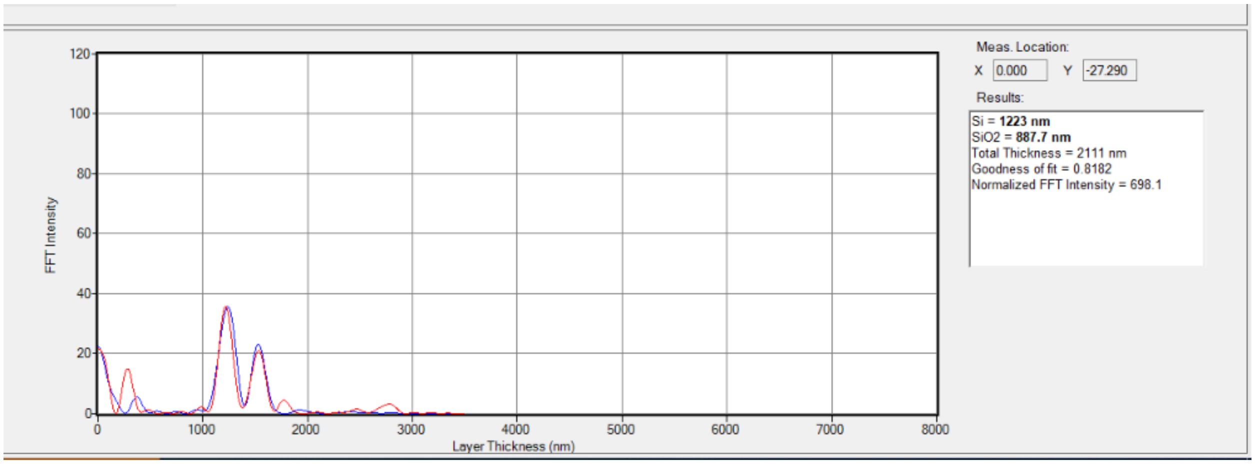
```
Z : 16180.3 um
```

(a) (b)

(c) (d)

Fig. 3.1-1 (a) Top-view of one encapsulation structure post developing after Heidelberg exposure of M1 mask. (b) The PANDORAS05 wafer post-oxide etch in PT-Ox. (c) Profilometry characterization post-oxide etch in PT-Ox across the structure shown in (d), showing a trench depth of 1.3 µm. Profilometry was carried out across these patterned encapsulation structures to determine if the sacrificial oxide layer was successfully cleared out from the trenches.

Material Thickness after Poly-Si Deposition – Process Step (c)

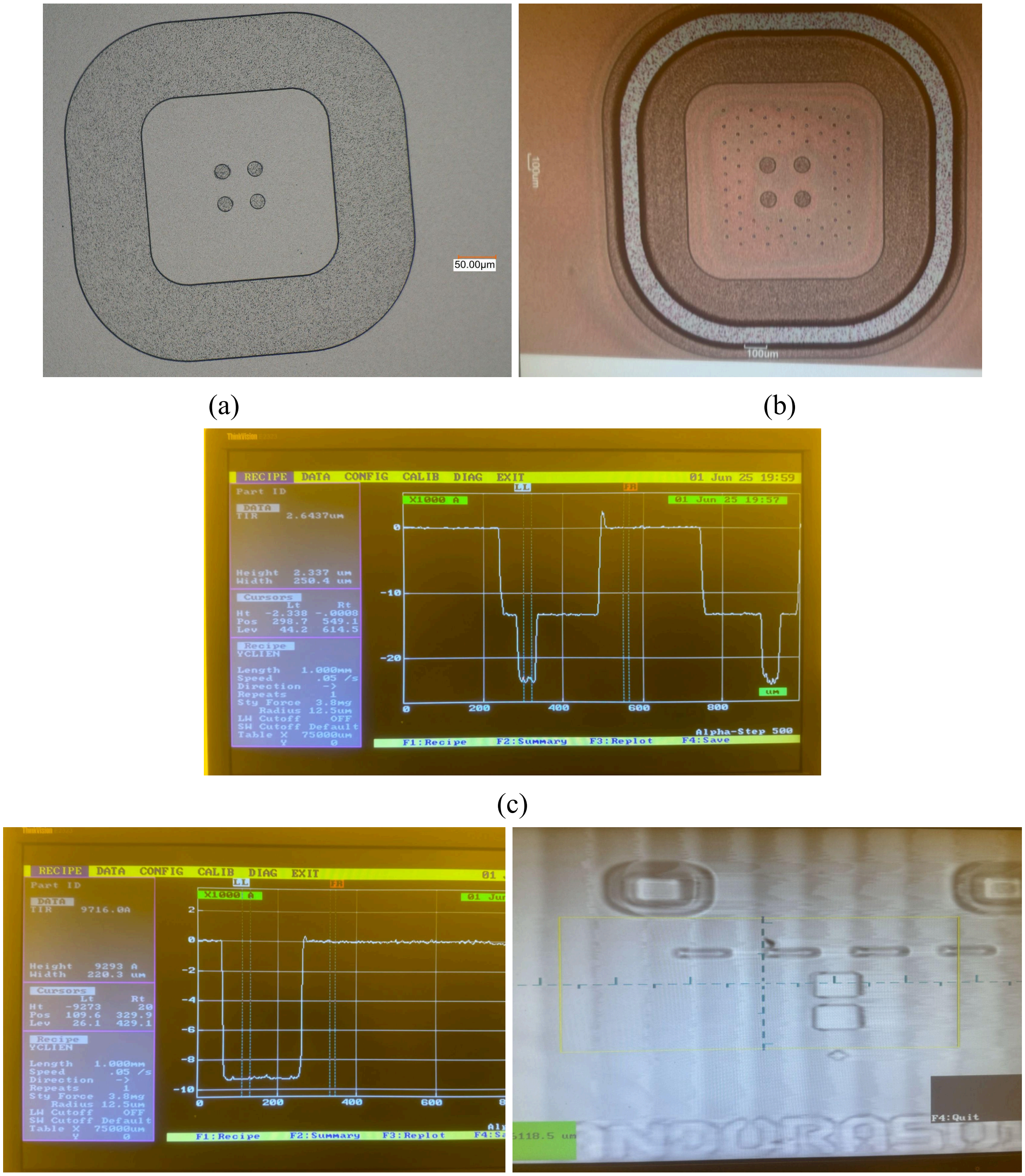


X 0.000 Y -27.290

Si = **1223 nm**
SiO2 = **887.7 nm**
Total Thickness = 2111 nm
Goodness of fit = 0.8182
Normalized FFT Intensity = 698.1

Fig. 3.1-2 Filmetrics two-layer fitting to long-wavelength spectrum (> 600 nm) with FFT analysis. The goodness of fit is about 0.82, which is not super great, but this gave us an approximate sense of how thick the Si cap layer is. The fitting suggested that the poly-Si cap thickness is about 1.223 µm and the sacrificial oxide layer thickness is about 887.7 nm. We aimed to deposit 1 µm of poly-Si with a 5% overhead to ensure structural integrity. Considering the goodness of fit, this validated that we have a thick enough Si cap layer for processing.

M2 Optical Lithography – Process Step (d)



(a)

(b)

```
Part ID
DATA
TIR      2.6437um

Height   2.337 um
Width    250.4 um
Cursors
            Lt       Rt
Ht     -2.338  -.0008
Pos     298.7   549.1
Lev      44.2   614.5
Recipe
YCLIEN

Length     1.000mm
Speed         .05 /s
Direction      ->
Repeats         1
Sty Force   3.8mg
    Radius 12.5um
LW Cutoff      OFF
SW Cutoff  Default
Table X    75000um
      Y          0
```

(c)

```
Part ID
DATA
TIR      9716.0A

Height    9293 A
Width    220.3 um
Cursors
            Lt       Rt
Ht      -9273       20
Pos     109.6    329.9
Lev      26.1    429.1
Recipe
YCLIEN

Length     1.000mm
Speed         .05 /s
Direction      ->
Repeats         1
Sty Force   3.8mg
    Radius 12.5um
LW Cutoff      OFF
SW Cutoff  Default
Table X    75000um
      Y          0
```

(d)

(e)

Fig. 3.1-3 (a) Microscope image of encapsulated structure after depositing poly-Si in the LPCVD. (b) Microscope image of encapsulated structure after patterning and developing the resist on the cap layer and stress-release trench. (c) Profilometer measurement of depth profile across the etched structure in (b), after stripping the resist. (d) Profilometer measurement of depth profile across the etched structure in (e), a test square exposing the sacrificial oxide beneath.

3.2 Deposition, Etch, and Release Rate Characterizations

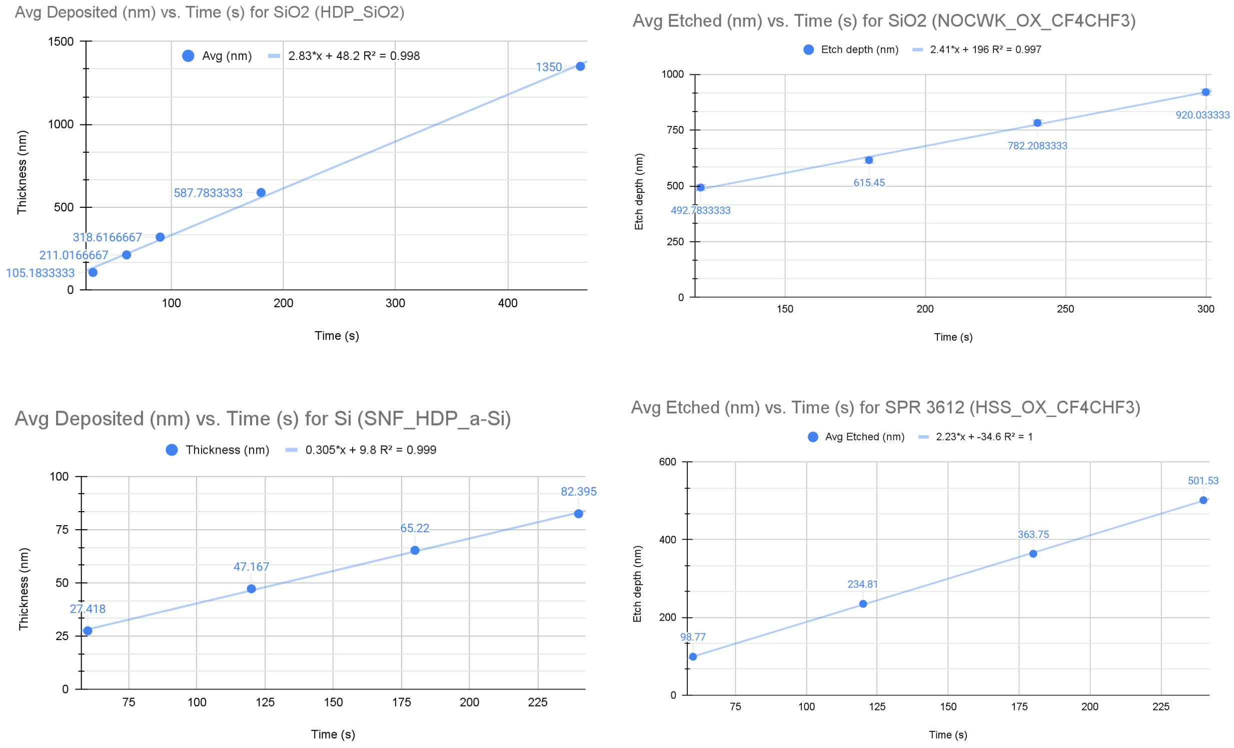


Fig. 3.2-1 Preliminary etch and deposition rate tests.
Each data point is an average across ~4 points on each test chip.

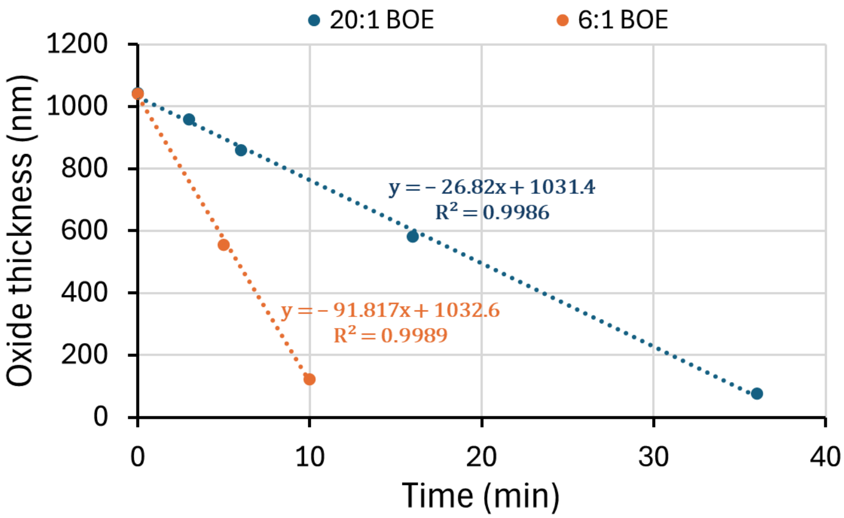
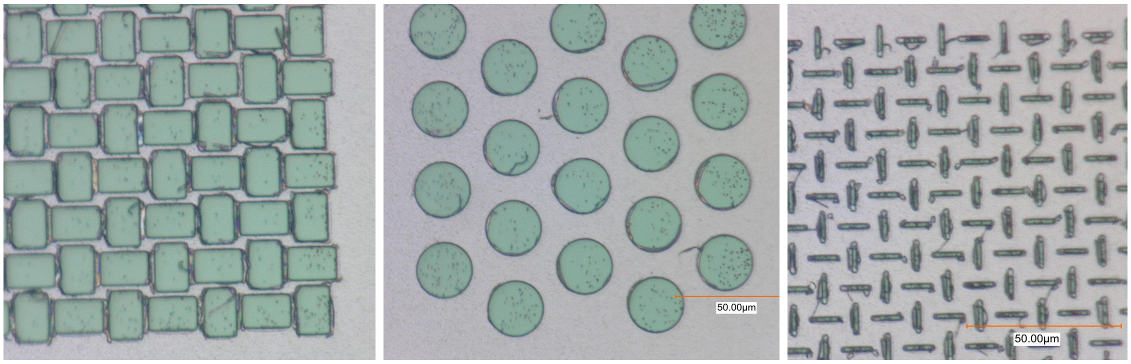


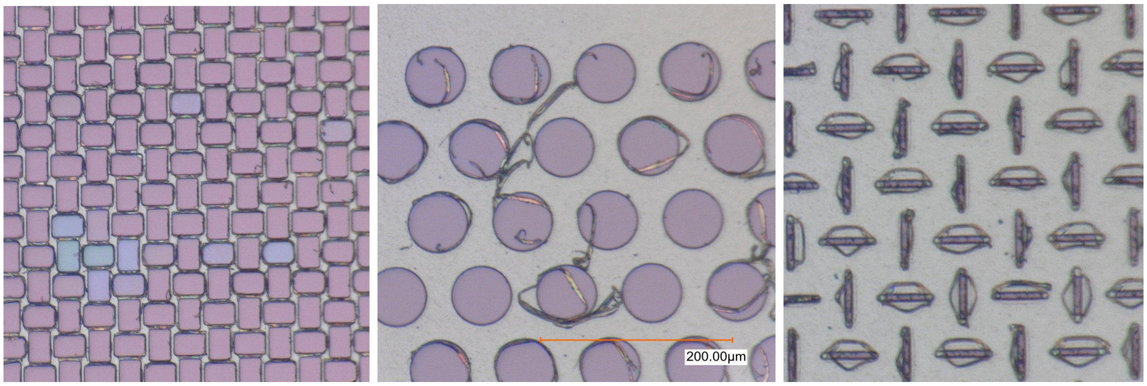
Fig. 3.2-2 Measured silicon dioxide wet etch rates for Wafer 5 structures.
The oxide film thickness was measured with Nanospec.

20:1 HF etch (Chip 2).

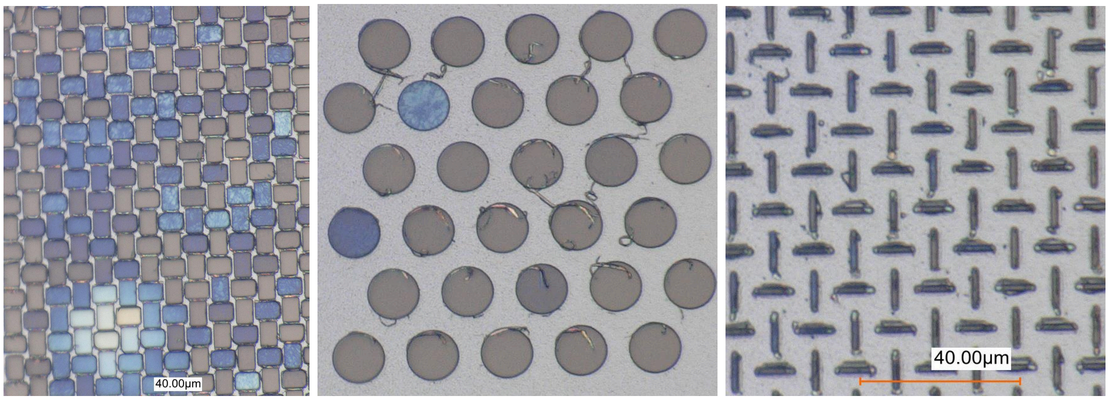
After 3 min. Remaining oxide thickness: ~ 960 nm.



After 6 min. Remaining oxide thickness: ~860 nm.

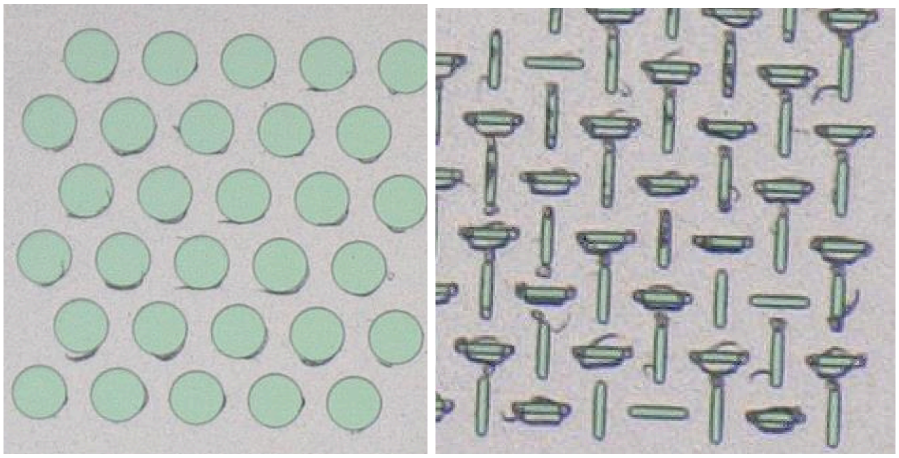


After 36 min. Remaining oxide thickness: ~70 nm in regions without blue coloration. Areas of blue coloration suggest a thicker amount of remaining oxide.

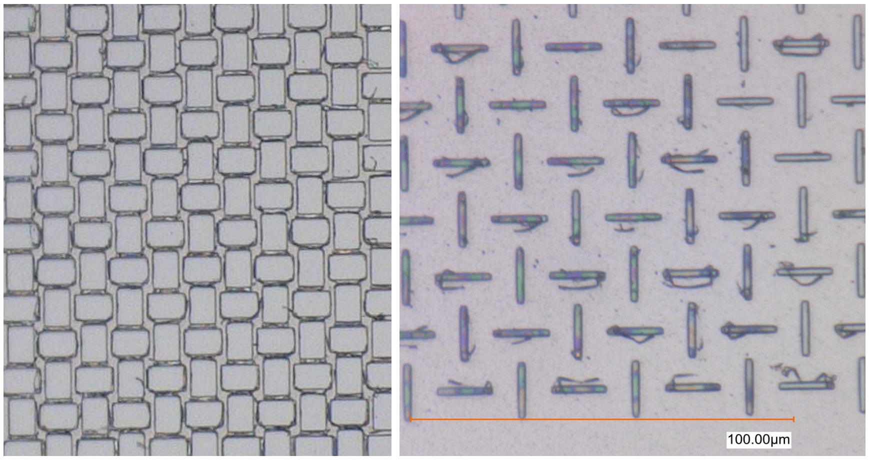


6:1 Buffered oxide etch.

Chip 5 after 5 min 6:1 BOE. Remaining oxide thickness: ~550 nm.



Chip 6 after 10 min 6:1 BOE. Remaining oxide thickness: ~80 nm.



Note on Resolving the Underetch Issue

After we etched in Ox-35 for 12 minutes, stripped the resist, and diced the wafer into smaller samples, we attempted to release the oxide using 20:1 BOE. We inspected the oxide thickness using a profilometer and didn't measure the thickness difference before and after the etch.

Because the Nanospec reading showed "out of range" when using the "Oxide on Silicon" recipe, we suspected that we might have underetched the Si release holes. We then put one test chip back into Ox-35 for an additional etch of 3 minutes universally without a mask. After this etch, we inspected under Nanospec again and got a reading of ~1.04 µm, suggesting that we finally etched through the Si layer this time. We then repeated this step across all of our samples in the PANDORAS05 fab run before further oxide release attempts.

3.3 Scanning Electron Microscope (SEM) Results

We then examined the cross-section of the released encapsulation structure using the Zeiss Gemini 560 scanning electron microscope (SEM) at SNSF.

With the help of LINQS member Kaveh Pezeshki, we carved scribe lines using an ultraviolet laser cutter for high-precision cleaving of the released chips. The black lines in Fig. 3.3-1(a) are scribe lines that are later used for precise cleaving. After cleaving, we then mounted four cleaved samples onto the 90° SEM stage, as demonstrated in Fig. 3.3-1 (b).

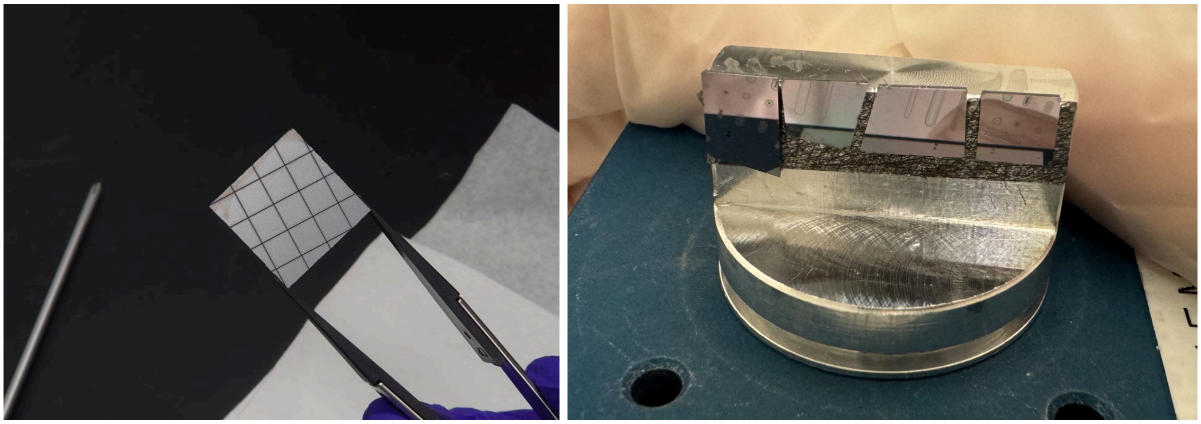
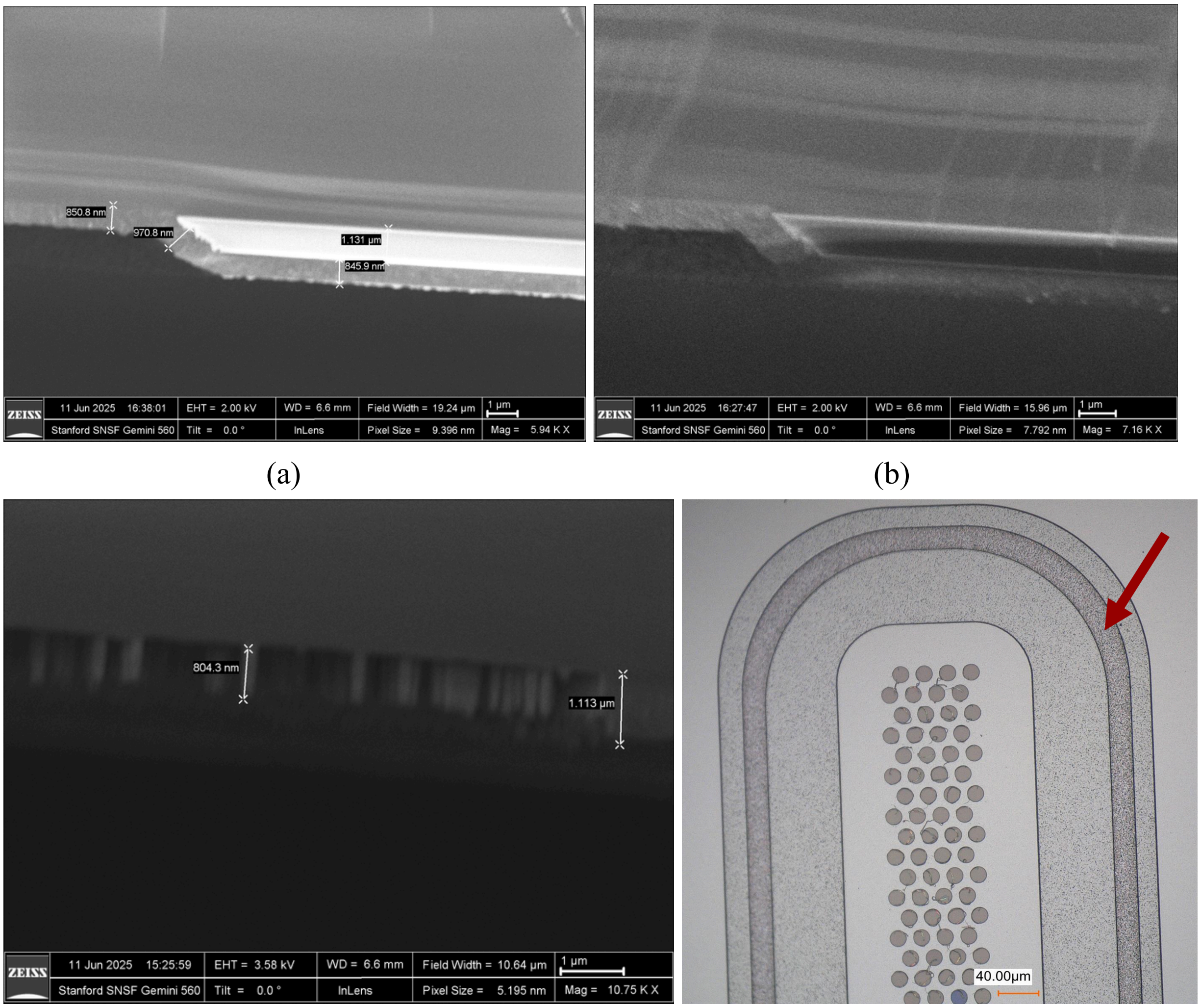

(a) (b)

Fig. 3.3-1 (a) Back side of one released chip (Chip 2) from PANDORAS05 with scribe lines for cleaving. (b) Four cleaved chips mounted on a 90° stage for SEM.

In all four of the samples, scribe lines have cut through at least one encapsulation structure, allowing us to examine the cross-section of our structure. Fig. 3.3-2 shows the SEM images at different regions of interest.

Fig. 3.3-2(a) shows the SEM image at the corner of one unreleased encapsulation structure, where the bright white layer indicates the sacrificial oxide encapsulated between the top thick Si substrate layer and the approximately 850 nm thick poly-Si cap layer at the bottom. This cross-section corresponds to the intersection of two layer stacks, Poly-Si on SiO2 on Substrate Si and Poly-Si on Substrate Si, in Fig. 2.1-1 (c). This SEM image confirms that where the layer stacks intersect, we formed conformal material stacks near the corners, which is crucial for structural stability.



(a) (b)

(c) (d)

Fig. 3.3-2 SEM images (a) at the corner of one unreleased encapsulation structure, (b) at the corner of one released encapsulation structure, and (c) at the film-stress-released region, which corresponds to the dark-gray strip region pointed by a red arrow in (d).

Fig. 3.3-2(b) shows the SEM image of a released encapsulation structure at a similar region of interest as (a). In (b), we observed that the bright white sacrificial oxide layer in (a) is all removed, with the poly-Si cap layer remaining intact.

Fig. 3.3-2(c) shows a group of pillar structures etched into the poly-Si layer, which is on top of the Si substrate. We believe that these patterns correspond to dark gray regions (indicated by the red arrow) in the optical microscope image shown in Fig. 3.3-2(d). This is the place where we etch into the Si substrate to completely separate individual encapsulation structures and release the film stress.

In our recipe, we etched Si in Ox-35 to ensure all the release holes on top of the Si cap in these film-stress-released regions. Because of the high etch selectivity (more than 10:1) between Si and SiO2 in our HBr+Cl2-based etch recipe, wherever there are oxide flecks, the etch is slowed down at those places.

Therefore, one conjecture of the origin of these pillars is that residual resist, native oxide, or other dirt that lands on top of the poly-Si layer and stops the directional etching in Ox-35 at places with flecks, effectively forming the group of pillars in (c).

As we did not perform a piranha clean before growing poly-Si, another potential source of fleck could be photoresist from the patterning of M1. It could also be that residual thermal oxide landed on the Si substrate after we cleaned the chip surface with 2% HF, forming the fleck pattern in the dark gray region in Fig. 3.3-2(d). However, these contamination sources would only contribute to flecks between the poly-Si and Si substrate. The true cause of this phenomenon requires further investigation.

4 Conclusions and Future Work

Over the past ten weeks, the primary objective of this project was achieved. We successfully developed a complete and reproducible process for fabricating self-supported hollow encapsulation structures on a silicon wafer, including the release of the sacrificial oxide layer.

The fabrication sequence involved defining the structure through sacrificial oxide growth, optical lithography, and etching. A robust poly-silicon cap was then conformally deposited over the oxide blocks, ensuring strong adhesion to the silicon substrate. Finally, release holes were patterned and etched into the poly-silicon cap, which enabled the removal of the internal sacrificial oxide using a low-concentration wet etch.

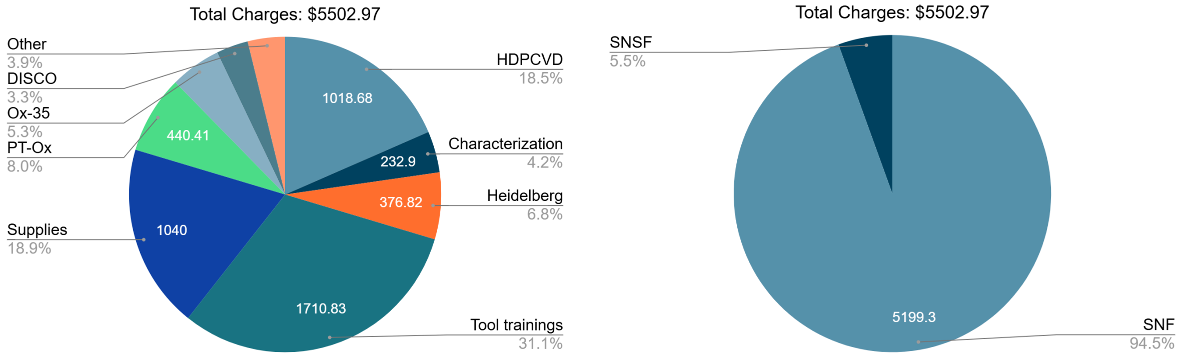
The robustness and reproducibility of this process were demonstrated successfully. The polysilicon cap structure remained intact after repeated wet etch attempts on a single chip and across multiple different chips, confirming the viability of our fabrication method. Process verification was conducted using a Nanospec to measure residual oxide thickness on test patterns, while optical microscopy and SEM imaging confirmed the structural integrity of the final, stable encapsulation structures.

The next phase of this project will focus on developing a metal sealing process for the release holes based on angle evaporation. The proposed tool for this process is the Kurt J. Lesker (KJL) E-Beam Evaporator at SNSF. Should smaller apertures be required, e-beam lithography presents a viable alternative.

The long-term objective is to adapt this encapsulation process for use with silicon-on-insulator (SOI) wafers. The ultimate goal is to achieve the hermetic sealing of functional optomechanical cavity devices, which could have applications in fields such as quantum information processing.

5 Budget and Expenses

Over the quarter, we conducted our project mainly utilizing the SNF-sponsored budget. We operated under a total SNF-sponsored budget of $5,500.00, comprising a base budget of $5,000.00 and a supplementary budget of $500.00. The detailed expense breakdown is shown in Fig. 5-1.



(a)

(b)

Fig. 5-1 SNF-sponsored budget usage breakdown (a) in terms of tool categories and (b) in terms of SNF/SNSF expenditures.

To reach our project objective and milestone, we are also supported by Prof. Amir Safavi-Naeini of the LINQS group for our out-of-budget expenses.

6 Acknowledgements

Our work was generously supported by the Stanford Nanofabrication Facility (SNF). We extend our sincere thanks to our mentors, Swaroop Kommera and Tony Ricco, for their patient guidance and for brainstorming with us through numerous challenges.

Swaroop provided critical insights into materials, tool choices, and process design that guided us through several bottlenecks. We are especially grateful for his accessibility and willingness to offer advice and discuss challenges whenever they arose. His suggestion to switch to thermal oxide and LPCVD polysilicon was key to our project's breakthrough.

Tony contributed many innovative ideas for our structural design, such as using circular release holes for better sealing without contamination. He frequently brainstormed with us, offering valuable perspectives on pattern design. His insights on sealing and vacuum characterization will be invaluable as we continue this project.

We also appreciate the prompt assistance and valuable advice from the SNF and Stanford Nano Shared Facilities (SNSF) staff. We thank Rachelle Salmani for training us on various etching and deposition tools, including the SVG tracks, and for providing useful advice. We are grateful to Lavendra Mandyam for guiding us through the advanced functions of the etch tools and explaining important principles of material deposition and etching. Neel Mehta's assistance in the project's later stages was a great help; he trained us to use the Tystar tubes and offered many useful processing tips. We are especially grateful to Neel and Rachelle, who generously donated several wafers with high-quality thermal oxide. Their support saved us significant time near the end of the quarter, allowing us to finish a full fabrication iteration within five days. We also thank Uli Thumser for her essential training on the corrosive wet benches, which enabled us to perform wet etch processes efficiently and with minimal risk.

We thank Professor Debbie Senesky for leading the course and for her unwavering support during times of budget constraints. Our gratitude also extends to course assistant Sergio Cordero and all ENGR 241 class members and mentors for their inspiration and assistance throughout this journey. Special thanks to Sara Azzouz for her help with the Woollam Ellipsometer. It was always motivating to see our fellow classmates in the fab, grinding through it together!

Finally, we thank all the members of the Laboratory for Integrated Nano-Quantum Systems (LINQS) who assisted and advised us throughout the quarter. Specifically, we thank Samuel Gyger for initiating and brainstorming this project with us from the very beginning. The earliest encapsulation design ideas and the initial process flow came from his brilliant mind. We also extend our gratitude to LINQS members (in alphabetical order) Helena Guan, Oliver Hitchcock, Ali Khalatpour, Kaveh Pezeshki, and Linus Woodard, for their insightful comments in refining our fabrication process design and for teaching us about tool operations, and we thank Professor Amir Safavi-Naeini for his continued support!

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Appendix I: Standard Operating Procedure

Self-Supported Chip-Scale Encapsulation in Silicon

Standard Operating Procedure

Nelson Ooi and Chou-Wei Kiang
Mentors: Swaroop Kommera and Tony Ricco
ENGR 241, Spring 2025

1. Fabricate photonic structures on a silicon / SOI wafer.
    a. Using your preferred lithography technique, fabricate waveguides and other photonic elements directly on a silicon-based substrate.
    b. If using SOI, do not release devices from oxide yet.
2. Deposit silicon dioxide.
    a. Enable the HDPCVD.
        i. Pre-cleaning.
            1. Load a dummy wafer (blank 4” quartz wafer) into the loadlock and close the lid.
            2. Chamber cleaning: Run Etchback for 5 min.
            3. Load a dummy wafer (blank 4” silicon wafer) into the loadlock and close the lid.
            4. Chamber seasoning: Run recipe SNF_HDP_SiO2 for 5 min.
        ii. Load the device wafer into the loadlock and close the lid.
        iii. Select recipe SNF_HDP_SiO2 and edit deposition run time for desired thickness: 1µm typically works for our purposes.
        iv. The calibrated deposition rate accurate as of May 30, 2025 is 2.83 nm per second.
3. Write etch mask 1 (M1).
    a. Spin.
        i. Enable the SVG Coat 1 & 2.
            1. Select the vapor prime recipe and run the wafer through the track.
            2. Select recipe for SPR 220-3 3.0µm and 2.0mm EBR, and run the wafer through the track.
        ii. Note: it may be useful to run a dummy wafer through the track first to ensure that hardened resist in resist nozzles.
    b. Expose.
        i. Enable Heidelberg2.
            1. Write M1 CAD patterns.

        2. Settings:
            a. Dose: 200 mJ / cm^2.
            b. Defocus: -2.
    c. Develop.
        i. Enable SVG Dev 1.
            1. Select recipe 7 for SPR 220-3 development using MF-26A.
            2. Select recipe 3 for 90s post-development hardbake.
    d. Measure resist thickness.
        i. Using the Nanospec, measure resist thickness at different points on the sample.
    e. Etch silicon dioxide.
        i. Pre-cleaning.
            1. Enable the PT-Ox.
            2. Load a dummy wafer (blank 4” silicon wafer) into the loadlock, close lid and pump down.
            3. Run O2 Clean for 5 min.
            4. Load a dummy wafer (blank 4” silicon wafer) into the loadlock, close lid and pump down.
            5. Run recipe NOCWK-OX_CF4CHF3 for 5 min.
        ii. Load device wafer into the loadlock, close lid and pump down.
        iii. Select recipe NOCWK-OX_CF4CHF3 and edit run time for desired etch depth: 1µm typically works for our purposes.
        iv. The calibrated etch rate accurate as of May 30, 2025 is 2.41 nm per second.
    f. Plasma ashing & resist strip.
        i. Load device wafer into Samco top shelf and run for 5 min.
        ii. Acetone & IPA clean resist for 5 min.
    g. Inspect structures.
        i. Use an optical microscope or Keyence.
4. Deposit polysilicon.
    a. Enable the B1T3 Flexible Poly LPCVD.
    b. Select the polysilicon recipe and run for desired deposition time: 1µm thickness is recommended.
        i. Load wafer into quartz wafer holder, after 8 min holder unloading is complete. The maximum loading time is 15 min.
            1. Ensure that the device wafer is sandwiched between two dummy wafers
        ii. The calibrated deposition rate accurate as of May 30, 2025 is 13.4 nm per second.
5. Write etch mask 2 (M2).

    a. Spin.
        i. Enable the SVG Coat 1 & 2.
            1. Select the vapor prime recipe and run the wafer through the track.
            2. Select recipe for SPR 220-3 3.0µm and 2.0mm EBR, and run the wafer through the track.
        ii. Note: it may be useful to run a dummy wafer through the track first to ensure that hardened resist in resist nozzles.
    b. Expose.
        i. Enable Heidelberg2.
            1. Write M2 CAD patterns.
            2. Settings:
                a. Dose: 200 mJ / cm^2.
                b. Defocus: -2.
    c. Develop.
        i. Enable SVG Dev 1.
            1. Select recipe 7 for SPR 220-3 development using MF-26A.
            2. Select recipe 3 for 90s post-development hardbake.
    d. Measure resist thickness.
        i. Using the Nanospec, measure resist thickness at different points on the sample.
    e. Etch silicon.
        i. Pre-cleaning.
            1. Enable the Ox-35.
            2. Load a dummy wafer (blank 4” silicon wafer) into the loadlock, close lid and pump down.
            3. Run O2 Clean for 5 min.
            4. Load a dummy wafer (blank 4” silicon wafer) into the loadlock, close lid and pump down.
            5. Run recipe LINQS-NOCWK-BT_only_Si for 5 min.
        ii. Load device wafer into the loadlock, close lid and pump down.
        iii. Select recipe LINQS-NOCWK-BT_only_Si and edit run time for desired etch depth.
    f. Plasma ashing & resist strip.
        i. Load device wafer into Samco top shelf and run for 5 min.
        ii. Acetone & IPA clean resist for 5 min.
    g. Inspect structures.
        i. Use an optical microscope or Keyence.
6. Dice sample into desired size.
    a. Enable the DISCO wafersaw.
    b. Set up dicing channels.

7. Wet etch sacrificial silicon dioxide.
    a. Enable the wbflexcorr-3 bench.
    b. Prepare 100 ml of 6:1 BOE in a Teflon dish.
    c. Prepare 3 other Teflon dishes with water for rinsing the etchant.
    d. Dip for desired etch time, we have found that 10 min works well to clear out the 1µm of deposited oxide.
    e. Rinse by successively placing the sample in each of the Teflon dishes with water, for 1 min each.
    f. Use the water nozzle to rinse off the sample, 3 times on each side.
    g. Safely clean the bench.

Steps remaining to be tested:

- KJL sputtering of Ti/Al getter metal to seal the encapsulation layer under vacuum.
- Vacuum test by probing deflection of Si cap.

Appendix II: Nanonugget

Nanonugget – Tips on Using DISCO Wafersaw

Nelson Ooi and Chou-Wei Kiang
Mentors: Swaroop Kommera and Tony Ricco
ENGR 241, Spring 2025

The DISCO Wafersaw is a convenient tool for dicing a full wafer or larger samples into smaller chips of customized dimensions. Blade dicing is a common and versatile technique that uses a high-speed rotating blade to cut through materials like silicon. The following tips are intended to help users achieve a smoother experience with the tool, especially when precise dicing of patterned wafers is required.

The demonstration below involves cutting a patterned silicon wafer with a hub blade. The material stack on the wafer consists only of silicon and silicon oxide.

<u>Tip 1: Dicing Resist</u>

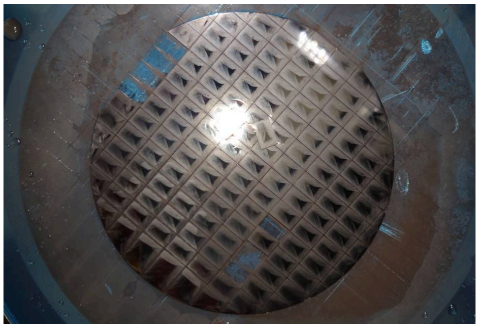
The dicing process generates significant dust and debris, while a simultaneous water spray cools the blade and removes particles from the cutting area.

To protect your device patterns from contamination, spin on a layer of baked photoresist (e.g., SPR-3612, SPR 220-3) before dicing. This resist acts as a protective layer.

- For 4-inch wafers, you could use SVGcoat tracks to spin the resist
- For smaller samples/chips, you can use the Headway spinner to manually spin the resist. Taping the sample on a blue dicing tape by adhering the backside of the sample to a blue dicing tape during the spin can help achieve a better vacuum level during the spin.

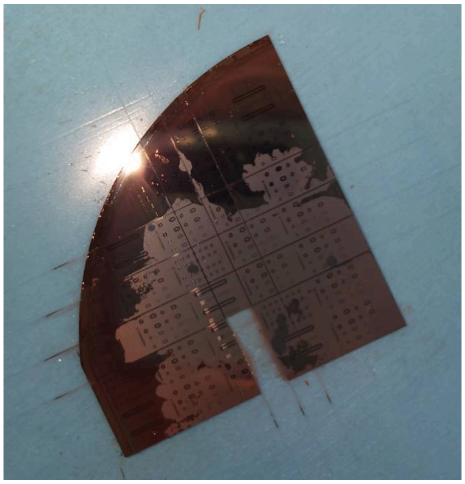
After the dicing is complete, the resist can be easily stripped with solvents like acetone and IPA, as it has not been exposed to plasma processing.

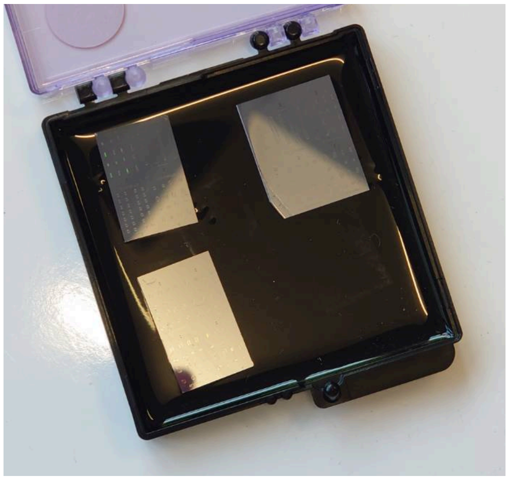
Chips diced without a protective resist layer show significant surface contamination.



After dicing with a resist layer and then stripping the resist, the chip surface is clean.

- On the left, there's no double-sided taping, and some chips flew away
- But after stripping the resist, we see that the chip is very clean on the right





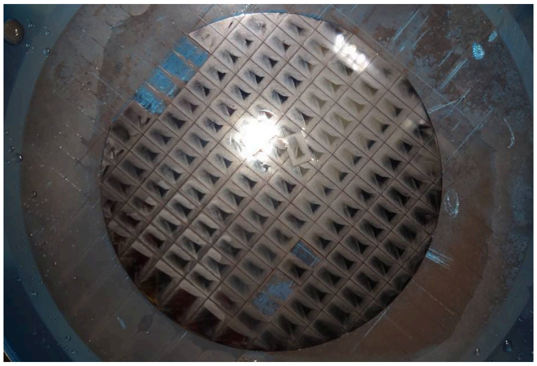
Tip 2: Double-sided manual taping

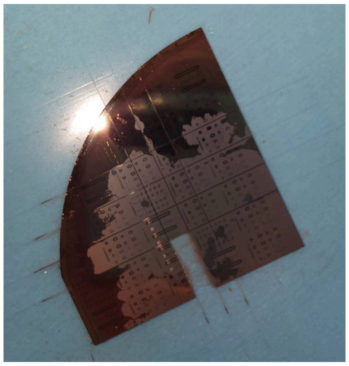
Typically, the backside of a wafer is adhered to blue dicing tape using the provided taping tool. This mounting process is critical, and care should be taken to avoid trapping air bubbles, which can cause material breakage during dicing.

A high water flow rate produces a cleaner cut but also exerts more force on the wafer. If your target chips are small (e.g., 6 mm x 9 mm), the water jet can blast them away. This can also happen if air bubbles are trapped between your sample and the dicing tape. To prevent this, consider using double-sided taping.

- Double-sided taping is recommended when dicing a wafer into small chips (e.g., a 4-inch wafer into 6 mm x 9 mm chips).
- Double-sided taping is not necessary when dicing a wafer into larger pieces, such as quadrants.

Example of no double-sided taping – some chips are blown away inside the tool somewhere



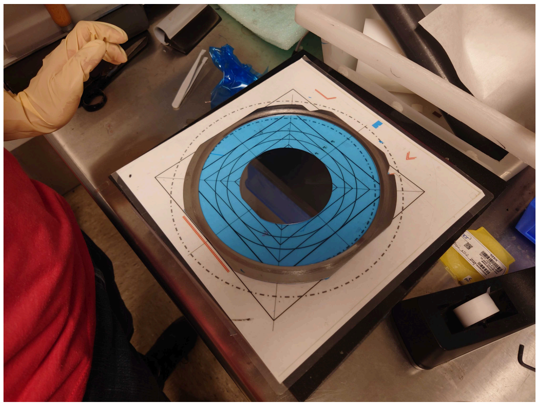


Here, we demonstrate the double-sided manual taping steps with photo illustrations below. Take one large piece of blue dicing tape and put it on the marble table.

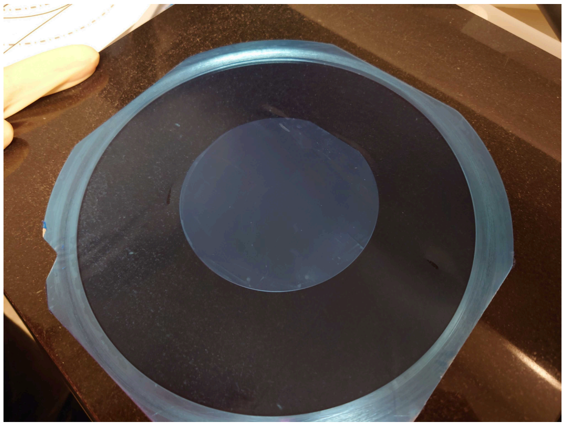
1. Align the gray circular ring on the tape. Use one hand to press one corner of the ring on the tape, and the other hand to pull on the corners of the tape to make sure that the tape is well extended and flat within the ring.

2. Carefully press the ring onto the tape. Use the presser to make sure the tape sticks well on the ring. The photo here shows the presser.

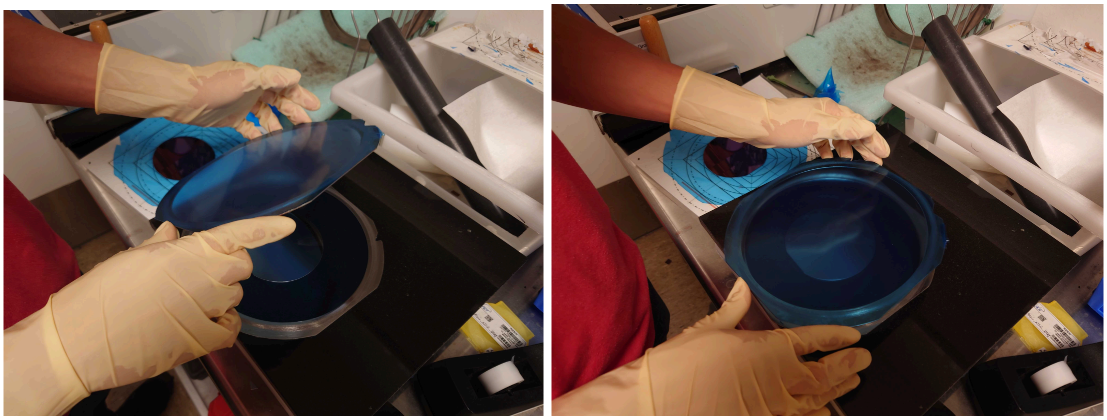
3. Use the alignment reference while adhering the backside of the wafer to the blue dicing tape



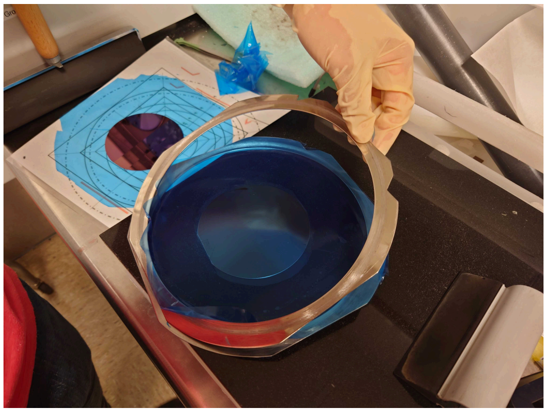
4. Flip the wafer and ring assembly over. Gently use the roller on the tape to press out any remaining air bubbles. The goal is to have a nearly bubble-free adhesion.



5. Take another metal ring, repeat steps 1 to 3.
6. Carefully align and gently place this second metal ring with the first metal ring (the one with the wafer adhered), on top of the front side of the wafer



7. Press gently with your hand to get as many bubbles away as possible. It is recommended to use a hand only because we might damage the patterns on the front side if using the presser.
8. Gently peel the tape from the second metal ring, leaving the tape adhered to the front of the wafer. Once the tape is free from the ring's edge, you can remove the ring itself.



9. Then, use the presser to adhere the top dicing tape to the only metal ring left. All set! Your sample is now ready to be loaded into the dicing tool.

Disclaimer: *The top layer of tape may pull off some of the dicing resist. If your sample's top layer is fragile or has poor adhesion, it could be damaged when the front-side tape is removed. In our case, the top layer is a patterned and etched polysilicon that adheres well to the silicon substrate, so front-side taping does not cause damage.*

<u>Tip 3: Test cut on a dummy wafer for hairline and cut position alignment</u>

It is always recommended to use your own dicing blade, as the condition of the shared default blade in the lab may vary. Each time a blade is replaced, a calibration must be performed due to differences in blade depth, width, and exposure.

There are a few notes and tips:

- To avoid damaging your patterned wafer, perform test cuts on a dummy wafer for blade calibration.
- You only need to perform the θ-alignment for Channel 1. Channel 2 is automatically set perpendicular to Channel 1, so do not override the θ-alignment for Channel 2.
- During alignment, press "Align θ" twice. When the message "... press ENTER …" appears, move the dotted alignment line to your intended cut position before pressing

ENTER. The tool assumes the position of the line at that moment is the target cut position.

- After the test cut, perform a quick sanity check. In "Manual align," make another parallel cut and use the index shifting function to see if the second cut aligns with the dotted line.

Tip 4: Alignment with double-sided taping with proper cut position setting

Once the test cut is complete, replace the dummy wafer with your double-sided taped wafer. When aligning, keep two key points in mind:

1. Increase Brightness: The dicing tape absorbs light, making it difficult to see the patterns on your wafer. Increase the microscope's brightness to make them visible.
2. Use Manual Focus: The thickness of the top dicing tape can confuse the autofocus feature, causing it to focus on the tape rather than the wafer surface. You must manually adjust the focus up and down until the patterns on your sample are sharp and clear.