Developing Planarization Technique for SiN_x Metasurfaces Encapsulated in SiO_2

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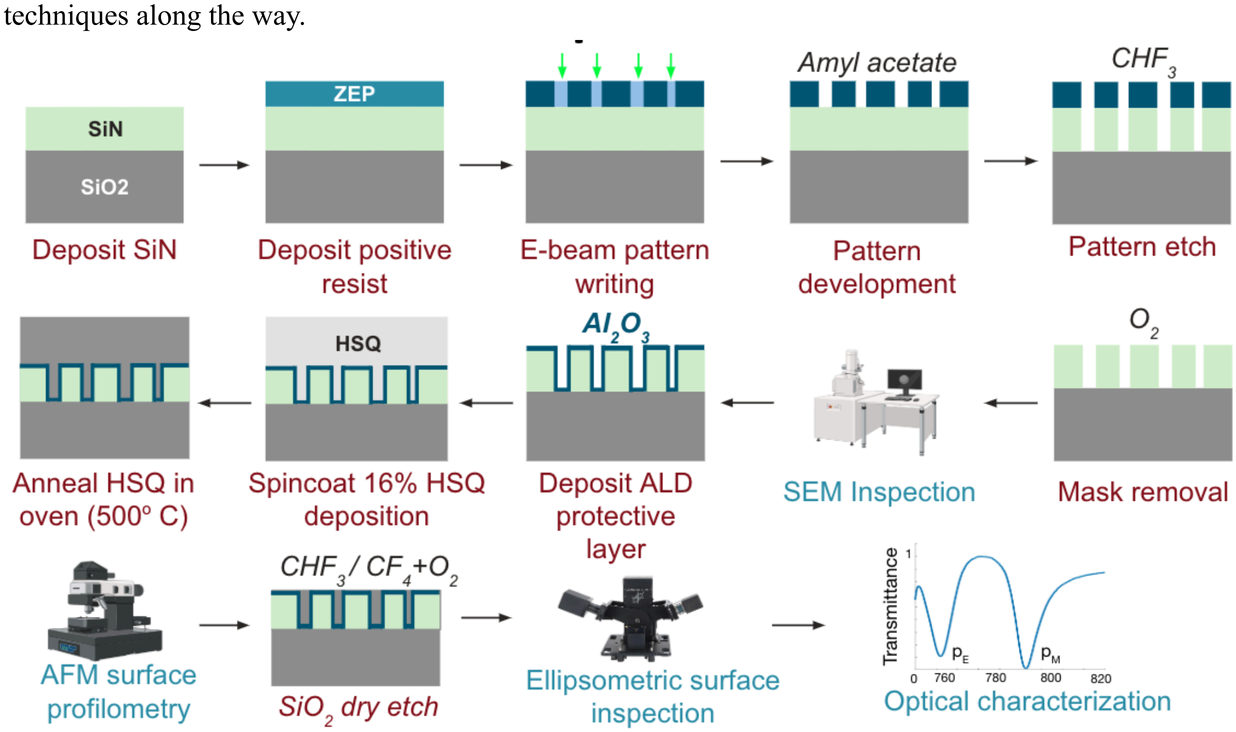
1. Introduction

1.1 Motivation

Metasurfaces supporting high quality factor (high-Q) resonances have emerged as a powerful platform for enhanced light matter interactions that are often used in biosensing, nonlinear optics, and label free molecular and cell imaging. These metasurfaces consist of sub-wavelength resonant structures, usually blocks or disks, which confine the electric field within the nanostructures. However, this confinement of the electric field deep in the structures limits interaction with external analytes such as biomolecules, tissue samples, or 2D materials due to the weak field intensity on the surface.

To address this limitation, we propose employing planarization of the metasurface using a material with a higher refractive index than air, specifically SiO_2, to push the electric field distribution closer to the top surface of the metasurface. This increases the field accessibility enabling a stronger interaction with materials that are interfaced on the surface. We intend to leverage this approach to enhance a spectra signal from Raman spectroscopy, a vibration spectroscopic technique that provides molecular specific information based on the inelastic scattering of light from a sample. We then plan to use it to phenotype distinct cell populations within a tissue sample such as tonsils and tumor immune microenvironments, to better understand their spatial arrangement. Given that Raman is a rare phenomena occurring 1 in 10^6 to 10^8 photons, enhancing the local electromagnetic field at the sample interface is essential for improving signal strength and sensitivity.

Early attempts to do planarization from our lab resulted in a swiss cheese in which the SiN_x metasurface was quickly etched away when trying to land on the planar surface. We started this project with the aim of understanding and developing a solution to that problem and learned many fabrication tools and techniques along the way.



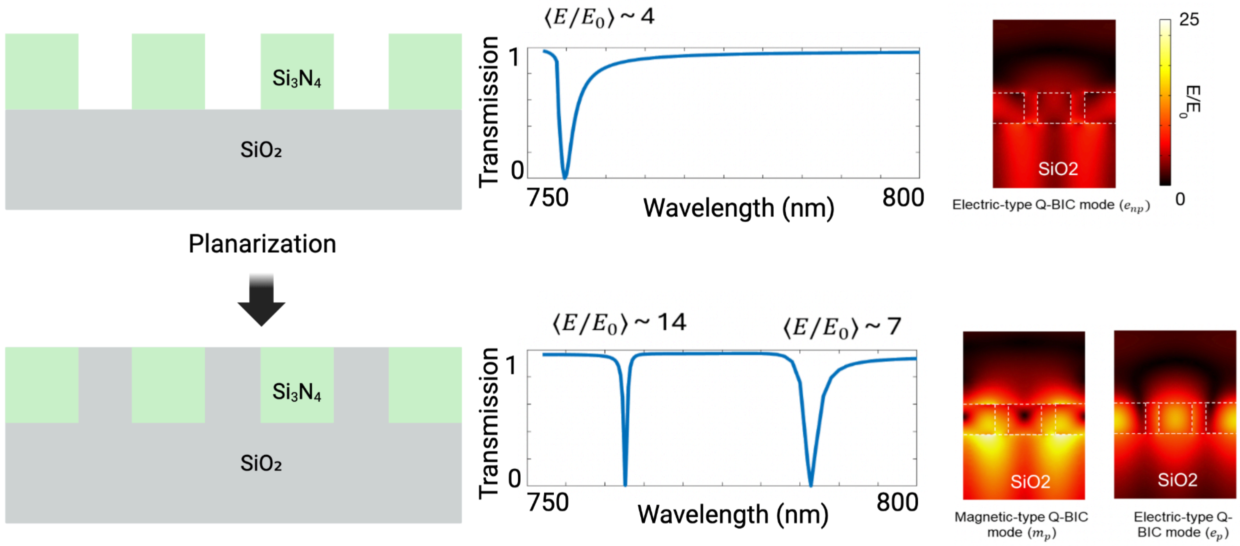


Figure 1: Overview of process explored, a schematic representation of the effect of metasurface planarization on optical mode structure in fully dielectric metasurfaces

In this paper, we present the development of a planarization process that is optimized for SiN_x based metasurfaces that are encapsulated in SiO_2. Hydrogen silsesquioxane (HSQ) is used as a substitute for SiO_2 to spin coat the metasurface and anneal it at high temperature to transition to SiO_2 like material. Our goal is to establish a reliable process for achieving a conformal and planar oxide layer on metasurface devices which reduce scattering losses and improve detection sensitivity for Raman based sensing and nonlinear optical effects, which are key focus areas in our research group.

1.2 Planarization requirement

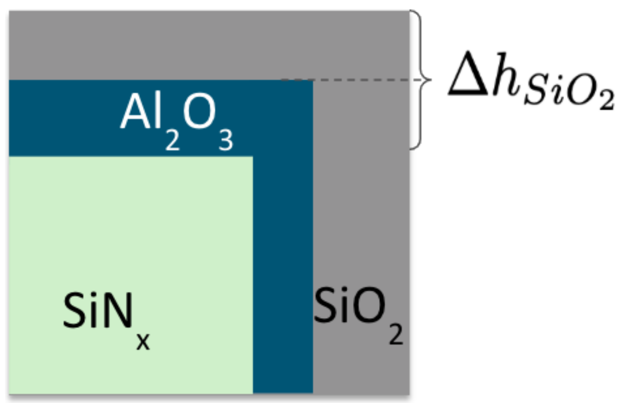
In order to achieve the above goal, we primarily focused on the following processes that are discussed further in depth in section two of this report:

1. Etch selectivity → investigating the etch selectivity of HSQ relative to Si_3N_4 to enable a precise control over planarization so that the underlying nitride nanostructures are not compromised.
2. Optical properties of planarization material (HSQ) → characterizing the chemical composition and the refractive index of annealed HSQ in comparison to glass or SiO_2.
3. Mechanical and surface characteristics → evaluate surface roughness / smoothness as a key metrics affecting the scattering losses.
4. Fabrication reproducibility → Assessing the consistency of the fabrication process across multiple fabrication runs for different designs.

2. Process Development

2.1 Etch selectivity

As part of our goal to land close to the top surface of the metasurface we needed to understand the process window we had available. To do this we needed to know what the different etch rates were of the materials involved in our process. This included baked HSQ, SiO_2, SiN, and Al_2O_3, which are the materials we used for planarization, as the substrate, as the photonic block material, and protective layer respectively. The problem is shown below in which we wanted to land on the tops of the blocks and the process window is dictated by the ability for the Al_2O_3 to protect the SiN from being over etched.



$$\Delta h_{SiO_2} * \frac{EtchRate_{Al_2O_3}}{EtchRate_{SiO_2}} = \Delta h_{Al_2O_3}$$

Figure 2.1 Schematic of the protective alumina layer with the equation that dictates the amount of Al_2O_3 required to protect the SiN_x device

In order to get the optimal etch selectivity we aimed to test a variety of parameters on the **Oxford-RIE** instrument so that we could hone in on an etch recipe that gave it the best selectivity. This included optimizing over the Power, Gas Ratios and Gas Pressure. We started with a base recipe in our lab that used CHF_3 and O_2 in a 40:2 gas ratio at 100 power and 25 mTorr pressure. Then tried an initial test to get a feel for the parameters of Power and Gas Pressure to see how they impacted etch selectivity.

Tip:

Avoid measuring the chip soon after cleaning as residual acetone and IPA can be left over, if you'd like to measure your chip immediately after the etch it is recommended to use a swab to clean the sandovac oil off of the back of the chip.

Preparation of Samples:

Tools: wbflexxcorr, CCPDEP, Spinning and Baking of HSQ, Savannah, Oxford-RIE

1. Wbflexxcorr - Clean a Silicon wafer by doing a 30 minute Piranha clean
    a. Use the 2-inch wafer holder to clean 4 separate pieces
    b. Put in Piranha for 30 minutes
    c. Wash in water bath
    d. Dry each piece
2. CCPDEP for SiO_2 and SiN_x

    a. Clean Chamber, It's free so clean as long as necessary
    b. Season the chamber, 5 minutes
    c. Deposit roughly 300 nm based on previous deposition rates (Default SiN and SiO_2 recipe)
        i. Put piece on a dummy wafer that looks clean
    d. Clean chamber
3. Savannah
    a. Check the precursors
    b. Adjust rate and deposit ~ 20-50 nm of Alumina
        i. The Alumina is not going to etch much so not much is required
4. Baking of HSQ (See below for more details)
    a. Snap pieces of Si into small 1cm squares by hand
        i. Make a small cut on the edge of the Silicon using a Diamond Scribe
        ii. Hold the wafer on the edge at that point with pointed tweezers and push down to snap
    b. Spincoat HSQ at 5000 RPM with a 3000 RPM/s ramp for 1 minute
        i. Bake on plate in SNSF for 5 minutes at 180C
        ii. Follow baking recipe recipe found in further sections

Etching of Samples:

1. Clean Oxford-RIE (SF6 Clean)
    a. Bring a clean wafer if you have one for your lab
2. Snap any test 1cmx1cm pieces required for your etch test
3. Season another wafer with the recipe of interest
    a. Run the etch recipe for 1 minute to season the chamber
4. Run Etch recipe
    a. Draw with Sharpie halfway across the chip to create an edge for verifying etch height later
    b. Take wafer that was seasoned and place 4 drops of Santovac Oil near the center
    c. Place each of Four chips on the Santovac oil
    d. Run the etch
5. Clean of the Si wafer with IPA and Acetone and repeat until completed with etch recipe testing

Final Plots:

2.1.1 Etch selectivity RF power and pressure optimization

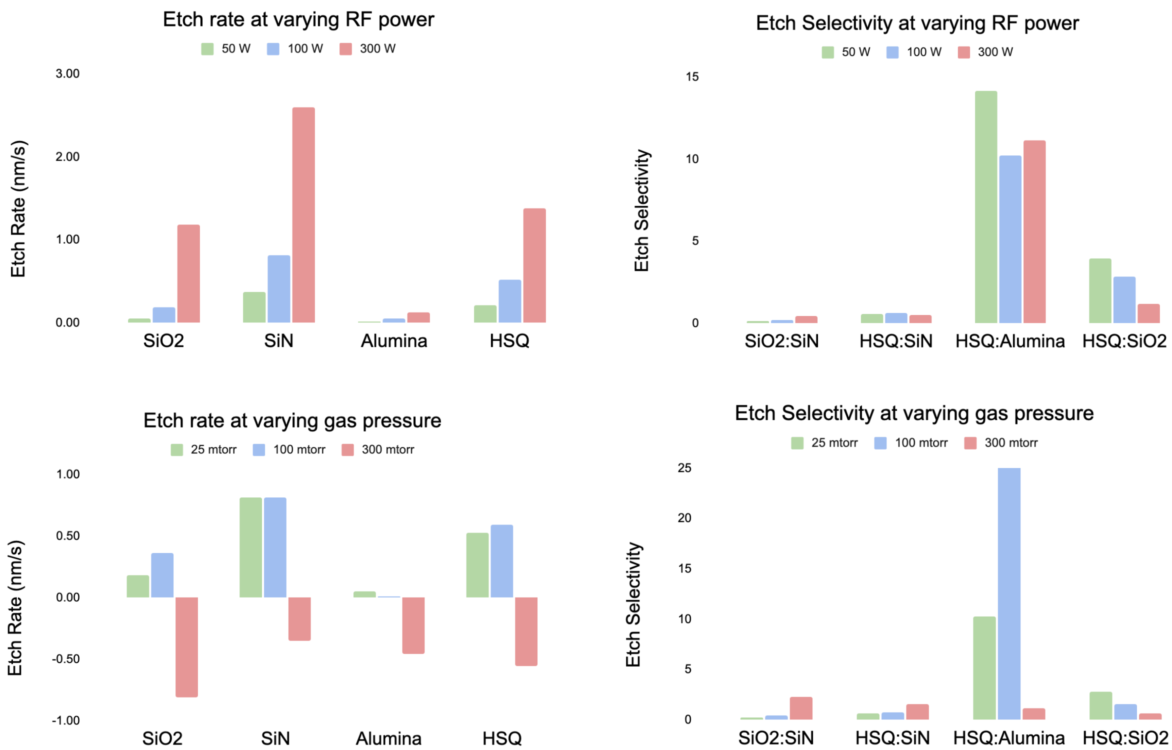


Figure 2.2 Etch Rate and selectivity data after a test sweep. Note that the HSQ:Alumina value in the fourth plot is much higher but it was likely due to a measurement error in the ellipsometry as it was not able to be repeated in future validation tests.

From this initial measurement, we decided to increase the gas pressure as it clearly decreased the amount of etching that we would expect to occur. This aligned with our expectations as we expected that at higher pressure a polymer layer may form to protect the Alumina which we see in its extreme case at the 300 mTorr pressure where the polymer buildup outpaces the ability for oxygen to remove it from the surface. This was something that we will see in future experimental data consistently. We also decided to explore increasing the gas pressure but with additional Oxygen sweep as we saw a positive correlation between the selectivity and increased gas pressure. We also decided to try to verify some of our measurements of ellipsometry by using Sharpie to create a step.

2.1.2 Etch selectivity gas ratio optimization

Following our exploration of the effects of gas pressure and RF power on both the etch rate and selectivity for the various substrates we used, we looked into the effects of gas ratio on the etch rate and selectivity. We did this by varying the ratio of O_2 from 0 to 10 by increments of 5, while keeping the CHF_3 to remain constant. By this we changed the volume of O_2 that's released into the chamber. As shown in Figure 2.3, there is a positive correlation between etch selectivity and gas ratio. We understand this to be a result of oxygen reacting with post-etch polymers on the surface of the substrate and providing a new surface for the fluoride ions to react and etch further. As shown on the left of Figure 2.3, the etch selectivity at 100 mTorr for HSQ:Al_2O_3 (substrates of interest), is maximized at 40:10 gas ratio of CHF_3 to O_2. We replicated this experiment for an increased pressure; 300 mTorr while maintaining all the other parameters similar, and found that etch selectivity is higher in 40:05 gas ratio than 40:10 implying the impact of pressure to be greater than that of gas ratio. We then did two control experiment sets at 0 oxygen volume in the chamber while keeping the same amount of CHF_3 (40:0 gas ratio), and saw that the thickness of the films increased post etching as shown on the left of Figure 2.4. We reason this to be a result of the build up of polymers on the substrate surface during the etch process due to lack of oxygen to react with. Based on these results and those demonstrated in Figure 2.2, we found optimal pressure to be 100 mTorr, and as a result we chose the gas ratio of 4:10 at 100 W and 100 mTorr to be our final etch recipe to use for our planarization project.

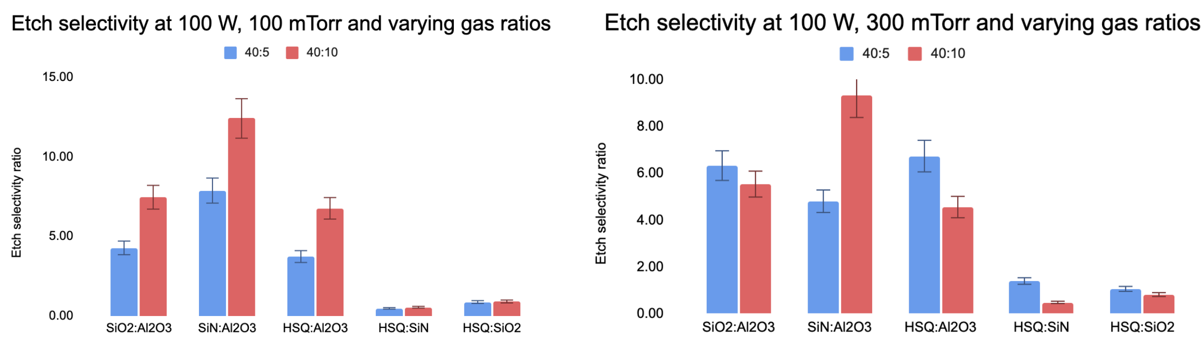


Figure 2.3: Etch selectivity data acquired at varying etch gas ratios of CHF_3 to O_2 (40:5 and 40:10) at 100 W, and two different plasma pressures; 100 mTorr (left) and 300 mTorr (left).

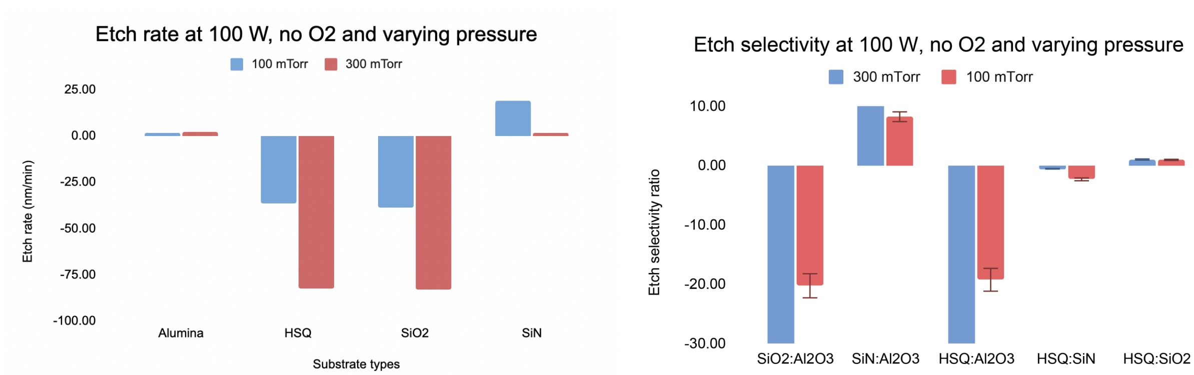


Figure 2.4: Etch rate (left) and selectivity (right) data acquired at 100 W, and varying gas pressures with no O_2 in the chamber.

2.2 Mechanical Measurement Verification

One concern we began to have was that we wanted to make sure we were etching the correct height during the above etch testing process so we used sharpie to create steps in our test chips seen below in order to see whether or not the step height would be enough. After putting these step height measurements in we were able to validate the heights using AFM but not without having quite the struggle with profilometer first. This was a good learning experience to see how a profilometer measurement that looks like the one below could have an AFM measurement that was completely smooth due to the noise in the profilometer. This was pretty important because at times we were worried about the surface smoothness of the HSQ after it had baked out.

2.3 HSQ annealing and characterization

Sample/material: HSQ on Si chips (~1cm by 1cm)

1. Initial wafer clean (SNSF Solvent Bench):
    a. Clean wafer using Acetone and then rinse with IPA
    b. Blow dry with N_2 gun on both sides
2. Dehydration (SNSF hot plate):
    a. Place wafer at 180ºC hot plate for 2 minutes
3. Spin coat HSQ (SNSF Cee Apogee Spinner):
    a. Suggested to filter with 0.1um Filters and a syringe for improved quality
    b. Add 4-5 bubbles of HSQ FOX 16 on wafer using a plastic pipette
    c. Spin coat HSQ at 5000 RPM with a 3000 RPM/s ramp for 1 minute
4. Soft bake (SNSF Hot Plate):
    a. Bake at 180ºC for 5 minutes
5. Prolonged Annealing Bake (Lab Oven):
    a. Ramp oven from 25ºC to 500ºC over 3 hours
    b. Hold at 500ºC for 6 hours
    c. Ramp down to 25ºC over 3 hours

Once we identified the optimal working parameters for the etch process, we focused on the preparation and characterization of HSQ; the planarization substrate for our metasurface. We spin coated and annealed a silicon chip with HSQ using the recipe described above. Prior to baking, we measured the thickness of the HSQ coat using an ellipsometer in order to determine the rate of shrinkage during the bake step as a result of polymer crosslinking. We found the change in highest to be about 20% across all samples. In addition, we acquired Raman measurements of HSQ chip post annealing and compared it to that of SiO_2 in order to verify that the chemical compositions of the two substrates are identical as shown on Figure 2.6 (right). Finally we acquired ellipsometry scans of baked HSQ and fitted it using a fit model that is built for SiO_2 (Figure 2.7) and found that the model was as suitable for HSQ as it is for SiO_2 further confirming the optical similarities between these two materials.

Figure 2.5: Oven temperature ramp cycle for slow heating HSQ post spin coating (left) and placement of chips in mini-oven for the 16 hours bake (right)

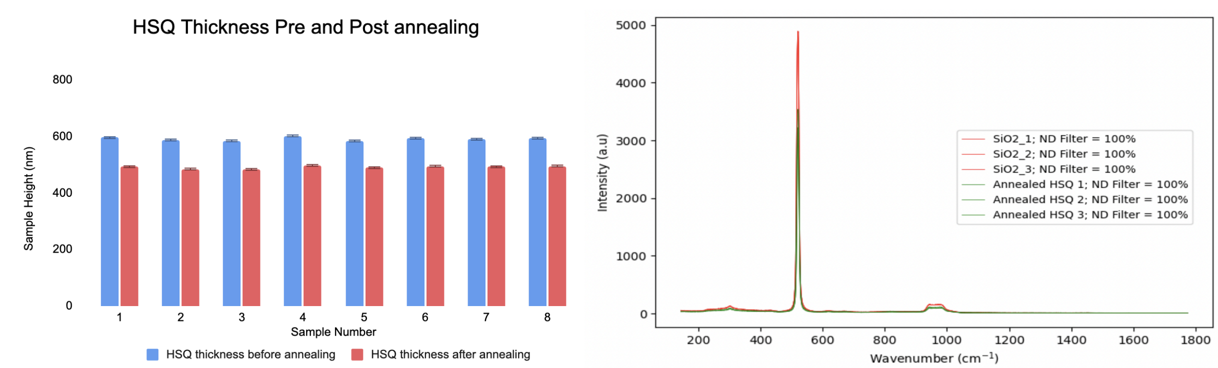


Figure 2.6: Change in HSQ thickness due to annealing (left) and Raman measurements of annealed HSQ chips and SiO_2 chips to verify the chemical and structural resemblance between the two

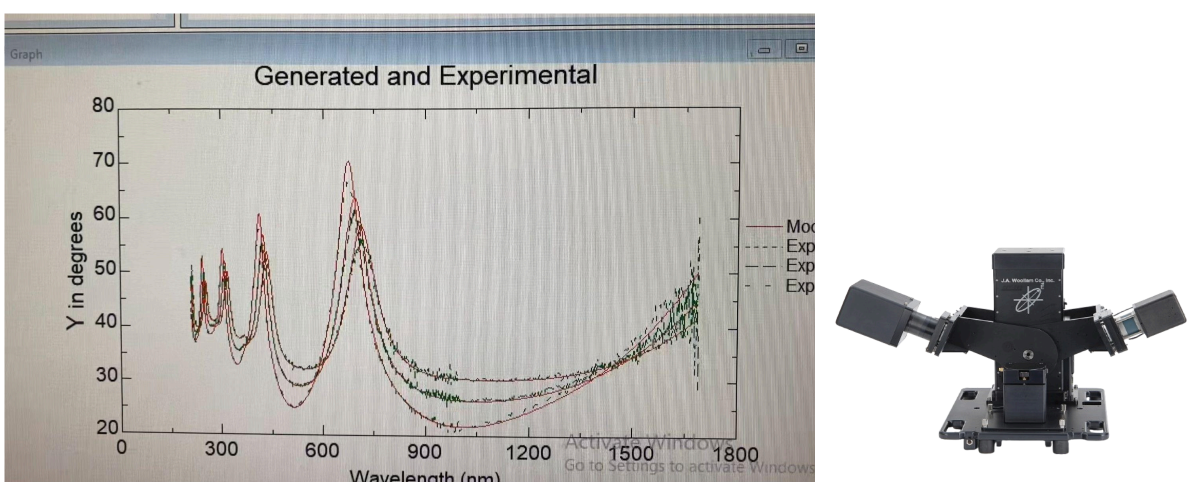


Figure 2.7: Ellipsometry measurement of annealed HSQ fitted to SiO_2 model

2.3 Device fabrication

2.3.1 Device Fabrication and Characterization Overview

As part of understanding the performance of our fabrication process we spent time trying to look at the device at various points during planarization in order to determine the quality of the surfaces at different points in the process. This included a variety of testing at various points. We ended up completing three metasurfaces with varying degrees of success. Challenges and tips are highlighted at various stages in the report.

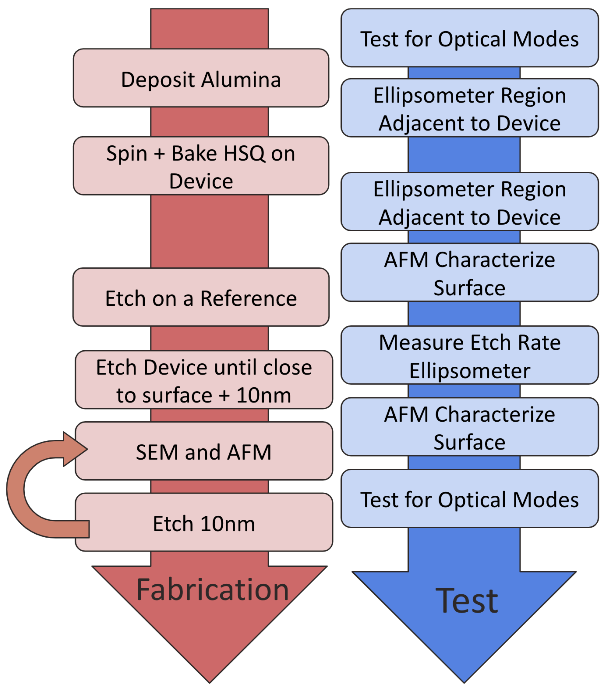
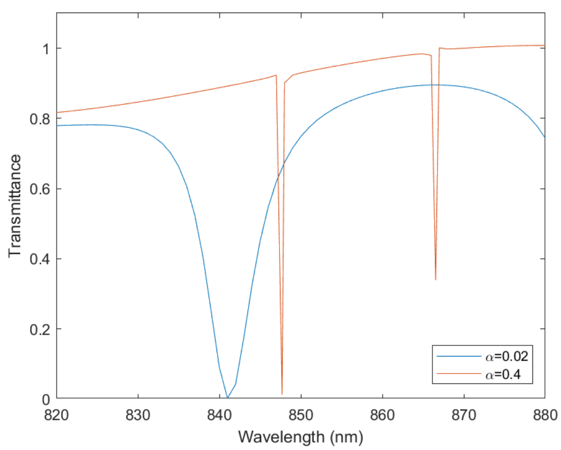


Figure 2.8 Fabrication and characterization cycle for development of process

2.3.2 Chip#1: Verification that Al_2O_3 Minimally Effects Optical Mode



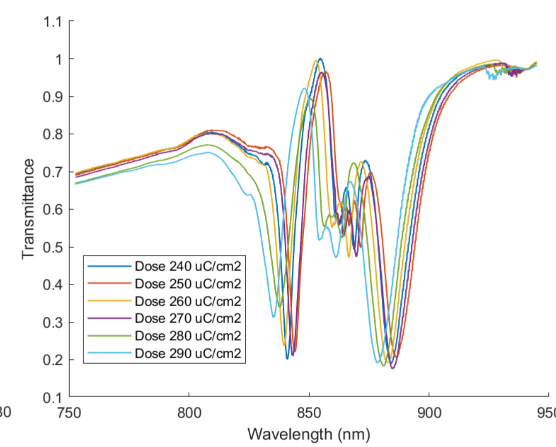


Figure 2.9: Simulation transmittance plot of metasurface before alumina deposition (left) and experimental transmittance of metasurface after alumina deposition at different dose sweeps (right) showing minimal effect of alumina on optical mode.

2.3.3 Initial HSQ Bake

We wanted to check the flatness after the completed bakes and also anticipated that we would see sagging near the edges of where the pads were as the HSQ would need to sink into the holes and lead to a net sinking across the area. In order to test these two phenomena we used AFM to characterize the edges of the chips in the sagging regions.

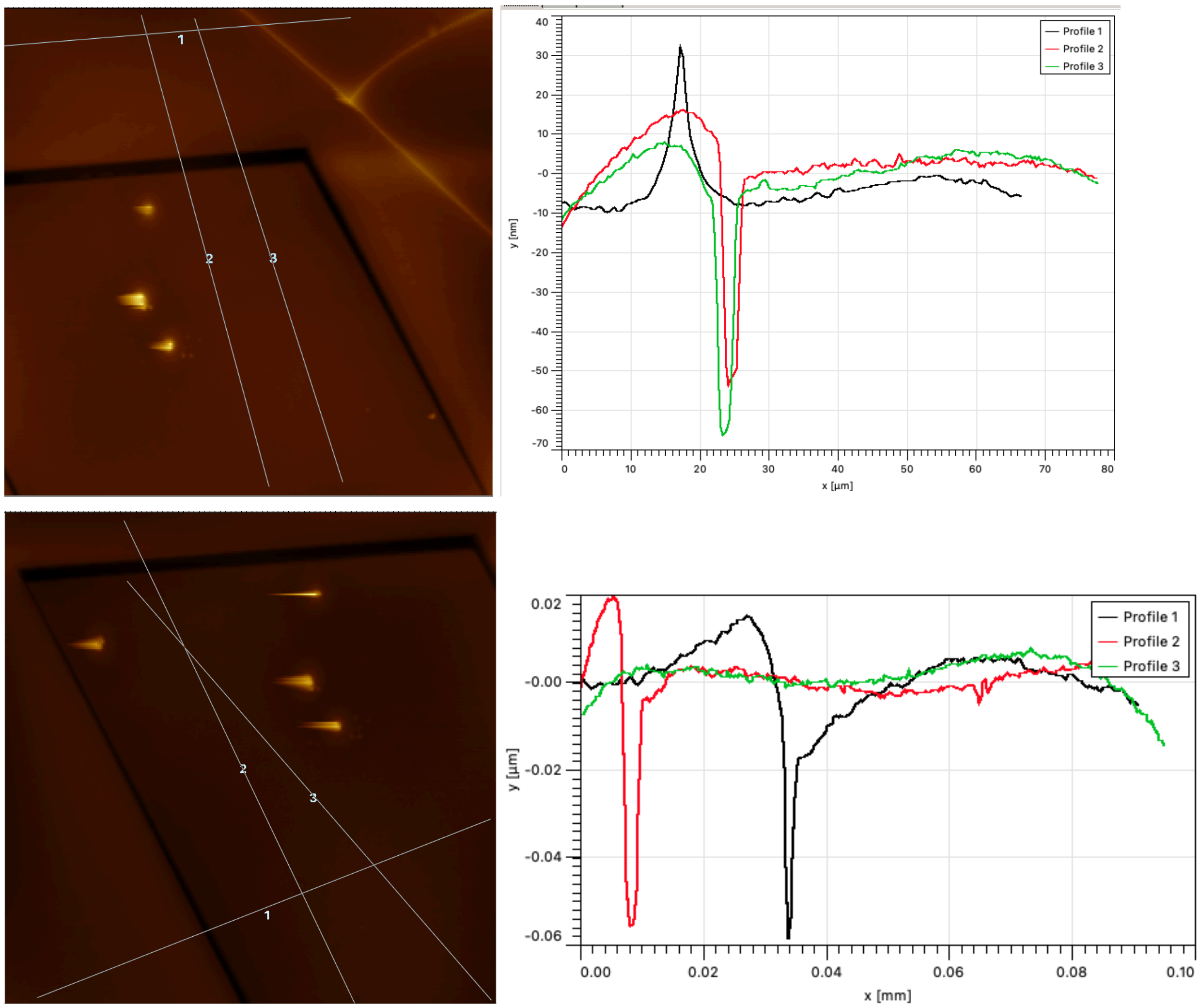


Figure 2.9:

In these images we found that there appeared to be a bump/dip that would form at the edges of the metasurface but the difference in height between the two surfaces was relatively small overall. As a result we assumed that the heights would be within ~5 nm of each other which was within our process window. After verifying the surface we began to do testing of the metasurfaces after trying to planarize to the surface.

2.3.4 Etch to the Surface

Chip #1 Severe Underetch: We etched a large amount of glass remaining and saw the modes we thought to expect as if we landed on the surface. However after checking the amount etched there was still a considerable amount of HSQ on the surface.

Second Etch Chip #1: During our second etch attempt, we still had the assumption from the first etch that we landed on the metasurface exactly. Operating under that assumption, we applied etch gas to etch 20nm. However, instead of achieving the desired etch, we saw a significant deposition of small particles on top of the metasurface. This was due to an error in the gases which showed us what could happen as a result of not having changed the oxygen level. This was found to be removable by using a 50% oxygen etch, at 100W and 25mtorr for 20 seconds on the Oxford-RIE.

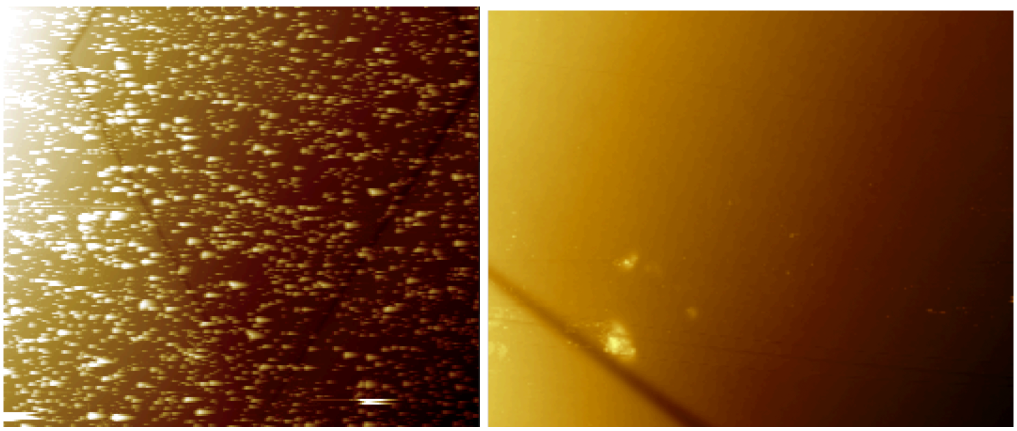


Figure 2.10: AFM photo of metasurface after second etch attempt with significant particle deposition on the surface

Chip #2 Etched to the Surface: We also etched to the surface on chip 2 and saw severe cracking along the surface in what looked like the pattern of an old fashioned donut. This suggested that the HSQ method that we had been pushing towards had severe inherent challenges. That went deeper than just cracking on the surface discussed below. This was likely due to the stress created from the HSQ shrinking by nearly 20% that was trapped beneath the surface.

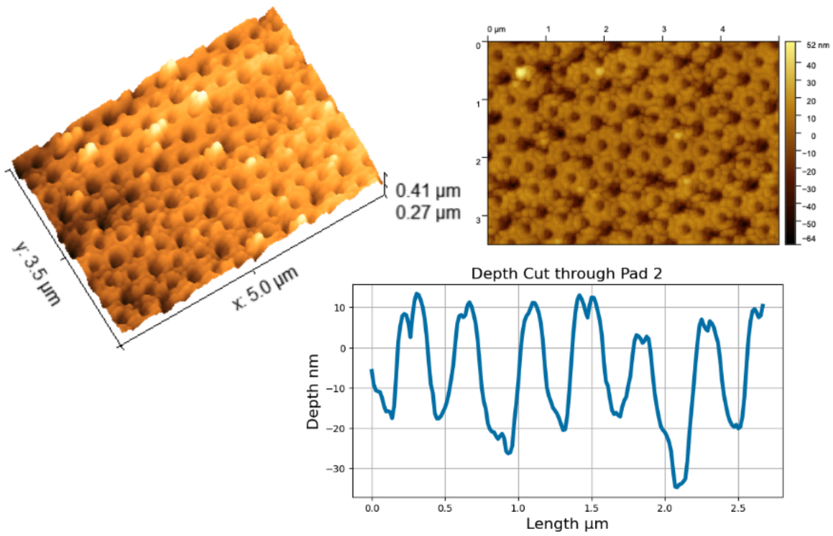


Figure 2.11 The above AFM measurements are of the top surface after the final etch on chip 2 which show a considerable amount of cracking that suggests tension across the top surface

2.3.5 Chip#1: Effects of planarization on Optical Mode

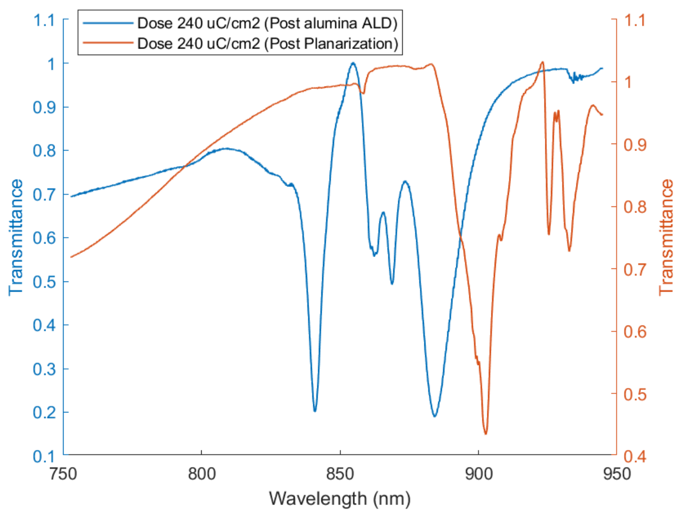


Figure 2.12: Resonant mode redshifts by about 60 nm after metasurface planarization with HSQ

3. Project Challenges

3.1 HSQ Cracking

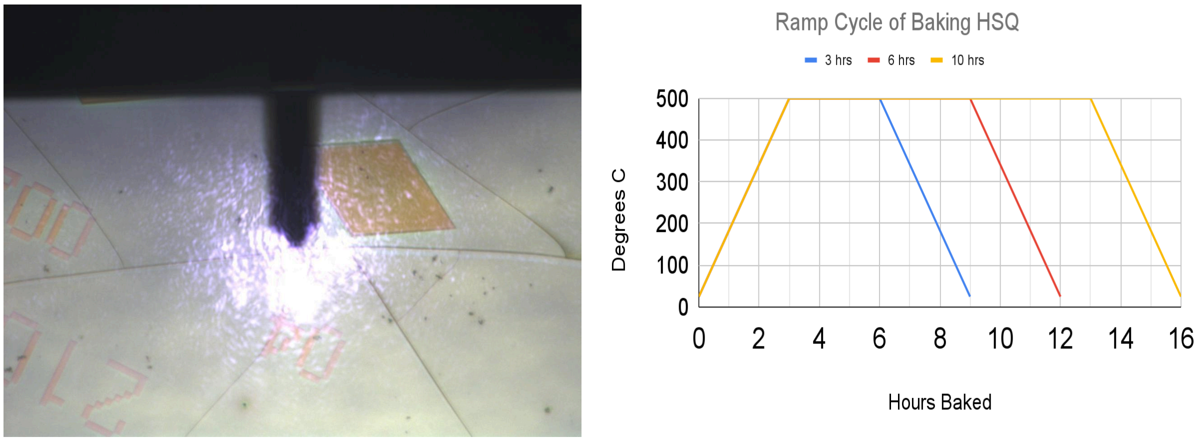


Figure 3.1: Crack shown on the HSQ layer of the metasurface (left) and oven ramp cycles for 3, 6, and 10 hours bake tests (right)

One of the major challenges we had in our fabrication process is the cracking of the HSQ layer on the metasurface as shown on Figure 3.1. Although it does not appear to affect the optical properties of the chips, we wanted to ensure that it is not a consistent problem moving forward. In order to resolve this we first looked at the effect of HSQ bake hours to see if the prolonged bake at 500ºC is causing densification of the material due to crosslinking and inducing stress on the film layer. We alternated the bake hours from the previous 10 hours to 6 and 3 hours. Despite these changes, we saw the cracking to be a consistent issue as demonstrated in Figure 3.2

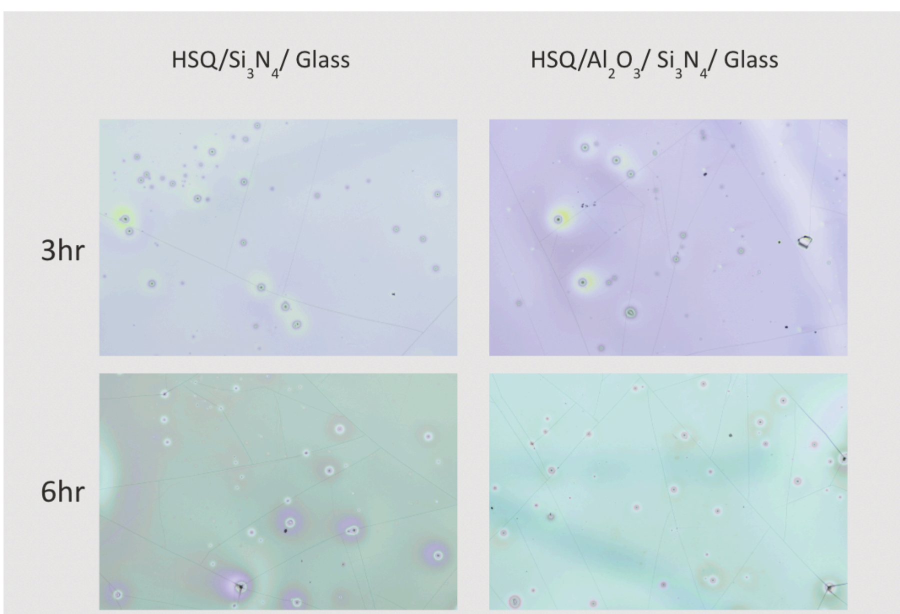


Figure 3.2: HSQ crack test at varying bake times (3 and 6 hours), and substrate compositions.

We did not observe HSQ cracking during the initial HSQ bake tests that were done on Si wafers. Since the major changes here are the base substrate being SiO_2 and the addition of Alumina and Silicon Nitride film layers, we conducted the crack test experiments in chips that resembled those film depositions on SiO_2. However we still found the cracks to continue to occur despite the different film compositions and bake hours as shown above.

3.2 Proposed Solution

To address the consistent HSQ cracking issue, moving forward, we plan on exploring the following approaches:

1. **Compression testing of SiN :** we plan on conducting mechanical stress and compression tests on Si_3N_4 layer on Si to determine if the compressive strain in the nitride film is contributing to the cracking of the HSQ layer during the thermal cycling. [1]
2. **Alternative Oxide deposition via HDPECVD:** we are also evaluating chemical vapor deposition of SiO_2 as an alternative to spin coating HSQ approach to mitigate the stress mismatch between different film layers and potentially improved adhesion to the nitride layer
3. **Modified bake ramps:** depending on the outcomes of option 1 and 2, we will explore developing a more controlled and lower temperature annealing process for HSQ to address the stress accumulation during HSQ densification at high temperature.

4. Discussion and Conclusion

In this project, we focused on developing a reproducible planarization process for SiN_x metasurfaces using spin-coated and annealed HSQ as a planarization material. The primary goal was to fill in the air gaps between nitride discs with a higher refractive index material, and create a planar top surface to push the optical modes to the surface, thereby increasing the interaction volume for applications such as Raman spectroscopy.

We optimized etch selectivity between HSQ and the underlying layers Al_2O_3 and Si_3N_4. Our investigation of different etch parameters (power, pressure, and gas ratio) showed that the gas ratio of CHF_3:O_2 and chamber pressure had a significant impact on the etch rates and selectivity of different substrates. A final etch condition of 100 W, 100 mTorr, and 40:10 gas ratio were chosen to be the most selective process to preserve the structural integrity of the protective layer (Al_2O_3) while also effectively removing the HSQ layer above the metasurface.

While Profilometer readings were not as reliable, AFM measurements confirmed the surface roughness to be within an acceptable range for our application.

Looking ahead we are excited to try the proposed solutions and continue to learn from our successes and failures during our first quarter in the clean room. We would like to thank our course instructors and classmates, Dionne lab members, as well as our wonderful mentors Lavendra and Michelle for all of their guidance and support throughout the project.

5. References

1. Mackenzie, K., Johnson, D., DeVre, M., Westerman, R. & Reelfs, B. Stress Control of Si-based PECVD Dielectrics. *Meet. Abstr.* **MA2005-01**, 406–406 (2006).