Superconducting Josephson Junctions in KJL2

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1 Introduction

1.1 Applications of Josephson Junctions

A Josephson Junction is a nanoscale device consisting of two layers of superconducting film (typically Al), separated by an insulating barrier. These devices are mesoscopic quantum systems, with applications such as quantum computing [2], highly-sensitive sensors [3], and simulating many-body systems [4]. As a result, they are fabricated by many groups across Stanford and SLAC. However, up until now, SNF and SNSF did not have a tool that was capable of making these devices to perform well. As a result of this project, we provide a recipe for making aluminum-aluminum oxide-aluminum junctions using the new KJL2 tool in SNSF.

1.2 Fabricating Josephson Junctions

There are various methods of fabricating Josephson Junctions. The two most common designs are Manhattan and Dolan style junctions. Manhattan junctions are formed by exposing two perpendicular rectangular arms. The two arms intersect with some known overlap area. With angled evaporations, one can selectively deposit in either of the two arms. To form an aluminum tunnel junction, a deposition is made in the first arm, then the aluminum is allowed to oxidize. Once an Al_2O_3 layer is formed of the desired thickness, an aluminum deposition is made in the second arm.

The Dolan junction process utilizies dual-layer resist features. Using Electron Beam Lithography (EBL), a photoresist bridge is formed. Using a double-angle evaporator, an aluminum deposition is made underneath the bridge. The sample is then exposed to oxygen, and allowed to form an Al_2O_3 layer of desired thickness. Then, the sample is rotated 180 degrees, and a second angled evaporation is made from the other side of the bridge. This layer crosses the first deposition layer, forming a small region of overlap. The area of this overlap depends on the angle of evaporation and the bridge's length, width, and height. Following this second deposition, the sample is removed from the evaporator and the resist is lifted off, leaving behind the junction feature. A diagram of this process is shown in Fig.10 for our fabrication process.

Each junction method has its own advantages. Since the Manhattan lithography step only involves patterning rectangular features, the design is fairly straightforward and less sensitive to dose and focus parameters. For some applications, it is possible to pattern Manhattan junctions using optical lithography. Although they are less sensitive to lithography parameters, the junctions are highly sensitive to deposition angles. If alignment or tool angle is askew, the junctions can become either open or shorted.

Dolan junctions are more difficult to pattern in EBL, and require care during the development stage to avoid rupturing the delicate bridge structures. However, once the bridges are made, the process is less sensitive to variations in deposition angle. Slight variations in this parameter can affect the area of deposition overlap (therefore changing the room temperature resistance and circuit energy of the feature), however, the junction will still be functional. Furthermore, feature size of the Dolan junction can be smaller, as the arms are parallel to one anther rather than perpendicular; the path from the Dolan junction to the rest of the circuit is reduced. Smaller junction features are optimal, as it reduces the chance of material defects that can degrade device performance, and reduces quasiparticle pathlength in detector applications.

1.3 Junctions in the KJL2

The primary requirement for fabrication of these junctions is the use of a double-angle evaporator capable of superconducting film deposition. The evaporator must also be capable of oxidation. The KJL2 is a new tool dedicated to superconductor fabrication, and is ideally suited for junction deposition. It is the only tool in the fab facilities capable of angled evaporation and oxidation.

Additionally, test depositions in the KJL2 demonstrated its ability to pump down to pressures on the order of 10e-7 Torr, and deposit films at rates as high as 1 nm/s.

2 Josephson Junctions

2.1 Mask Design

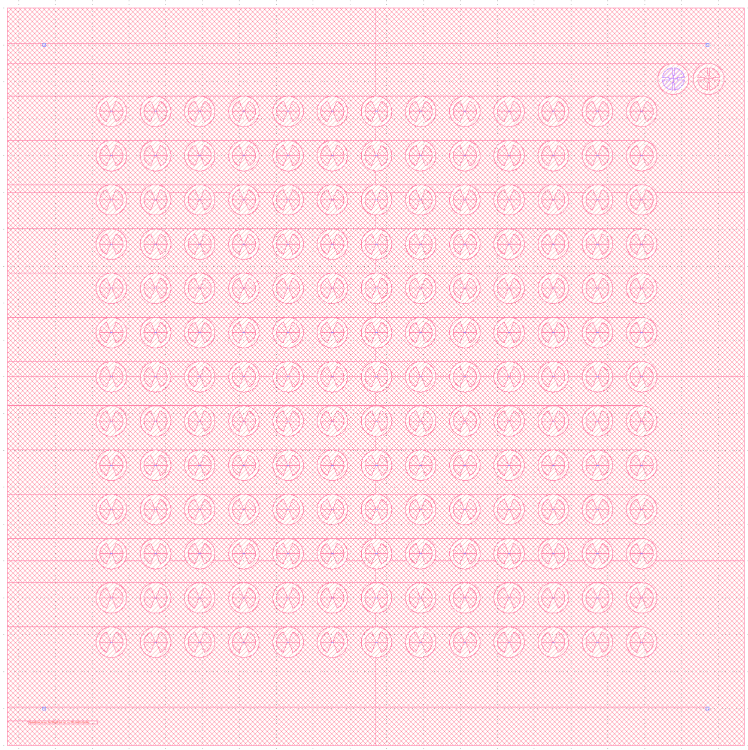


Figure 1: A mask containing an array of Dolan junctions with varying design parameters.

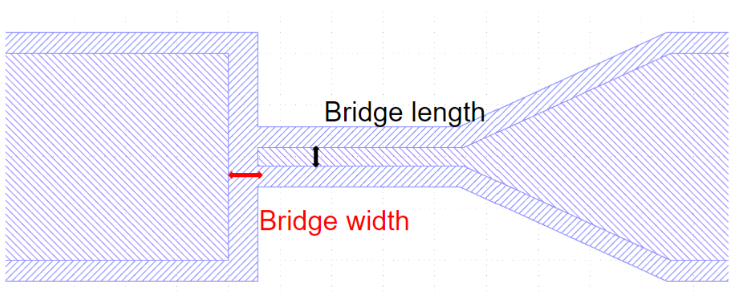


Figure 2: An EBL mask to generate a Dolan josephson junction. Design parameters relevant to the Dolan bridge are called out with arrows. The outer purple layer is used to create an undercut, exposing only the bottom MMA layer. The inner light purple layer is used to create a full cut through both the under MMA and upper PMMA layers..

To calibrate junctions resistances as a function of overlap area, we designed the mask shown in Fig.1. This mask contains a 2D array of junctions with various design parameters, as defined in image Fig.2. In this diagram, the inner, light purple feature is assigned a high dose capable of exposing both the upper PMMA layer and the bottom MMA layer. The outer, dark purple feature

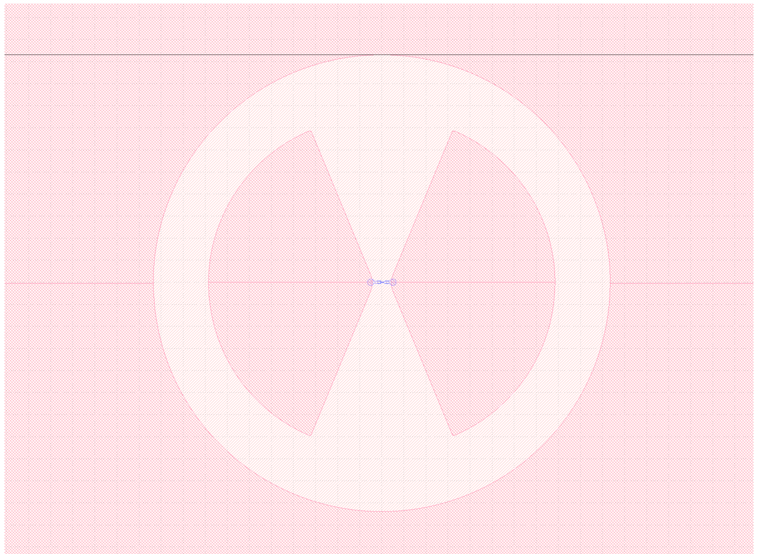


Figure 3: Each pixel of the calibration mask includes a Dolan josephson junction coupled to large probe pads

is assigned 0.25 times the standard dose so that only the undercut MMA layer is exposed. This forms a bridge-like structure in the center of the feature. Along the x-axis of the Dolan junction array, we sweep the junction bridge length from 0.12 µm to 0.36 µm in steps of 0.02 µm. Along the y-axis of the array, we sweep the junction bridge width from 0.12 µm to 0.36 µm in steps of 0.02 µm. By sweeping the size of the Dolan junction bridges, we are able to achieve various Dolan junction overlap areas. Since all junctions will have roughly the same oxide thickness, this variation in overlap area will cause the junctions to have varying resistances and inductive energies.

The junction features are quite small, with their largest dimension being approximately 20 µm in length. In order to measure the resistance of the junctions, we needed to connect them to structures large enough to serve as targets for micromanipular probes. We designed large fin structures of radius 112 µm to serve as a probe pads. A graphic of the total junction and probe feature is shown in Fig.3. We found this size to be sufficient to accommodate a single micromanipulator probe on each side of the junction feature. An image taken through the microscope of the SNF micromanipulator probe station is given in Fig.4. To ensure good electrical connection between the junctions and the probe pads, a connection circle with a 4 µm diameter is placed on the end of each EBL junction. The probe pad beneath this circle is then ion milled to remove ambient oxide growth. This process is described in more detail later in this report.

2.2 Single Deposition Junction Method

During the first round of fabrication, the probe pads were combined with the Josephson junctions in the mask so that they could be deposited in one single step (Fig.5). This temporary procedure was used to allow us to make junctions in parallel with developing an ion mill recipe. Without the recipe, we lacked the ability to make robust electrical connections between different deposition layers. However, we can circumvent this limitation by combining the junctions with probe pads in the mask, and patterning them with a single deposition. This is not a robust long-term method, as it creates an oxide layer in the middle of the probe pads. If part of a superconducting circuit, this oxide would inhibit quasiparticle transport to the junction, and could contain microscopic defects that hurt coherence lifetimes. Additionally, this forces the design to use the same material (Al) for

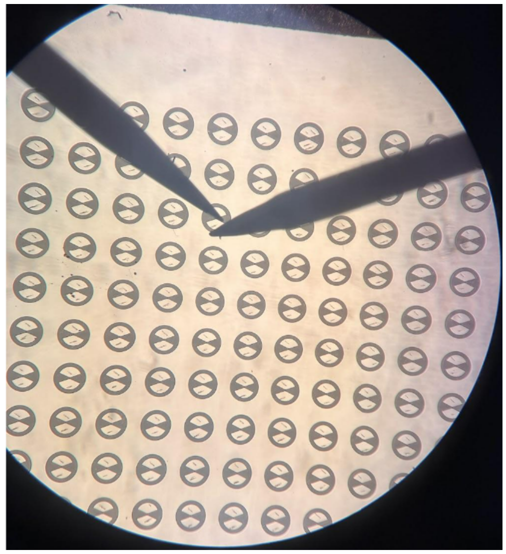


Figure 4: An image taken through the microscope of the SNF micromanipulator6000 shows an array of probed junctions. Small scratches in the surface of the Niobium probe pads are caused by contact with the probe tips.

both layers. Nevertheless, this method was useful in helping us write an initial recipe, and establish reliable functionality of the tool.

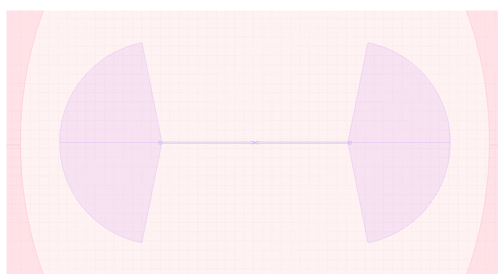


Figure 5: A mask modified for single-deposition junction development. In this mask, the probe pads are combined with the junction layer, and move 100 µm away from the junctions to mitigate EBL proximity effects.

In order to pattern the large probe pads using ebeam lithography, we ran several dose arrays to calibrate the correct exposure parameters. In the EBPG2 tool in SNSF, we determined that the optimal dose to expose both our MMA and PMMA layers together was 1450 µC/cm^2 for small, junction-scale features, and was approximately 980 µC/cm^2 for large probe pad features. The optimal dose for exposing just the MMA undercut was found to be 362.5 µC/cm^2. However, in calibrating this dose, we found that the optimization curve for the large probe pad features was quite narrow, and it was difficult to replicate results. Some of the dose arrays taken days apart indicated conflicting optimal parameters, and the optimal dose for the large features was found to vary as much as ±120 µC/cm^2. When the large probe pad dosage was incorrect, the junction dose was impacted, even though they were located over 100 µm away on the chip. An image of junctions impacted by underexposed probe pads is shown in Fig. 6. The darkened region surrounding the junctions indicates that there is remaining ebeam resist on the wafer in this region. Depositing on top of the resist remnants will likely lead to unintentional liftoff of the junction features. An image of junctions impacted by overexposed probe pads is shown in Fig. 7. When we examine the junctions more closely in this exposure (as shown in Fig. 8), we find that the bridges appear to be missing. Both the MMA and PMMA are exposed. If a deposition was run with this wafer, the junction pads would be found to be shorted to one another.

This type of error likely indicates that the Proximity Effect Correction (PEC) function that we are using in Beamer is slightly inaccurate. When used with small features, the function is sufficient, however, its inaccuracies compound for larger features, leading to a less robust process. Given this unreliability, we determined that this "shortcut" method was beginning to consume more time ad budget than desired, so we refocused our efforts on developing the standard junction process, involving two deposition layers.

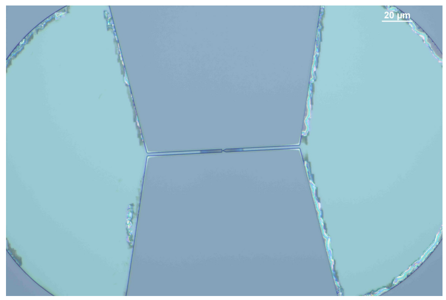


Figure 6: An optical image of underexposed ebeam resist features. The darkened region of the exposure indicates residual resist in an area that was intended to be fully exposed and developed away.

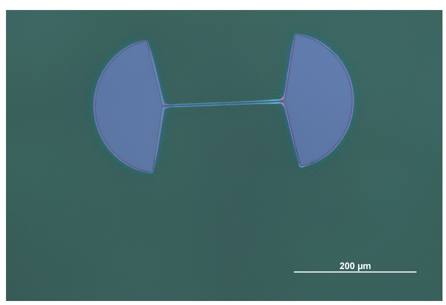


Figure 7: An optical image of overexposed ebeam resist features. The rainbow hue surrounding the feature indicates a sloped gradient to the resist. The height of the top layer of PMMA is being reduced in the vicinity of the overexposed feature.

2.3 Double Deposition Junction Method

Once we calibrated an ion mill recipe, as described later in the report, we adopted a 2-layer process for our junction calibration. An outline of our approach is given below and illustrated in Fig. 10. The full SOP for making these devices is included in appendix B. The outline for this process and our comments are included here.

1. Begin with a clean sapphire wafer.
2. Deposit a layer of Niobuum across the wafer.
3. Spin photoresist and optically expose a pattern with probe features.
4. Dry etch to remove Niobium in unwanted regions of the pattern.

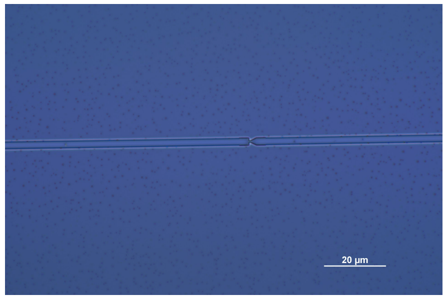


Figure 8: An optical image of the Dolan bridge in an overexposed ebeam resist feature. We note that the Dolan bridge is missing as a result of the overexposure.

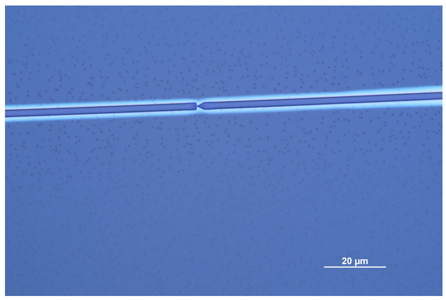


Figure 9: An optical image of a correctly exposed Dolan bridge. The hazy region in the center of the bridge indicates that it is in-tact and functional.

5. Spin ebeam resist and expose Dolan junction features.
6. Mount wafer in KJL2. Ion mill to remove oxide. Deposit first layer of Aluminum at an angle underneath the Dolan bridge.
7. Oxidize the wafer in KJL2.
8. Rotate the wafer 180 degrees and deposit the second layer of Aluminum at an angle underneath the Dolan bridge.
9. Remove wafer from KJL2 and liftoff excess Aluminum.
10. Probe room temperature resistance across the junctions.

2.4 Resistance Measurements

We use the micromanipuator 6000 at SNSF to measure the resistance of junction. To do this, one probe tip is placed on each side of the junction as shown in Fig. 4, and a simple IV measurement is made. The IV curve is measured for currents up to 1 µA, and if the junction is functional, the IV curve will appear linear. The slope of the IV curve gives the room temperature resistance of the junction.

For the recipe described above, we measured the resistances given in Fig. 11. The x and y axes refer to design parameters described previously in Fig. 2. We note that some of the junctions rendered shorted due to design parameters. This is visible by the dark (<1 kΩ) resistances in the table. SEM photos of typical junctions and shorted junctions are included in Figures 12 and 13 respectively.

Room temperature resistance is a useful parameter to measure because it can be mapped directly to the Josephson energy E_j of the circuit component. The critical current of a Josephson junction

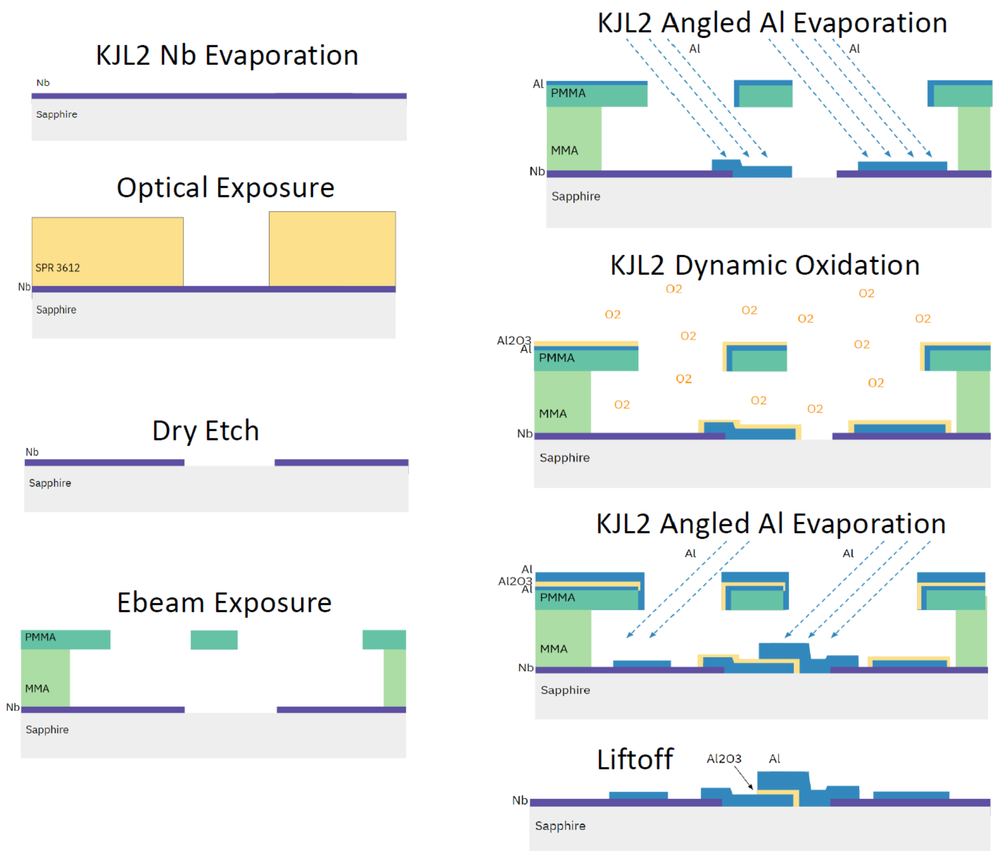


Figure 10: A block diagram illustrating the Josephson junction fabrication process.

is related to the junction resistance by the Ambegoakar-Baratoff (AB) relation [1]:

$$I_c = \frac{\pi\Delta}{2eR_n}\tanh\left(\frac{\Delta}{2k_bT}\right) \tag{1}$$

Where:

- I_c is the critical current of the junction at cryogenic temperatures
- R_n is the resistance measured at room temperature on the probe station
- Δ is the BCS superconducting gap of the material
- T_c is the critical temperature of the material. For aluminum, this number is 1.2 K.
- T is the cryogenic operation temperature of the junctions. In our dilution fridge facilities, we aim for temperatures between 8 and 30 mK.

We can relate this to the Josephson energy using the equation:

$$E_J = \frac{\phi_0}{2\pi}I_c \tag{2}$$

Where here, ϕ_0 is the magnetic flux quanta. Combining these equations and approximating the hyperbolic tangent term to be equal to 1, this relation reduces to:

$$E_J(\text{GHz}) = \frac{142}{R_n(\text{k}\Omega)} \tag{3}$$

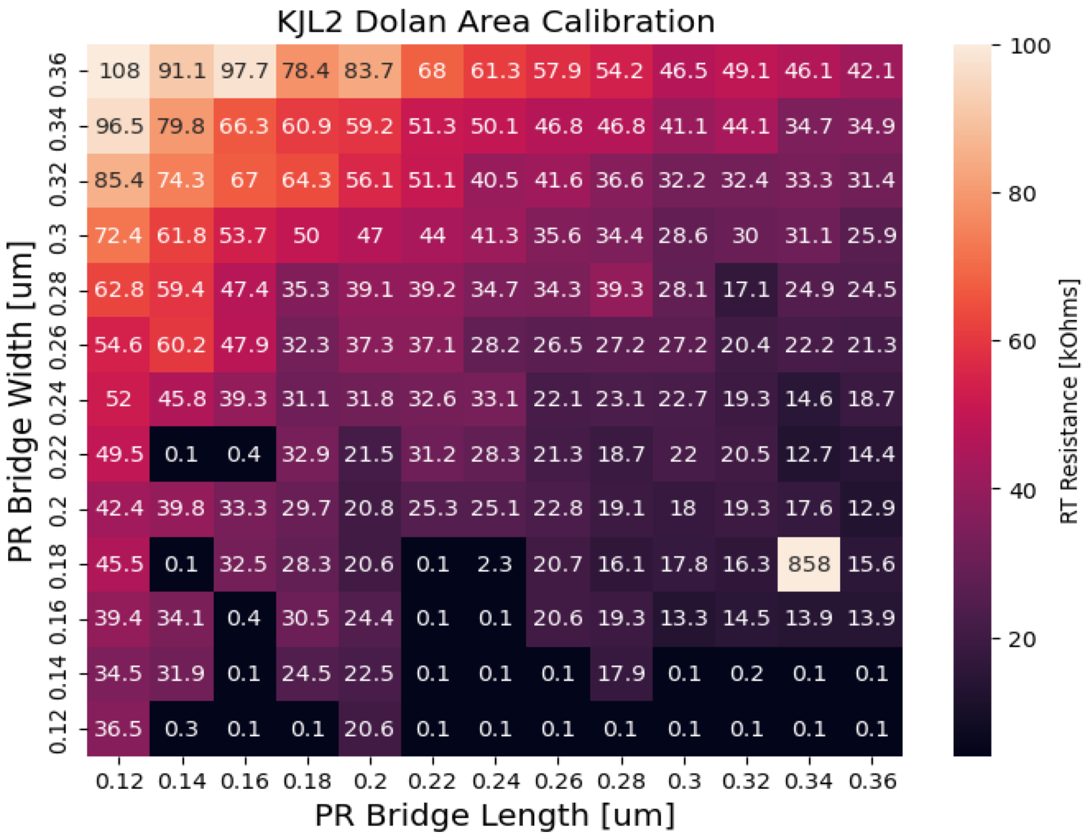


Figure 11: Junction resistances as a function of design parameters.

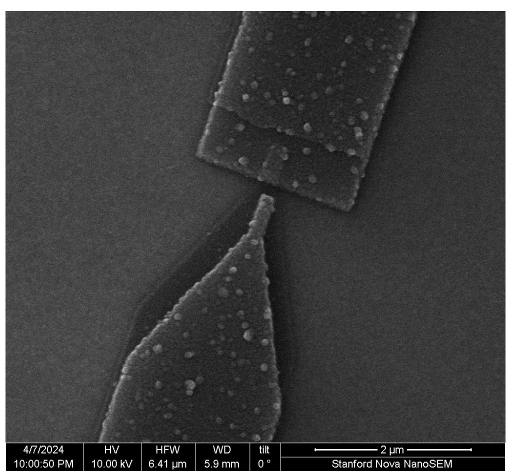


Figure 12: An SEM photo showing a working Josephson junction.

In practice, the prefactor of 142 has been found to vary slightly based on the probe station being used. Group members have anecdotally found it to be closer to 120. In the next section, we outline how we calibrated the ion mill step in order to enable this two deposition junction method.

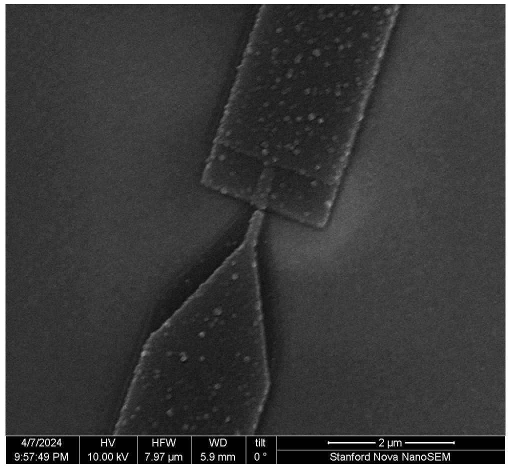


Figure 13: An SEM photo showing a junction with top and bottom layers shorted together.

3 Calibrating the Ion Mill

3.1 Introduction

Before we were able to make working JJs, we first had to calibrate the in-situ ion mill in KJL2. Immediately after depositing the ground plane, we have a metal layer without any oxide. However, in order to do the subsequent etching and lithography steps, we unavoidably expose this metal layer to atmosphere, forming an oxide. If this oxide isn't removed before the double-angle evaporation step, we will have poor electrical contact and create stray Josephson junctions. This also would add to our normal resistance, leading to an incorrect estimation for the calibrated JJ area to get the qubit parameters we want. To address these problems, we introduce an in-situ ion mill step before the first angled Al deposition, removing this native oxide and enabling good electrical contact.

As some of the first users of the ion mill functionality, we didn't have any estimates for which protocol to use. The KJL2 tool has a KRI eH 400 Ion Source, which differs from the KRI KDC 40 Ion Source for which our lab group has previously developed recipes. These are ion sources which rely on different operating methods, so we needed to calibrate the amount of ion milling to remove the native oxide. Table 1 gives the four available ion mill recipes. We also knew that from previous tests that 10 minutes of ion milling burnt electron beam resist and 5 minutes substantially reduced the size of bridges. As a result of these problems, we decided to try initial testing with recipe 3 instead, as this had the lowest discharge volts.

Table 1: KJL2 ion mill recipe parameters. Program 3 is the one we characterized.

Program #	1	2	3	4
Gas Flow (sccm)	23	23	23	23
Discharge Volts (V)	150	150	100	200
Discharge Current (A)	2	2.66	3	2
Emission Current (A)	2	2.66	3	2

To get an initial estimate of the ion mill rate, we deposited a thin layer of Nb and Al on a transparent substrate (sapphire). We then iteratively ion milled and checked to see if the substrate was visible through a view-port in the KJL2 tool. For these initial tests, we did not get an estimate for the oxide or metal thicknesses beyond the crystal monitor deposited amount. We treated this as an initial test to check that the ion milling rate is roughly on the same rate as the literature values. Our rough conclusions are shown in table 2. As we only had a rough estimate for the metal and oxide thicknesses, the right amount of ion milling to remove all of the Nb oxide could vary a large amount from these ion milling rates.

Table 2: Full wafer ion mill estimates for Nb on recipe 3.

Metal Stack	Base Metal Layer Thickness (nm)	Total Ion Mill Time (s)	Ion Mill Rate (nm/s)	Literature Ion Mill Rate (nm/s) [5]
Nb	20	960	0.02	0.033 ± 0.004
Nb and Nb Oxide	19 and 2	1080	0.02 and 0.011	-

As we cannot use a thickness measurement for the oxide amount remaining due to the oxide forming quickly after being removed from the KJL2, we decided to measure the resistance of the oxide between two layers of metal instead. The schematic of this calibration is shown in Fig.14. By increasing the amount of ion milling, eventually all of the native oxide will be milled away, leading to plateau in the resistance. The optimal etch time will be once the resistance plateaus.

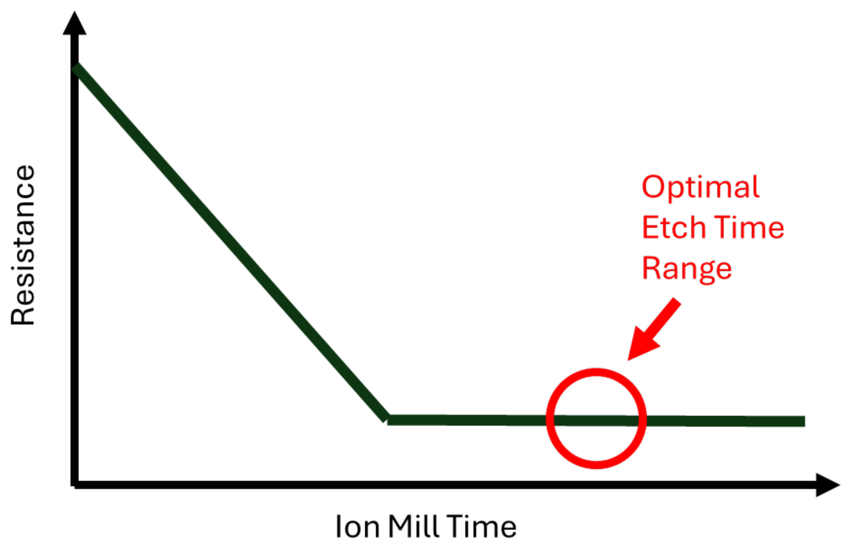


Figure 14: Cartoon of ion mill calibration. With increased ion milling, the oxide between the Nb and Al layers decreases in thickness, decreasing the resistance. After all of the oxide is milled away, the resistance will plateau at the residual resistance from the Al and Nb thin-films.

3.2 Process Flow

We require two steps of photolithography to pattern the two layers of metal with the native oxide in-between. The full process flow for these test devices is shown in Fig.15.

Our process with parameters is:

1. **Clean wafer** *(SNSF Solvent Bench)*: sonicate in acetone, methanol, IPA for 3 min in order. Then DI rinse for 1 minute.
2. **Deposit Nb** *(SNSF KJL2)*: Load wafer into chamber and pump to <1e-6. Deposit 20 nm of Nb with 10 rpm rotation, 0.2 nm/s.

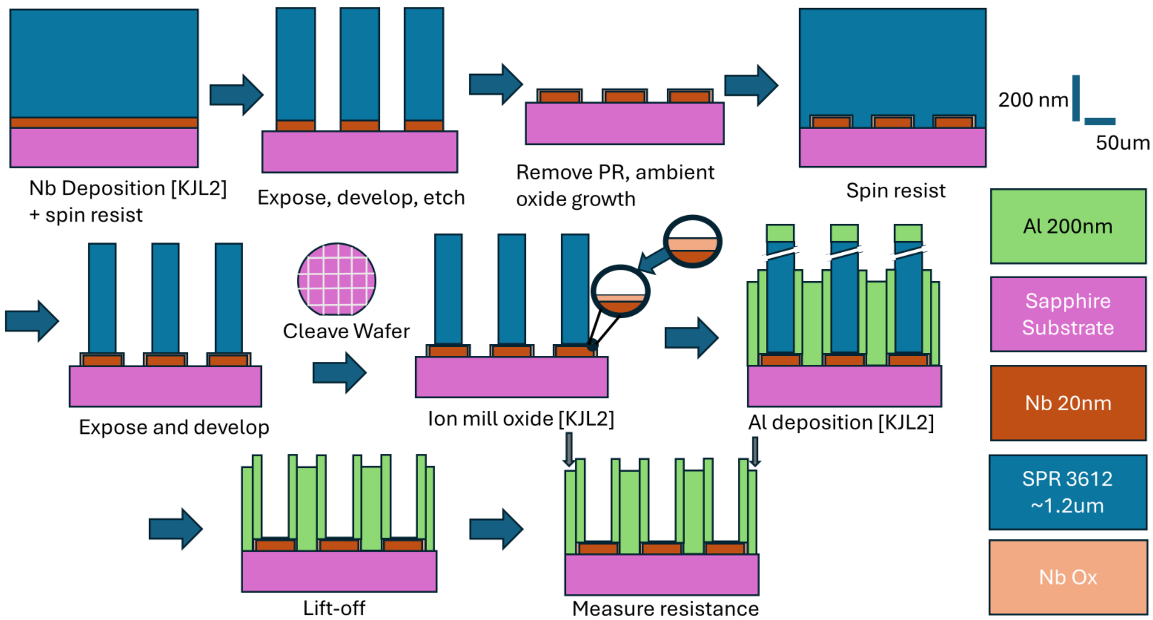


Figure 15: Block diagram for devices to test the ion mill rate in KJL2.

3. **Photolithography 1** *(SNF headway2, heidelberg2, wbexfab_dev)*: Spin SPRN3612, 4000 rpm, 1000 rpm/s ramp, 45 s. Soft bake 90 s at 90°C. Expose inverted pattern 1 on Heidelberg 2 with optical focus, 100 dose, -2 defocus. Post exposure bake 60 s at 115°C. Develop in MF26A for 35s still 35s agitating. Rinse in DI wafer 20 s and dry with N2 gun.
4. **Etch Nb** *(SNSF Oxford RIE)*: Clean chamber using `SLAB_O2_Clean`. Load dummy sapphire wafer, run `SLAB_Nb_Etch_seasoning`: SF_6 - 50 sccm, Ar - 7.0 sccm, O_2 - 4.9 sccm, pressure - 20 mTorr, forward power 20 W. Remove dummy wafer and put device wafer in, run `SLAB_Nb_Etch_120s`, which has the same parameters as above but for 120 s. Check that the substrate is see-through to ensure the Nb has been removed.
5. **Strip/Clean** *(SNSF Solvent Bench)*: Soak in Remover PG (NMP) at 80°C overnight. Run AMI clean as in the first step.
6. **Photolithography 2** *(SNF headway2, heidelberg2)*: Spin SPRN3612, 4000 rpm, 1000 rpm/s ramp, 45 s. Soft bake 90 s at 90°C. Expose pattern 2 on Heidelberg 2 with optical focus, 100 dose, -2 defocus. Post exposure bake 60 s at 115°C.
7. **Cleave Wafers** *(SNSF FlipScribe)*: Cleave wafer into chips. See the NanoNugget in appendix C for further details.
8. **Develop Chips** *(SNF wbexfab_dev)*: Develop in MF26A for 35s still 35s agitating. Rinse in DI wafer 20 s and dry with N2 gun.
9. **Ion Mill and Al Deposition** *(SNSF KJL2)*: Load one of the chips into chamber. Pump to <5e-6, run ion mill recipe 3 with 10rpm rotation, 120s warm up, for chosen ion mill times (0s, 60s, 15s, 30s). and pump to <1e-6. Deposit 200 nm of Al with 10 rpm rotation, 0.2 nm/s. Use 1A/s recipe.
10. **Lift Off** *(SNSF Solvent Bench)*: Put chips into small beakers of Remover PG. Put on 80°C hot plate overnight. Use a glass pipette to agitate the liquid and enable lift-off. Clean chips using AMI clean.
11. **Measure Resistances** *(SNF Micromanipulator6000)*: 2-pt using `LINQS_JJ` recipe.

3.3 Mask Design

After some iteration, we decided on using the mask shown in Fig.16. As it has a wide range of overlaps, this ensures that if the resistance from the oxide is too small, we will have enough contrast by measuring multiple effective resistors in series.

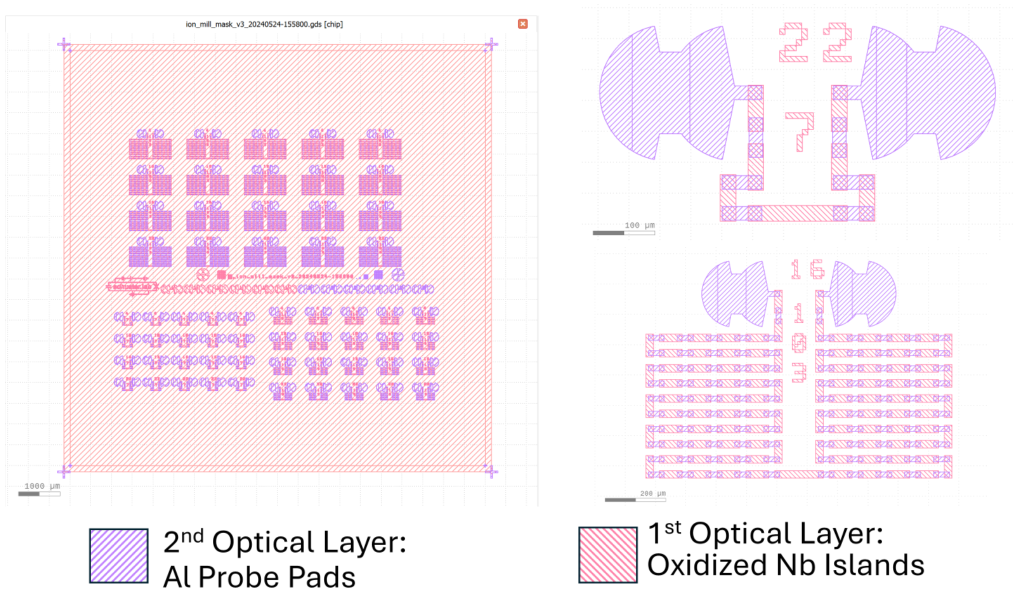


Figure 16: Mask for testing ion mill rate in KJL2. The probe structures have 7, 19, and 103 Nb islands, leading to 14 and 38, and 206 overlaps with Nb oxide between the two metal layers. In the center we have shorted features of only Al and only Nb for comparison. We also included Van der Pauw structures to measure sheet resistance.

3.4 Fabrication and Experiment

We tested 4 chips at 0 s, 15 s, 30 s, and 60 s ion mill times. The results of two-point probing is shown in Fig.17. We then plot the average resistance in Fig.18. We clearly see a decrease in the measured resistance from 0 s of ion milling to 15 s, however the resistance does not drop to 0. The dotted lines are an approximation for the amount of geometrical resistance remaining from having a thin film wire of Nb. For our Nb, we measured a sheet resistance of 40 $\Omega/\square$. This indicates that after 15 s, we have removed most of the oxide. The Al sheet resistance was between 200 m$\Omega/\square$ and 250 m$\Omega/\square$, so does not contribute much to the geometrical residual resistance.

4 Future Work & Conclusion

As an extension to this work, HM and PV intend to fabricate a transmon qubit sample in the KJL2 following the recipes developed during this course. Once fabricated, we will mount the sample in a dilution refrigerator (DR) to measure its coherence times. Using a flux-tunable transmon design, we will scan qubit frequency, searching for avoided crossings indicative of interactions with TLS (two-level-system) style material defects. The coherence of this will be compared to that of devices made in the LINQS group's plassys evaporator by Eesh Gupta. Additionally, we can also validate the ion mill times by cooling an ion mill sample to below the Al and Nb superconducting transition temperatures, so any residual resistance would come from the oxide between the layers.

HM intends to explore fabricating Josephson junctions using alternate superconducting materials. Recipes from this project are already being used to fabricate Titanium junctions. Next steps

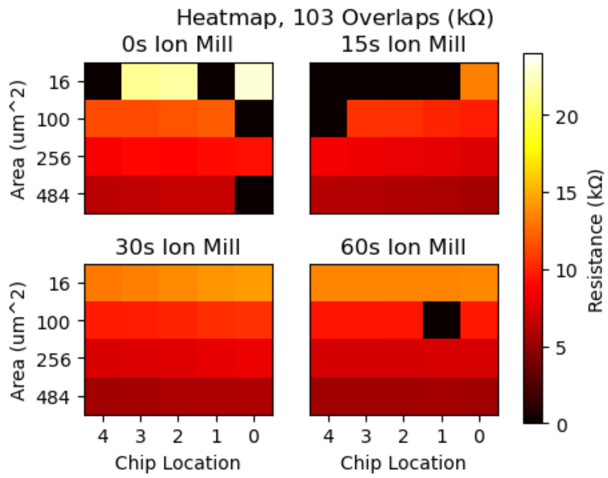


Figure 17: Heatmap of measured resistances for various ion mill times. Black squares indicate either shorted, open, or missing patterns.

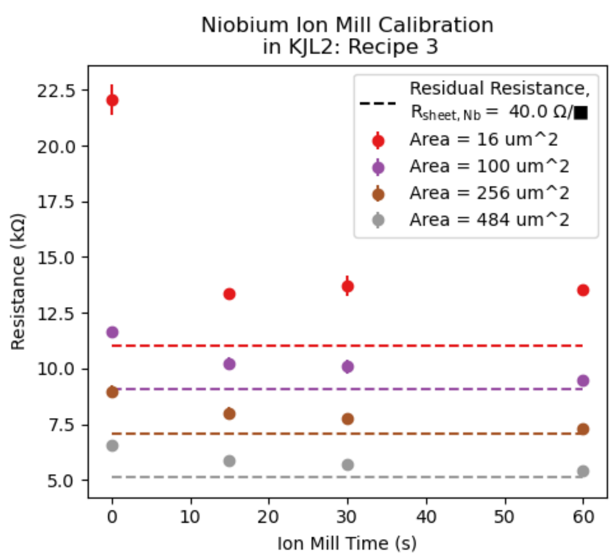


Figure 18: Average resistance from ion mill patterns.

involve measuring IV curves through the junction in a dilution fridge, and if they prove functional at low temperatures, incorporating them into transmon style devices. PV will use this process to fabricate fluxonium superconducting qubits, using KJL2 as a potential method for creating Josephson juncitons.

To mitigate wafer alignment issues during the KJL mounting stage, HM plans to work with an undergraduate intern to design a 3D printed mounting jig. The jig will screw onto the KJL plate and serve as a flat edge against which to mount the wafer. Once the wafer is secured, the 3D printed jig will be removed prior to deposition. Additionally, Grant Shao will be making changes to the mounting methods in KJL2, allowing easier alignment and more repeatable depositions.

5 Acknowledgement

We would like to express our gratitude for several individuals who have been instrumental in the success of this project. First and foremost, we thank Grant Shao for his support. He ensured that the KJL2 remained operational throughout the duration of the project, debugged the many errors we ran into, and debriefed with us when our results were unexpected. This project would not have been possible without his hard work.

We also extend our thanks to our mentors, Usha Raghuram and J Provine, for their insightful feedback. Their advice was invaluable in navigating many of the challenges we faced. In particular, they helped us to understand the reason why our Niobium liftoff did no go as planned, and suggested many creative workarounds to the problem. Similarly, we want to thank our advisors, David Schuster and Noah Kurinsky for supporting this project and regularly checking in to discuss progress and debug issues. Their advice, along with that of Shannon Harvey, Ziqian Li, Zoë Smith, and Wendy Wan was instrumental in helping us understand and implement existing group recipes.

We are grateful for Swaroop Kommera and Jason Tower, as they engaged in productive discussions about our processes. Along with the rest of the SNF and SNSF team, they kept the cleanrooms functional and free of floodwater. We also recognize that it wouldn't have been possible without the support of C-ShARP and the Deans, for which we are exceptionally thankful! Finally, we are thankful for the leadership of the ENGR241 teaching team, including Debbie Senesky and Sergio Cordero who kept the course exceptionally organized and always had insightful comments during class. This course provided us with the opportunity and funding to gain valuable nanofabrication experience. Over the quarter, we developed our knowledge-base while exploring new recipes to share with other users.

6 References

References

[1] Vinay Ambegaokar and Alexis Baratoff. "Tunneling Between Superconductors". In: *Phys. Rev. Lett.* 10 (11 June 1963), pp. 486–489. DOI: 10.1103/PhysRevLett.10.486. URL: https://link.aps.org/doi/10.1103/PhysRevLett.10.486.

[2] Frank Arute et al. "Quantum supremacy using a programmable superconducting processor". In: *Nature* 574.7779 (Oct. 2019), pp. 505–510. ISSN: 14764687. DOI: 10.1038/s41586-019-1666-5. (Visited on 06/16/2020).

[3] Aaron Chou et al. *Quantum Sensors for High Energy Physics*. Nov. 2023. DOI: 10.48550/arXiv.2311.01930. URL: http://arxiv.org/abs/2311.01930 (visited on 11/07/2023).

[4] Ruichao Ma et al. "A dissipatively stabilized Mott insulator of photons". en. In: *Nature* 566.7742 (Feb. 2019), pp. 51–57. ISSN: 1476-4687. DOI: 10.1038/s41586-019-0897-9. URL: https://www.nature.com/articles/s41586-019-0897-9 (visited on 09/13/2023).

[5] *Technics Ion Mill Etch Rates*. URL: https://apps.mnc.umn.edu/pub/equipment/ionmill_rates.pdf.

A Budget

The budget spending breakdown is shown in Fig.19.

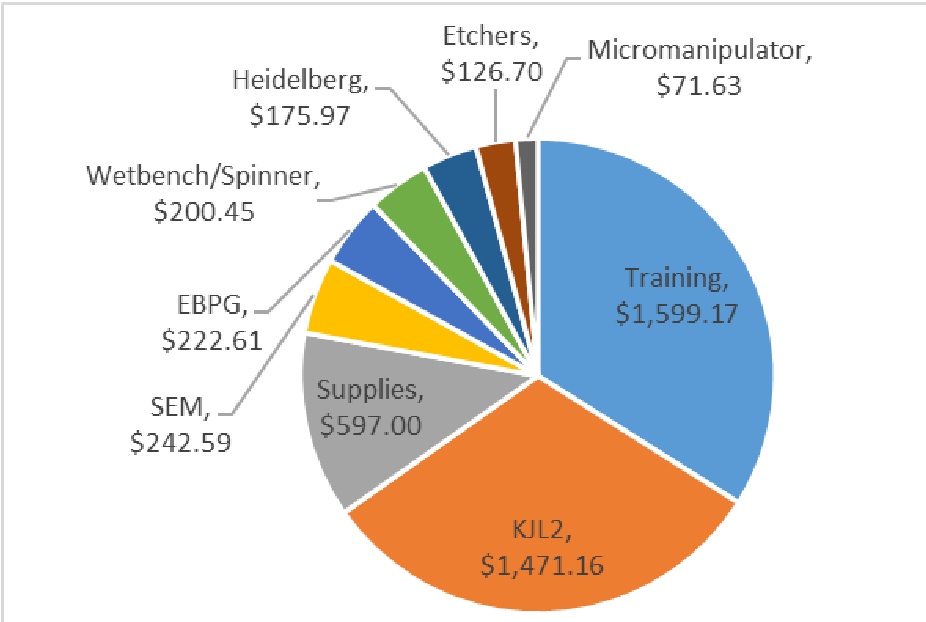


Figure 19: Budget allocation. Total usage: $4707.27.

B SOP: Josephson Junctions in KJL2

B.1 Wafer Cleaning

The following recipe is used to clean new sapphire wafers.

Location: SNSF Wetbench

- Sonicate in toluene for 3 minutes at power=3.
- Sonicate in acetone for 3 minutes at power=3.
- Sonicate in methanol for 3 minutes at power=3.
- Sonicate in IPA for 3 minutes at power=3.
- Dunk in beaker of DI water. Rinse under faucet for 1 minute.
- N2 dry.
- Bake dry at 180C for 5 minutes. Inspect under microscope for debris.

B.2 Niobium Ground Plane Deposition

The following recipe is used to deposit a base layer of Nb.

Location: KJL2 in SNSF

- Use N2 gun to blow debris off of the KJL2 mount plate. Mount wafer in the center of the KJL2 plate. Use N2 gun to blow any debris off of the mounted wafer. Mount plate in the load lock, and begin pumpdown sequence.
- Pump down chamber until desired pressure is reached. We observed a diminishing return to pumping on the chamber for longer than 7 hours. A plot of load lock pressure as a function of pump time is given in Fig. 20.
- Use controller to rotate the KJL2 mount plate such that the large metal extrusion is facing the window. Once this position is reached, tilt the plate 90 degrees. Watch through the window to ensure that the rotation of the plate remains in the desired location.
- Run a titanium-getter step to reduce substrate chamber pressure. Note that due to the 90 degree tilt of the mount plate, the wafer will not be coated in a layer of titanium. This deposition is only intended to coat the surrounding chamber walls. The following parameters are used:
  - **Rotation:** No
  - **Rotation Speed:** 0 rpm
  - **Tilt Station:** Tilt 90
  - **Deposition Rate:** 2.0 A/s
  - **Deposition Amount:** 0.15 kA
- Tilt the mount plate back to the "standard" location. The mount plate should be facing down towards the evaporator source.
- Deposit Nb with the following parameters:
  - **Rotation:** Yes
  - **Rotation Speed:** 10 rpm
  - **Tilt Station:** Standard
  - **Deposition Rate:** 3.0 A/s
  - **Deposition Amount:** 1 kA

  Note that for higher quality Nb films, higher deposition rates may be desired. Currently, access to these higher deposition rates require users to undergo an additional training session with Grant Shao.
- Vent the load lock and remove sample. Place wafer case in a cleanroom bag. Use the N2 gun near the KJL2 to first flush any air out of the bag, and inflate it partially with nitrogen. This will help reduce the rate of oxide growth on the sample.

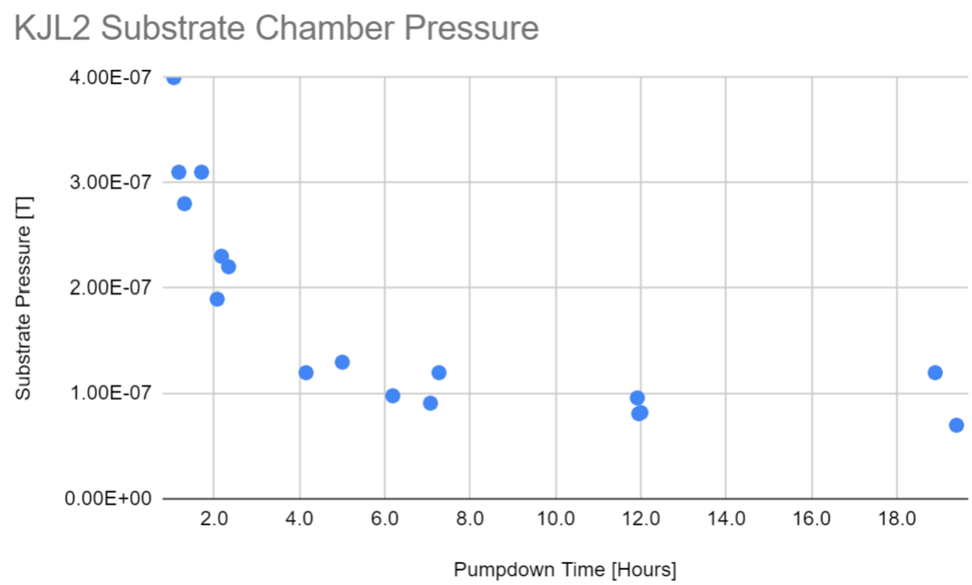


Figure 20: A scatterplot displaying KJL2 load lock pressure as a function of pumpdown time.

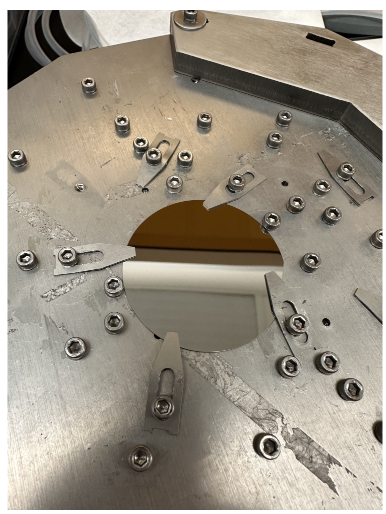


Figure 21: A photograph of a wafer following a KJL2 niobium deposition.

B.3 Wafer Cleaning

Location: SNSF Wetbench

- Sonicate in acetone for 3 minutes at power=3.
- Sonicate in methanol for 3 minutes at power=3.
- Sonicate in IPA for 3 minutes at power=3.
- Dunk in beaker of DI water. Rinse under faucet for 1 minute.
- N2 dry.
- Bake dry at 180C for 5 minutes.

B.4 Spin Photoresist

Location: SNF Headway 2

- Set up spin recipe:
  - **Step One:** Speed = 4000 rpm, Ramp = 1000 rpm/s, Time = 45 s
  - **Step Two:** Speed = 0 rpm, Ramp = 1000 rpm/s, Time = 5 s
- Bake wafer on 90 degree hotplate for 90 seconds. Remove lid of hotplate 15 seconds before the time is up. Begin pushing wafer to edge of hotplate 5 seconds before time is up. Cool wafer on a clean piece of foil before placing into plastic wafer case.
- If edge beads are present, remove with acetone swab.

B.5 Expose Photoresist

Location: SNF Heidelberg 2

- Expose with Dose = 100, Defor= -2
- Post exposure bake on 115 degree hotplate for 60 seconds.

B.6 Develop Photoresist

Location: SNF Wetbench Dev Flex

- Fill one beaker with MF26A, and two beakers with DI water.
- Place wafer into MF26A beaker for 70 seconds total. Agitate the beaker gently for the first 35 seconds. Let the beaker sit for the next 35 seconds.
- Remove the wafer from the developer and quickly transfer to the first DI water beaker. When removing the wafer, try to minimize the area that emerges from the surface of the water (i.e. tilt wafer vertical while removing).
- Let wafer sit in DI water for 20 seconds. Transfer to second DI water beaker.
- Let wafer sit in DI water for 5 seconds.
- Rinse wafer under faucet for 2 minutes. N2 dry.
- Examine under microscope. Ensure that exposed regions have clear edges. Look for rainbow effects across the wafer or a blue glow around features indicating changes in resist height.

B.7 Dry Etch

Location: SNF PT-MTL

- Mount dummy 4" wafer into the PT-MTL. Run default O2 chamber clean #1 recipe.
- Vent chamber. Check that 4" wafer mounting is still sufficient. Remount dummy wafer.
- Run "season" chamber recipe with the dummy wafer. Use recipe: 15 sccm SF6, 40 sccm CF4, 5 mT pressure 500 W ICP, 75 W Bias. Run the main etch for 360 seconds.
- Mount actual wafer. If you are using a 2" wafer, use santovac oil to mount it to a 4" carrier wafer. Apply approximately 5 drops of oil to the carrier wafer. Place the 2" wafer on top. Press gently on the edges of the 2" wafer to spread the oil. You should be able to press and slide the 2" wafer around slightly without resistance/scraping. If excess oil emerges from the sides, remove it with IPA. If the 2" wafer scrapes while sliding, remove it and add another drop of oil.
- Run etch recipe for 130s using the same parameters as before.
- Inspect under optical microscope. Look for tinted sapphire (indicating under-etch), or jagged feature edges (indicating contamination).

B.8 Remove PR

Location: SNSF Wetbench

- Place wafer in beaker of Remover PG. Cover beaker with tin foil and place beaker on 80C hot plate.
- Let sit for 4-8 hours.
- Sonicate in acetone for 3 minutes at power=3.
- Sonicate in IPA for 3 minutes at power=3.

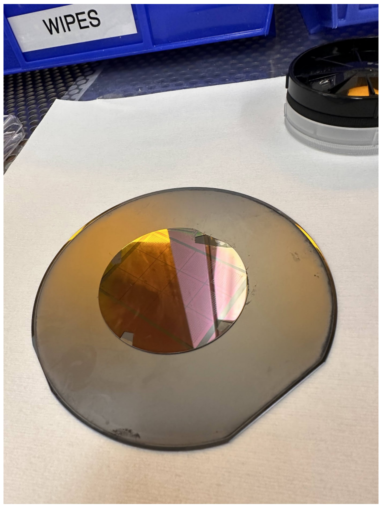


Figure 22: Photograph of mounting scheme for 2” wafer in PT-MTL.

- Dunk in beaker of DI water. Rinse under faucet for 1 minute.
- N2 dry.
- Bake dry at 180C for 5 minutes.

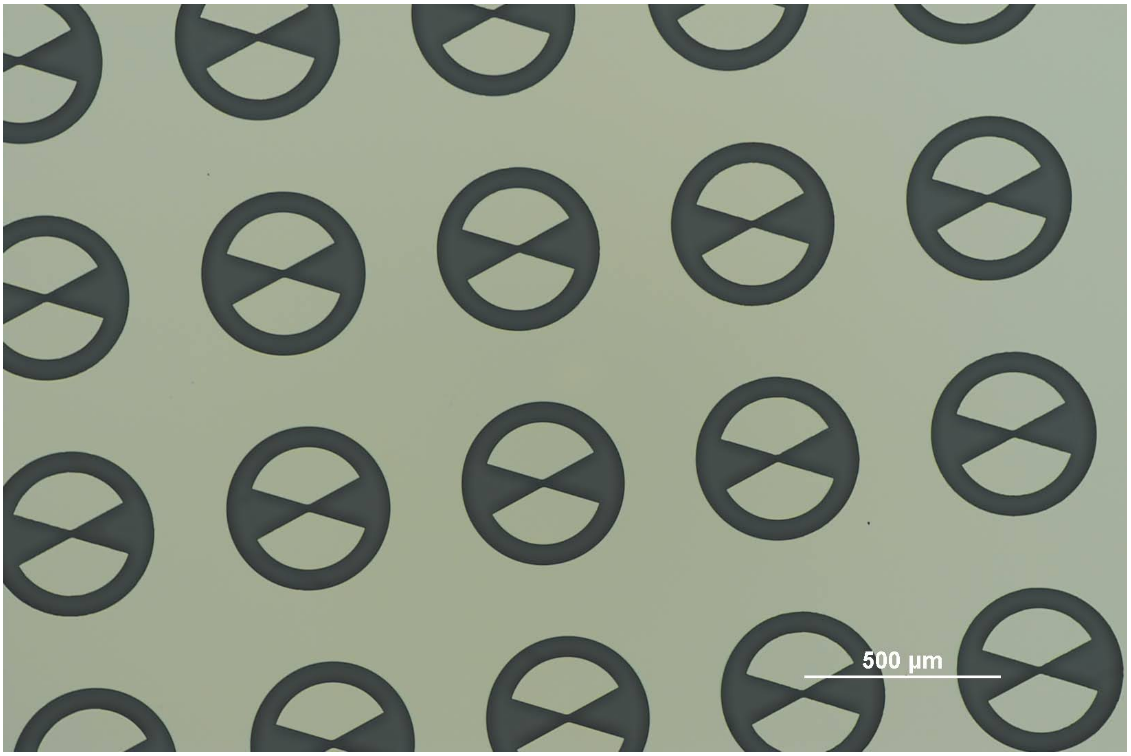


Figure 23: Optical microscope photograph of the etched probe pad base layer.

B.9 Spin Ebeam Resist

Location: SNSF Spinner

- Spin MMA (8.5) EL 13

  - **Step One:** Speed = 6000 rpm, Ramp = 1000 rpm/s, Time = 90 s
  - **Step Two:** Speed = 0 rpm, Ramp = 1000 rpm/s, Time = 7 s
- Bake 180 C 5 minutes on clean piece of tin foil.
- Spin PMMA 950 A4
  - **Step One:** Speed = 2000 rpm, Ramp = 1000 rpm/s, Time = 90 s
  - **Step Two:** Speed = 0 rpm, Ramp = 1000 rpm/s, Time = 3 s
- Bake 180 C 5 minutes on clean piece of tin foil.
- Spin first coat of Electra
  - **Step One:** Speed = 4000 rpm, Ramp = 1000 rpm/s, Time = 60 s
  - **Step Two:** Speed = 0 rpm, Ramp = 1000 rpm/s, Time = 5 s
- Bake 90 C 2 minutes on clean piece of tin foil.
- Spin second coat of Electra
  - **Step One:** Speed = 4000 rpm, Ramp = 1000 rpm/s, Time = 60 s
  - **Step Two:** Speed = 0 rpm, Ramp = 1000 rpm/s, Time = 5 s
- Bake 90 C 2 minutes on clean piece of tin foil.

B.10 Aligned Ebeam Exposure

Location: SNSF EBPG 2

- Align to marks on first layer. In our masks, we include 40 µm square alignment marks on the corners of our chips. Since they are etched from the Niobium base plane, they are considered "negative" alignment marks. These marks are visible in SEM without needing to apply sharpie to the bottom of the sapphire wafer.
- Expose full cut through both PMMA and MMA with dose = 1450 µC/cm2. Expose undercut through MMA only with dose = 362.5 µC/cm2. For small junction features, use 10nA beam current.

B.11 Develop Ebeam Exposure

Location: SNSF Wetbench

- At least 60 minutes in advance, combine 45mL of IPA and 15mL of DI water in a beaker as developer. Cover with tin foil and place the developer mixture on the 6C cold plate. Applying a drop of water beneath the beaker will help it reach temperature faster.
- Place wafer in beaker of DI water for 60 seconds to remove electra.
- Rinse wafer under faucet for 60 seconds.
- N2 dry
- Place wafer in developer for 90 seconds. Do not remove developer from the cold plate to do this.
- Dunk wafer in IPA for approximately 3 seconds.
- N2 dry. Use low power on the N2 gun to avoid breaking the Dolan bridges. Do not hold the gun too close to the wafer. The bridges are extremely fragile.
- Examine under microscope. By adjusting the focus of the microscope, you should be able to resolve the upper and undercut layers of the Dolan bridge.

B.12 Junction Deposition

Location: KJL2 in SNSF

- Use N2 gun to debris off of the KJL2 mount plate. Use sharpie the side of the KJL2 plate along the sides shown in Fig. 24. Mount wafer in the center of the KJL2 plate as shown in the image. The Dolan junctions should be oriented as shown in Fig. 25 to ensure correct ordering of depositions with respect to the bridge. Carefully align wafer such that the wafer flat is parallel with the bottom of the extrusion feature on the plate. DO NOT USE N2 gun on wafer because you may risk damaging the Dolan bridges. Mount plate in the load lock,

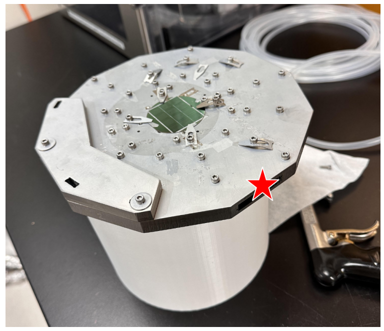


Figure 24: Photograph of wafer mounted on KJL plate. Left face of plate is marked with a red star, and should be rotated to face the KJL window during junction depositions.

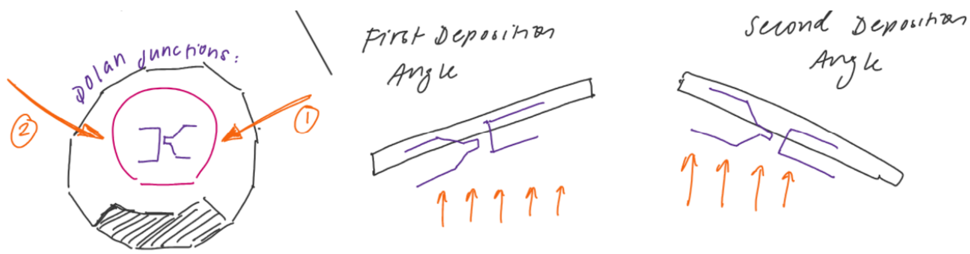


Figure 25: Orientation of Dolan junction bridges with respect to KJL mounting plate.

and begin pumpdown sequence.

- Pump down chamber until desired pressure is reached. We observed a diminishing return to pumping on the chamber for longer than 7 hours. A plot of load lock pressure as a function of pump time is given in 20.
- Use controller to rotate the KJL2 mount plate such that the large metal extrusion is facing the window. Once this position is reached, tilt the plate 90 degrees. Watch through the window to ensure that the rotation of the plate remains in the desired location.
- Run a titanium-getter step to reduce substrate chamber pressure. Note that due to the 90 degree tilt of the mount plate, the wafer will not be coated in a layer of titanium. This deposition is only intended to coat the surrounding chamber walls. The following parameters are used:
  - **Rotation:** No
  - **Rotation Speed:** 0 rpm
  - **Tilt Station:** Tilt 90
  - **Deposition Rate:** 2.0 A/s
  - **Deposition Amount:** 0.15 kA
- Tilt the plate to angle +23 degrees. Use the controller to rotate until the face marked with a star in Fig. 24 is facing the window. Take care to ensure that the face is exactly parallel with the window slots. Note that we run the tilt recipe before adjusting rotation because the plate tends to shift when tilted.
- Deposit first layer of Aluminum using recipe:
  - **Rotation:** No
  - **Rotation Speed:** 0 rpm
  - **Tilt Station:** Tilt +23
  - **Deposition Rate:** 3.0 A/s

  - **Deposition Amount:** 0.45 kA
- Tilt the plate back to the "Standard" tilt station
- Run Dynamic Oxidation at 6T for 50 minutes.
- Following the oxidation step, run "substrate pump" and wait until the chamber reaches 4e-7 Torr.
- Use controller to rotate the KJL2 mount plate such that the large metal extrusion is facing the window. Once this position is reached, tilt the plate 90 degrees. Watch through the window to ensure that the rotation of the plate remains in the desired location.
- Run a titanium-getter step to reduce substrate chamber pressure. Note that due to the 90 degree tilt of the mount plate, the wafer will not be coated in a layer of titanium. This deposition is only intended to coat the surrounding chamber walls. The following parameters are used:
  - **Rotation:** No
  - **Rotation Speed:** 0 rpm
  - **Tilt Station:** Tilt 90
  - **Deposition Rate:** 2.0 A/s
  - **Deposition Amount:** 0.15 kA
- Tilt the plate to angle -23 degrees. Use the controller to rotate until the face marked with a star in Fig. 24 is facing the window. Take care to ensure that the face is exactly parallel with the window slots. Note that we run the tilt recipe before adjusting rotation because the plate tends to shift when tilted.
- Deposit first layer of Aluminum using recipe:
  - **Rotation:** No
  - **Rotation Speed:** 0 rpm
  - **Tilt Station:** Tilt +23
  - **Deposition Rate:** 3.0 A/s
  - **Deposition Amount:** 1.15 kA

  An asymmetric junction pad recipe is used here to suppress quasiparticle tunneling events. With this configuration, there is a gap-engineered potential between the two junction pads, thus creating a preferred tunneling direction and minimizing the repeat tunneling of quasiparticles back and forth across the junction.
- Tilt the plate back to the "Standard" tilt station
- Run Dynamic Oxidation at 6T for 20 minutes to passivate the top layer and promote uniform oxide growth.
- Vent the load lock and remove the wafer.

B.13 Liftoff

Location: SNSF Wetbench

For this calibration process, we did not dice the wafer into chips. Instead, we deposited junctions on one chip at a time, allowing all recipes to share the same optical layer. If instead, one wishes to dice into chips, it is recommended that dicing occurs before liftoff. This protects the junctions from an unnecessary liftoff, and prevents ESD events during the dicing process.

Liftoff follows the procedure:

Location: SNSF Wetbench

- Place wafer in beaker of Remover PG. Cover beaker with tin foil and place beaker on 80C hot plate.
- Let sit for 4-8 hours.
- Use a glass pipette to create gently currents in the water. This should remove the Aluminum

liftoff layer. Use the glass pipette to catch floating clumps of aluminum. Blot in cleanroom wipe. Attempt to remove as much of the Aluminum debris as possible before dumping the contents of the beaker into the solvent waste.

- Place wafer in acetone beaker for 2 minutes.
- Place wafer in IPA beaker for 2 minutes.
- Dunk in beaker of DI water. Rinse under faucet for 1 minute.
- N2 dry.

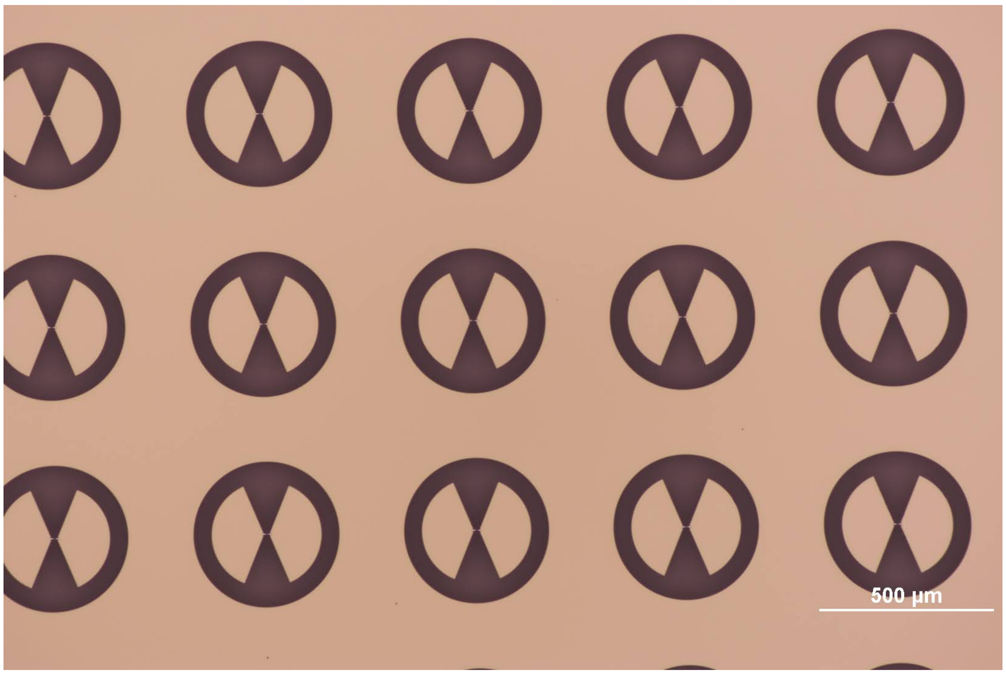


Figure 26: Optical microscope photograph of array of junctions with probe pads.

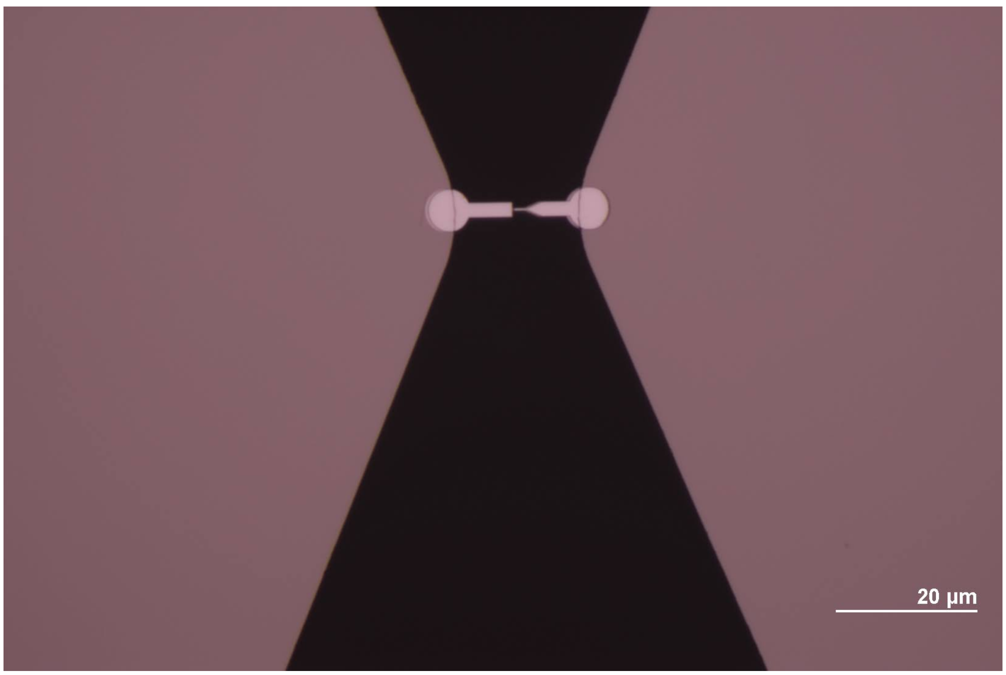


Figure 27: Optical microscope photograph of a single pixel of the array of junctions with probe pads.

C NanoNugget: Cleaving Sapphire Wafers using the SNSF Flip-Scribe

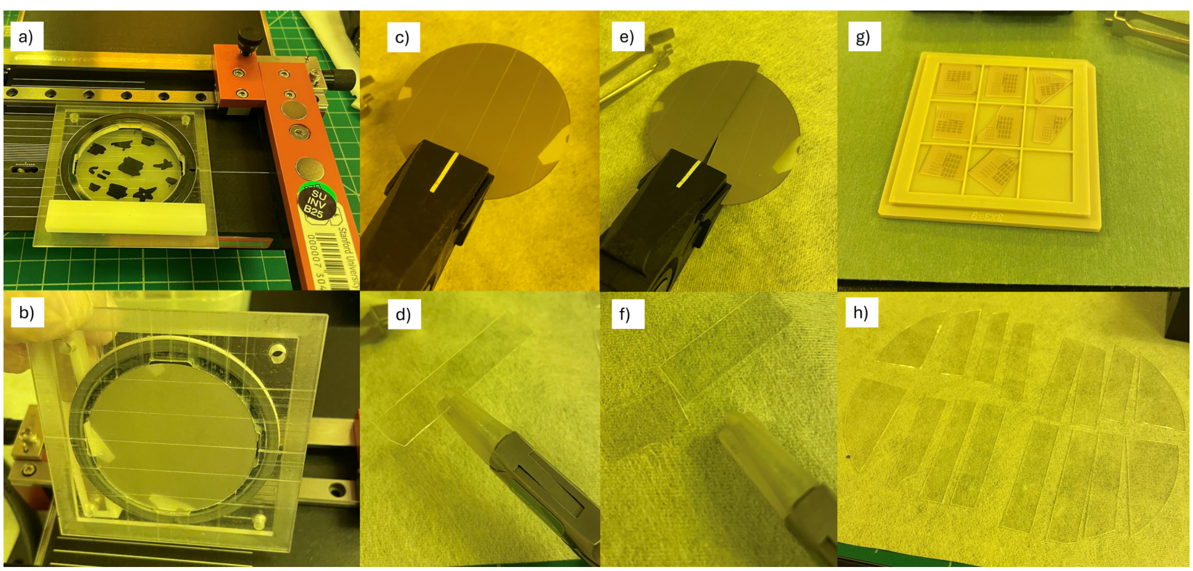
Hannah Magoon and Paul Varosy

Sapphire is a substrate used used in many superconducting circuits labs for its low dielectric loss and resistant chemistry to fluorine-based etching. Sapphire is a hardness 9 on the Mohs scale, meaning that sawing using the SNF DISCO Wafersaw can take between 3-5 hours due to the material's hardness. For non-crucial samples, using the SNSF LatticeGear FlipScribe can reduce the time required to cleave a wafer. This process is quite repeatable for double-side polished wafers, and fairly repeatable for single-side polished wafers. The SNSF SOP [1] and LatticeGear sapphire reference [2] are additional good references.

To start, properly adjust the height, following the steps in this video [3]. There is an extra glass slide which we use to check the height of the diamond tip. Move this glass slide over the diamond scribe until it just starts scraping. Then, adjust the height to half a turn higher, with the cutting facet facing along the line. We found that using a phone flashlight was helpful to align the cutting facet.

Next, place wafer/pieces inside the appropriately sized holder, as demonstrated in (a). Make sure that flat of wafer aligns with scribe direction. If using a wafer, place plastic magnetic piece, squeezing the sample inside the holder. Now, press down on the sample holder with two hands and scribe along the entire length of the sample, pressing uniformly. The scribe mark should be noticeable through the substrate and deep throughout the entire length of the wafer, such as in (b). If the scribe is not easily seen, it probably means that it wasn't deep enough, and should be re-marked. In our experience, double-side polished sapphire cleaves more easily, likely because single-side polished has more defects for the cleave to follow. Do all of the scribe marks on the entire wafer before removing it and breaking the pieces.

Start with cleaving from the flat, using the big sample cleavers, aligning the white line with the back side of the sample, shown in (c) and (e). Have the holders as close to the flat as possible. Ensure that you have a good alignment and press down gently. The wafer should break easily. If you have to press down with a large amount of force, check that the alignment is correct and/or consider scribing more deeply. Once you have pieces smaller than 20mm, cleave using the small sample cleavers, shown in (d) and (f). In testing ~10 wafers, when we had square patterns, we could get between 50-80% useful chips on single side polished (g) and $> 95\%$ with double-side polished (h).



[1] SNF SOP: https://drive.google.com/file/d/1BvsymB_CnihoTh8QCKagsJeV9-MJTQVc/view

[2] "Dicing Sapphire Wafers by Cleaving Using the LatticeAx and FlipScribe." Lattice Gear Website. https://www.latticegear.com/use-cases-and-applications-stories__trashed/cleaving-sapphire-2

[3] "Setting the FlipScribe Scribe Height and Tilt." YouTube, LatticeGear LLC. https://www.youtube.com/watch?v=d1vKYwiwFoI