Multilevel Silicon Structure and Fabricated Pushing Mold for Sample Transfer

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ENGR 241 Final Report

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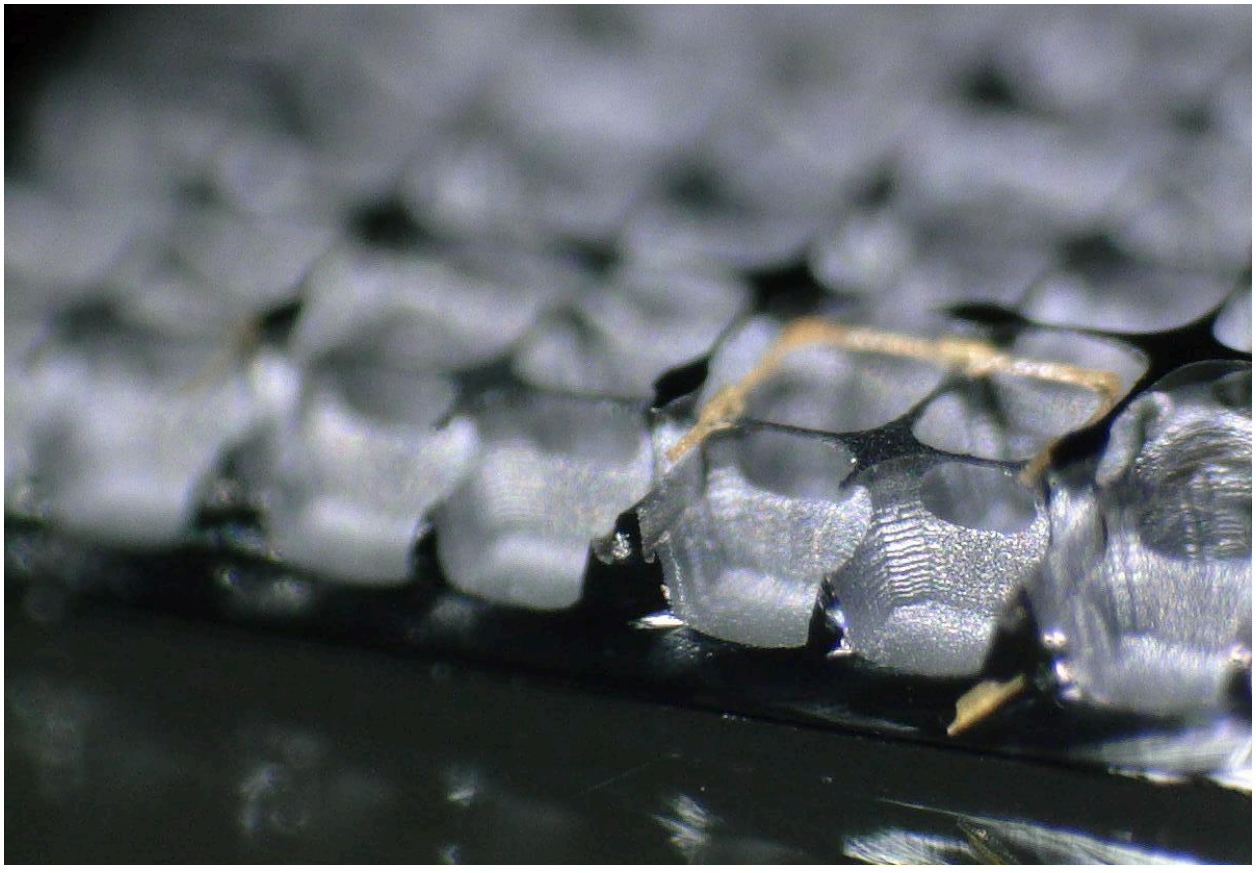

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Introduction

Motivation

Tissue microdissection plays a crucial role in various biological applications, particularly in cancer research and drug discovery. For example, patient-derived tumor organoid generation has shown great promise as a model for predicting personalized drug responses. The most common method for fragmenting tissue to generate organoids is manual dissection using scissors or scalpels. However, this process is often time-consuming and carries a risk of contamination. Additionally, the resulting tissue fragments are often large, irreproducible, and lack uniformity [1].

The Tang Group has recently published work on alternative tissue microdissection tools, the μDicer and the μGrater, which enable faster and more uniform tissue fragmentation [2, 3]. These tools not only provide more consistent fragments but also demonstrate tissue viability comparable to that of manual mincing.

Objectives

Building on the work presented in [2], our project had two main objectives:

1. **Design and fabrication of a multi-tiered silicon structure**: We aimed to explore different geometries and improve upon the fabrication techniques described in [2].
2. **Address mechanical performance limitations**: The microstructures often experience mechanical failure, especially when force is unevenly applied, leading to stress concentration and potential fracture. To mitigate this, we focused on designing a pushing

structure that would act as both a stop and a support layer for the tissue, reducing the risk of structural failure.

Benefits to the SNF Community

While working towards our project goals of creating a multi-level silicon structure, we contributed the following SOPs for the SNF community:

- **Spray Coating Recipe and Characterization of Negative Resist**: We developed a spray coating recipe for applying negative resist onto a patterned substrate, including a characterization process for improved consistency.
- **Double-Masking Process for Deep, Multi-Tiered Structures**: We introduced a double-masking approach to fabricate deep, multi-tiered silicon structures.
- **Two-Step Hybrid Oxide Etching Method**: A two-step etching approach combining dry and wet oxide etching has been developed. This method enables more precise control over sidewall and trench bottom etching than with wet etching alone.

Additionally, we have developed a basic python script to predict the etch profile of the structure using two masks. The script will be available for the general SNF community to download and modify as necessary.

Fabrication Methods

Tools Utilized in Process

The following tools were used during the fabrication process:

- PlasmaTherm Shuttlelock SLR-730-PECVD for capacitively coupled plasma deposition (CCP-DEP) of oxide on silicon.
- YES Prime Oven for dehydrating wafers at 150℃ and priming with HMDS
- SVG Resist Coat for positive resist coating
- SVG Resist Develop for resist development
- Heidelberg 2 for patterning positive photoresist
- PlasmaTherm Versaline LL ICP Dielectric Etcher for oxide dry etching
- EVG 101 Spray Coater for negative resist coating
- Karl Suss MA-6 Contact Aligner for patterning negative resist on patterned substrate
- SAMCO Ozone cleaner to clean wafer and strip photoresist
- 6:1 BOE (34% Ammonium Fluoride (NH_4F), 7% Hydrofluoric Acid, 59% Water) for oxide etch
- PlasmaTherm Deep Silicon Etch of silicon using an oxide hard mask
- Gemini Scanning Electron Microscope, Nanospec2, and Keyence Digital Microscope VHX-6000 for characterizing mask thickness and resultant etches

Overall Process Flow

Our objective was to fabricate a multi-tier deep silicon-etched structure with at least a 20 µm height difference. This etching process builds upon the methods described in [2]. In brief, single-level silicon structures were formed using alternating Bosch process etching and isotropic etching to create a tapered etch with a controllable angle. To achieve the height difference between the two levels, we introduced a two-mask fabrication process.

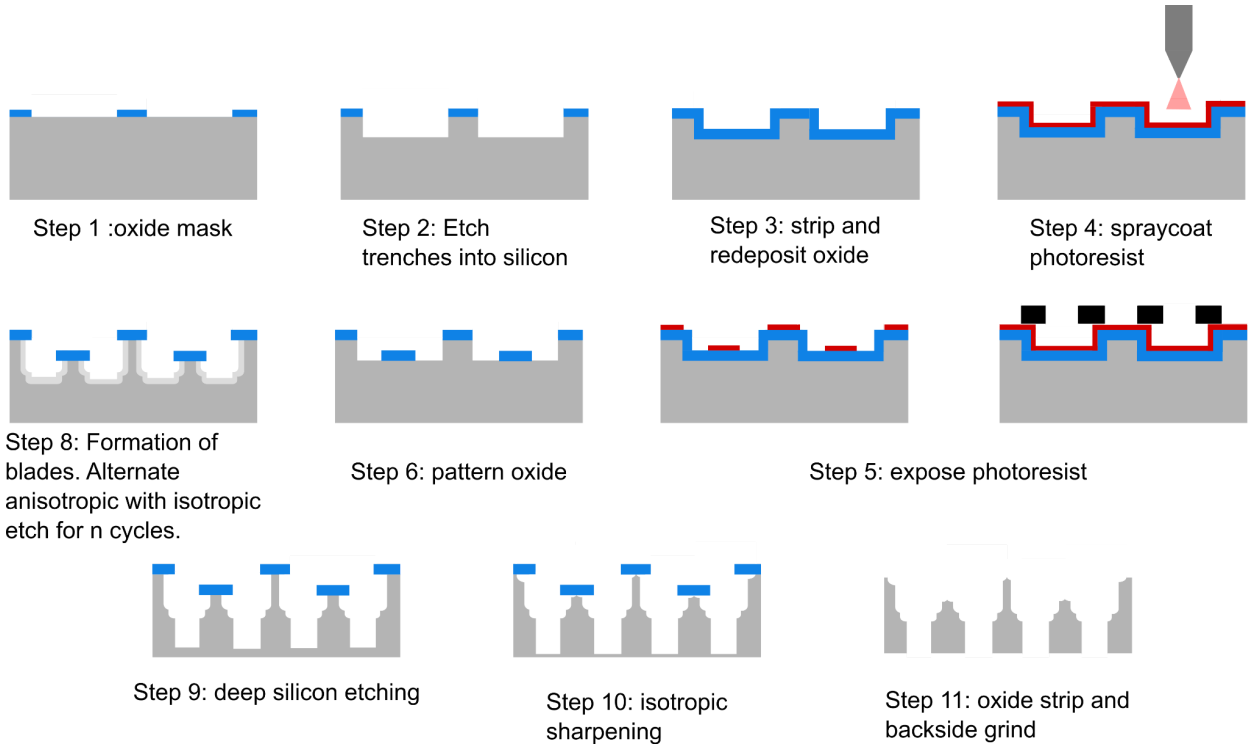


Figure 1: *The general fabrication process for etching a multi-level silicon structure with tapered edges.*

The majority of this project focused on three main areas: 1) designing a two-mask process to create stepped structures, 2) developing and optimizing a negative resist recipe for spray coating, and 3) refining an oxide etching process to effectively clear oxide from the sidewalls. These areas are discussed in more detail in the following sections.

Mask Design and Etch Simulations

Throughout the quarter, we encountered challenges with downstream processes, including photoresist development, sidewall oxide etching, and silicon etching. These issues are discussed in more detail in the following sections. In Figure 2, we highlight the design changes made to the mask. The first layer (in red) consists of an array of large squares. We initially etched a straight trench approximately 25 µm deep using the Bosch process on the deep silicon etcher. The second layer (in green) features smaller squares inset within the larger pattern.

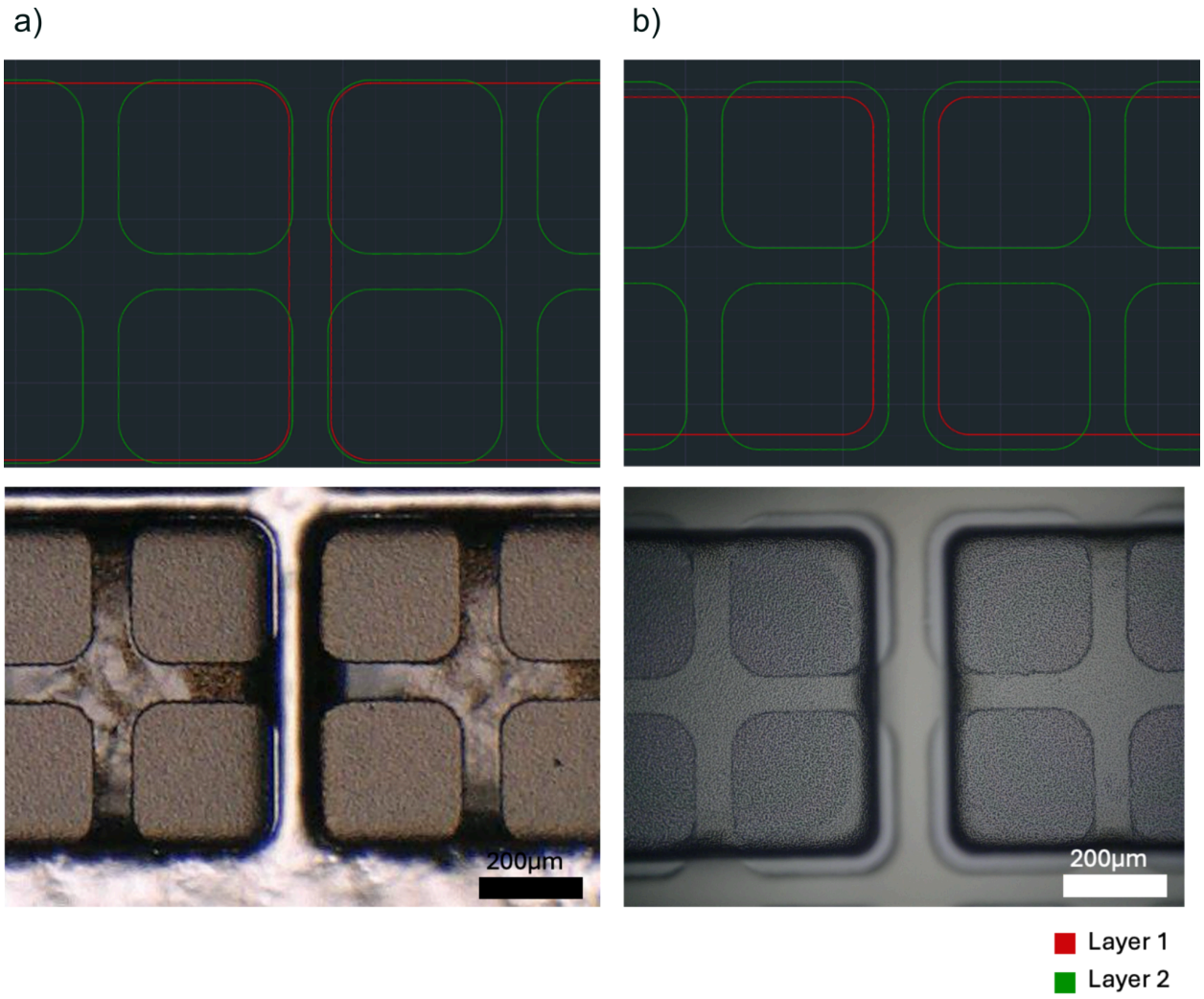


Figure 2: *Two-layer design. (a) Version 1 of the two-layer mask design, with a minimal gap between the first and second layers, primarily intended for alignment tolerances. (b) Version 2 of the two-layer mask design, featuring a wider gap between the layers to improve photoresist development and enhance oxide and silicon etching. The bottom images show the structures after development.*

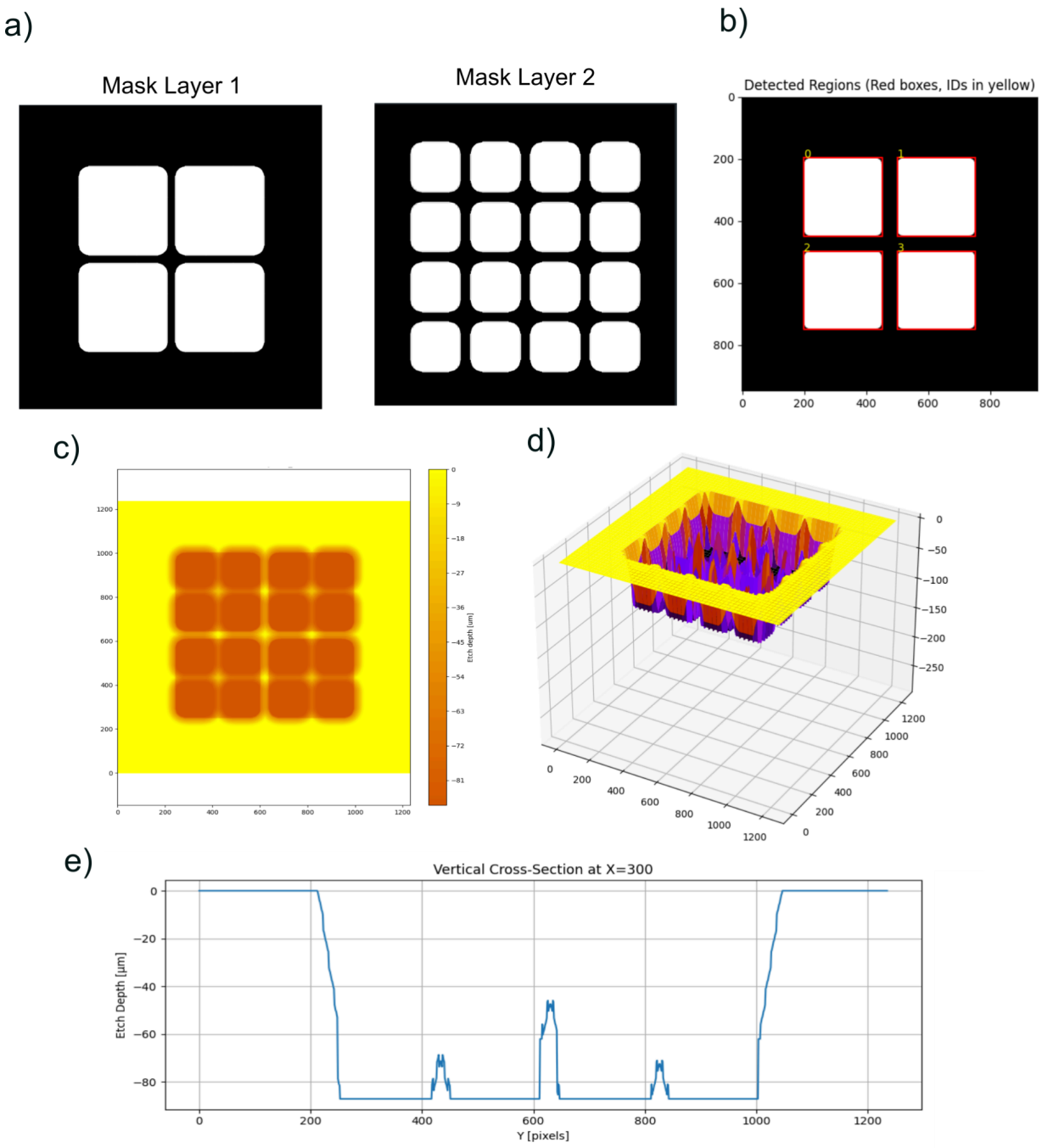


***Figure 3**: **Simulation of etching profile**. (a) Two-layer mask input into the simulation. (b) Example of edge detection functionality, which converts pixels from the mask (with a known length) to microns. (c) Contour map of the final etch depth. (d) 3D representation of the final etch depth. (e) Example of a cross-section showing the two tiers.*

To visualize the etching profile before committing to the full fabrication process, we developed a Python script to model the etch recipe for a double-layer mask on the PT-DSE. This script was based on the model developed in previous work [1], with added functionality. First, the model

automatically converts pixels into lengths based on a feature from the input mask. Second, we included the option to add a second mask layer, enabling simulation of the two-mask process. Additionally, we developed a separate script to visualize both the x and y cross sections at any point in the simulation. While the script still requires refinement to more accurately reflect the etching profile from the PT-DSE, it proved to be sufficient for providing a rough estimate of the etching profile.

Spray Coating

Our design incorporates two patterned layers of photoresist. The first layer is patterned on a flat wafer and can be processed using conventional spin coating. However, the second layer must be conformal over a patterned wafer with >25 μm trenches across the surface. Conventional spin coating struggles with wafers having varying topographies, as it is difficult to achieve consistent layer thickness across the entire wafer. Spray coating addresses this issue by dispensing small droplets across the wafer, where they stick upon landing. Conformal coatings on irregular surfaces depend on factors such as evaporation rate, dispense rate, and the number of passes.

While positive resists are most commonly used at the SNF, we opted for a negative resist to ensure proper removal of sidewall photoresist. Using a positive resist would require exposure on the side walls, which is difficult with the equipment available in the SNF lab. By using a negative resist, we can expose the features directly and develop away the sidewall photoresist.

As part of our work, we tested and characterized various resist recipes. Spray coating requires a photoresist with a viscosity of less than 20 cSt [4]. Therefore, we needed to dilute our negative resist with compatible solvents. We chose AZnLOF 2020 negative resist as the base and varied the concentrations of methyl ethyl ketone (MEK) and PGMEA. Since MEK is a faster-evaporating solvent, higher concentrations tend to produce more conformal coatings, but at the expense of surface smoothness. However, excessive solvent evaporation can increase resist viscosity, preventing the formation of a closed surface. Additionally, as the concentration of photoresist increases, droplet size also increases, which affects both film thickness and conformality.

With these factors in mind, we conducted two experiments to identify a suitable resist recipe for our process. For our application, we need a photoresist thickness greater than 3 μm to properly mask the oxide hard mask, which exceeds 3 μm in thickness. The first experiment varied the concentrations of photoresist, MEK, and PGMEA to find the most promising recipe that would yield a conformal coating. We kept the parameters constant at four passes and a dispense rate of 9 μL/s. The second experiment involved adjusting the spray coating parameters using the resist recipe we identified as most suitable for our purposes. Table 1 below lists the experimental test conditions.

Table 1: Spray coater recipes with varying concentrations of resist and solvents

Recipe	solids percent	resist wt%	MEK %	PGMEA %
1	2.50	10.00	63.00	27.00
2	2.50	10.00	45.00	45.00
3	4.00	16.00	58.80	25.20
4	4.00	16.00	42.00	42.00
5	6.00	24.00	53.20	22.80
6	6.00	24.00	38.00	38.00

Exposure of Layer 2

Many users in the SNF prefer to use a maskless lithography tool, such as the Heidelberg direct write tools. While this would be more convenient for us, our topologies of varying heights of greater than 25 μm put the tool at risk of crashing into the substrate. Therefore, for our second layer, we used the Karl Suss contact aligner. Since our features were large, we were able to order a transparency mask that worked sufficiently with our process. To test the exposure energy, we sectioned off four different parts of a flat wafer using aluminum foil and varied the exposure time. A detailed procedure can be found in the appendix.

Table 2: Exposure energies tested

Area on wafer	Time	Energy (mJ/cm^2)
right top	6sec	90
left top	8 sec	120
left bottom	9.3s	139.5
right bottom	11s	165

a) b)

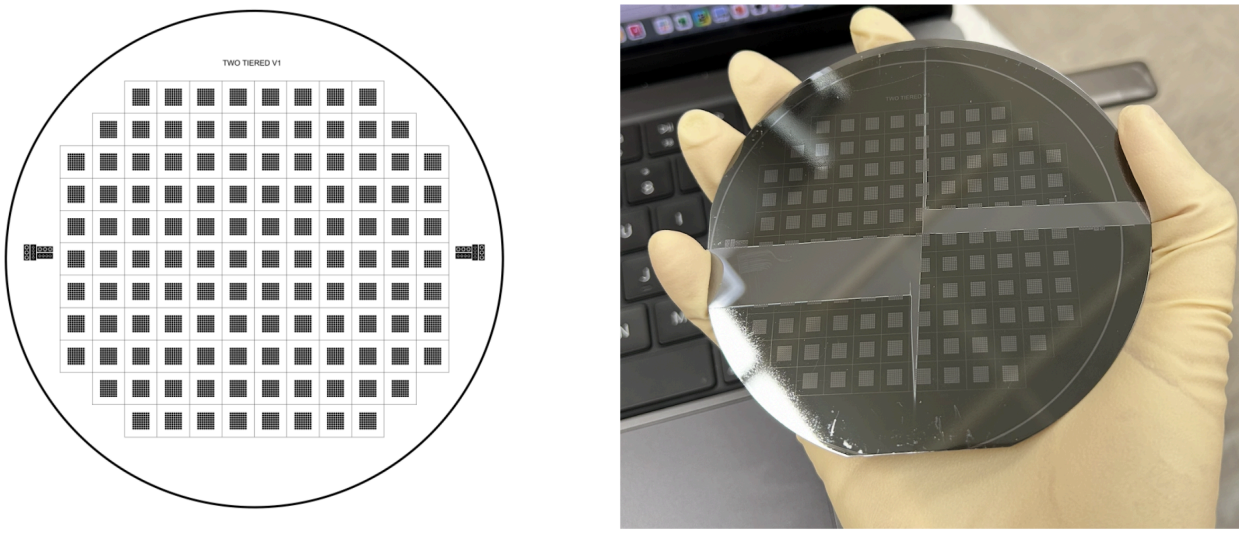


Figure 4: Transparency mask design (a) and dosage test (b).

Oxide Etching

For our process, we required an oxide hard mask for the second layer of etching. Oxide deposition using PECVD is a conformal process, meaning the oxide is deposited on all surfaces, including the sidewalls of the etched features. To successfully fabricate the tapered edges, it was essential that the sidewall oxide be removed, as it would mask the edges and interfere with the etching process.

For the first layer, we used the PlasmaTherm Versaline LL ICP Dielectric Etcher (PT-Ox) for oxide dry etching. While this method effectively removes oxide from the tops and bottoms of the trenches, dry etching is highly directional, making it difficult to etch the oxide on the sidewalls. As a result, we initially explored wet etching, which is isotropic and theoretically capable of etching both the bottom surfaces and sidewalls of the trenches. However, due to wetting issues, the etch rate of the wet etchant (6:1 BOE) was not uniform across the wafer. This caused overetching in some areas and insufficient etching in others. Specifically, the oxide on the bottom surfaces of the trenches was not clearing, while the sidewall oxide was overetched, leading to uneven silicon etching in the subsequent step.

To address this, we developed a hybrid dry/wet etching process. First, we used dry etching to clear the oxide from the bottoms of the trenches, followed by a short, 3-minute wet etching step to remove the oxide from the sidewalls. This approach ensured both uniform oxide removal and preserved the integrity of the tapered edges.

Pushing Mold

Given the nature of the microstructure fabrication process, a molding approach is a natural solution for creating a complementary polymer structure. This molded polymer can serve as both a stop for the blade and a buffer layer to help uniformly distribute mechanical stress. The molding process is performed prior to backgrinding shown in Figure 5. First, a 3 µm-thick sacrificial layer is deposited to provide separation and flexibility during demolding. PDMS is then poured into the microstructure and cured at an elevated temperature to solidify the mold. After curing, the sacrificial layer is etched or dissolved away, releasing the PDMS mold from the microstructure. To use the mold, tissue is placed on top of it, and the microstructure is reinserted into the mold to ensure alignment and mechanical support during subsequent processing.

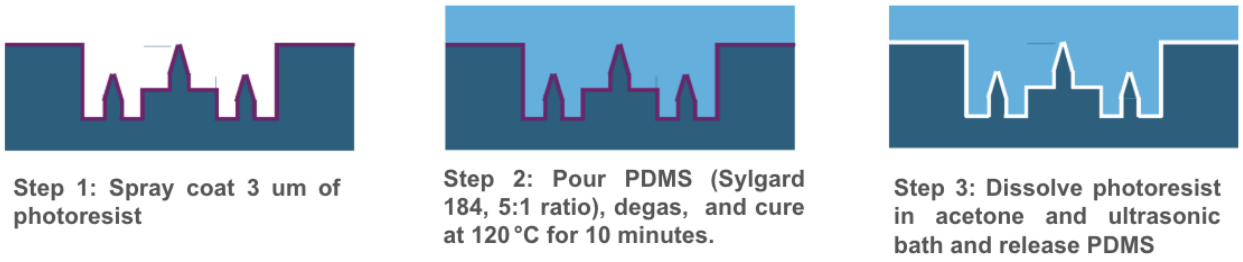


Figure 5: Fabrication process for the molding process

A 5:1 base-to-curing-agent ratio of PDMS is chosen for the mold material to achieve an optimal balance between softness and stiffness. The softness ensures conformity and compliance with the microstructure, while the stiffness provides sufficient mechanical integrity to prevent bending or deformation during use. Spray-coated photoresist is used due to its excellent conformality and controllable thickness. Moreover, the existing recipe for fabricating two-tiered structures can be conveniently adapted for spray coating the photoresist, streamlining the overall process.

Results and Discussion

Photoresist Spray Coat and Exposure

We used scanning electron microscopy (SEM) to characterize the morphology and coverage uniformity of the spray-coated photoresist layer. For this test, a 50 µm-deep trench was first etched using the Bosch process, followed by spray coating of positive photoresist [resist name] with four passes. The SEM image (Figure 6) shows that the resist coverage is non-uniform across the topography. On the top surface (island), the resist layer appears very thin nearly conformal to the substrate. However, it is not clearly visible in the SEM image, likely due to cleaving artifacts or local charging effects.While on the trench sidewalls, the resist is significantly thicker, exceeding 15 µm in some areas. In the center bottom of the trench, the resist thickness tapers to approximately 3 µm. This uneven coverage suggests that using a positive resist is not suitable for such high-aspect-ratio structures. The excessive resist on the sidewalls, combined with the directional nature of exposure, prevents full exposure of the sidewall resist, as the thick

accumulation and vertical incidence of light hinder pattern transfer. To address this, a negative resist should be considered, as it allows for more effective sidewall patterning under these conditions.

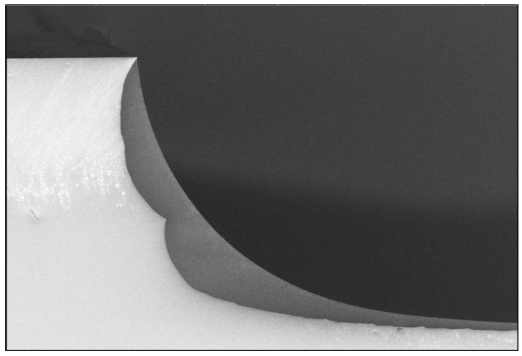


Figure 6: SEM image of spray coated positive resist of 4 passes

SEM was then used to characterize the coating profiles of negative photoresist applied by spray coating. Both 4-pass and 8-pass conditions were examined using a straight trench with a depth of 25 µm. As shown in Figure 7, the 8-pass coating resulted in trenches nearly filled with photoresist, with thickness reaching approximately 24 µm near the sidewalls and around 14 µm at the trench center. Only a very thin resist layer was present on the top surface (island). The non-uniform distribution of photoresist thickness continues to hinder consistent exposure across the surface. In comparison, the 4-pass condition (Figure 8) produced a more uniform profile. The resist on the sidewalls was significantly thinner—approximately 50% less than that in the 8-pass case—and the center of the trench showed a reduced thickness of about 4 µm. These observations suggest that fewer spray passes can reduce sidewall accumulation and improve coating uniformity for high-aspect-ratio features.

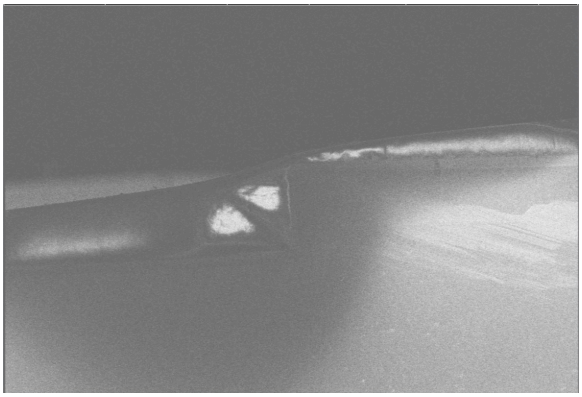


Figure 7: SEM image of 8 passes spray coated negative resist

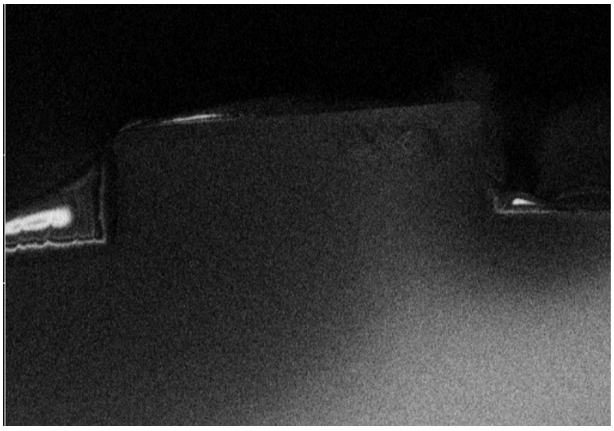


Figure 8: SEM image of 4 passes spray coated negative resist

After characterizing the photoresist thickness using SEM, we selected a photoresist recipe with a lower resist concentration, while keeping the concentrations of MEK and PGMEA the same (recipe 2). Both recipe 1 and recipe 2 produced thicknesses within the desired range, but recipe 1 resulted in excessive pinholes, leading to inconsistent photoresist coverage. In contrast, recipe 2 provided a mostly closed layer with fewer imperfections. To further improve coverage, we modified the recipe by adding two mist coat layers with a lower dispense rate to fill any remaining holes.

The top left image in Figure 9 shows the photoresist spray-coated on a flat wafer with four spray-coat passes. While the wafer was mostly covered, some areas, as indicated in the image, failed to coalesce. After adding the mist coat passes, the top right image shows a much smoother and more uniform layer.

After spray coating, we exposed the wafer at an exposure energy of 180 mJ/cm². Although this was higher than the energies tested, we chose it to ensure adequate exposure in areas where the resist was slightly thicker. Since the mask was in direct contact with the wafer, no visible overexposure signs were observed. Additionally, our features were large enough that overexposure was not a concern. The bottom images in Figure 9 show the resulting pattern after exposure.

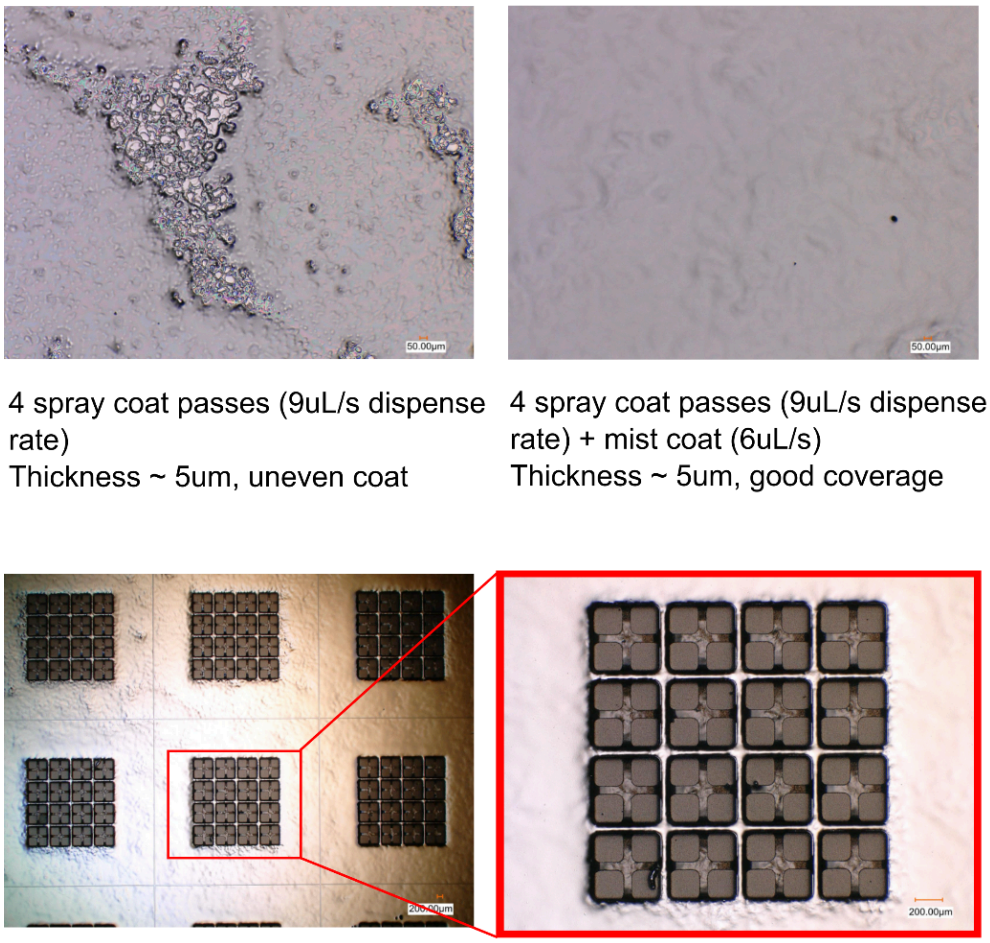


***Figure 9**: **Photoresist spray coating and exposure.** The top left figure shows an uneven coating full of pinholes after 4 passes at 9 µL/s. The top right figure shows a smooth coating with an added mist coat at a lower dispense rate (6 µL/s). The bottom figures show the resulting pattern once the photoresist was exposed. The smaller squares are inset 25µm below the top of the silicone surface.*

Oxide Etching

The oxide etching process for our structure was delicate, as we needed to remove all the oxide from the bottom and sidewalls of the trenches without overetching, which could compromise the top tier of our silicon structure. We initially attempted wet etching using 6:1 BOE. However, after checking at intervals of 2-5 minutes, we observed that some areas, such as the top beams, were overetched, while the bottoms of the trenches were not fully etched. **Figure 10a** shows the pattern after photoresist development, and **Figure 10b** shows the oxide etch after wet etching. The darker areas in the small squares indicate oxide that was not fully etched, while the top beams were overetched in some regions. The uneven etching was likely due to wetting issues.

To resolve this, we first performed a dry etch to clear the oxide from the bottom layer of the trenches, ensuring that the beams were not overetched. Once the bottom oxide was cleared, we followed with a short, 3-minute wet etch in 6:1 BOE, which was sufficient to etch the sidewall oxide. **Figure 10c** shows the resulting structure after the hybrid etch, and **Figure 10d** provides a close-up view of a small wet etch undercut, confirming the removal of oxide from the sidewalls.

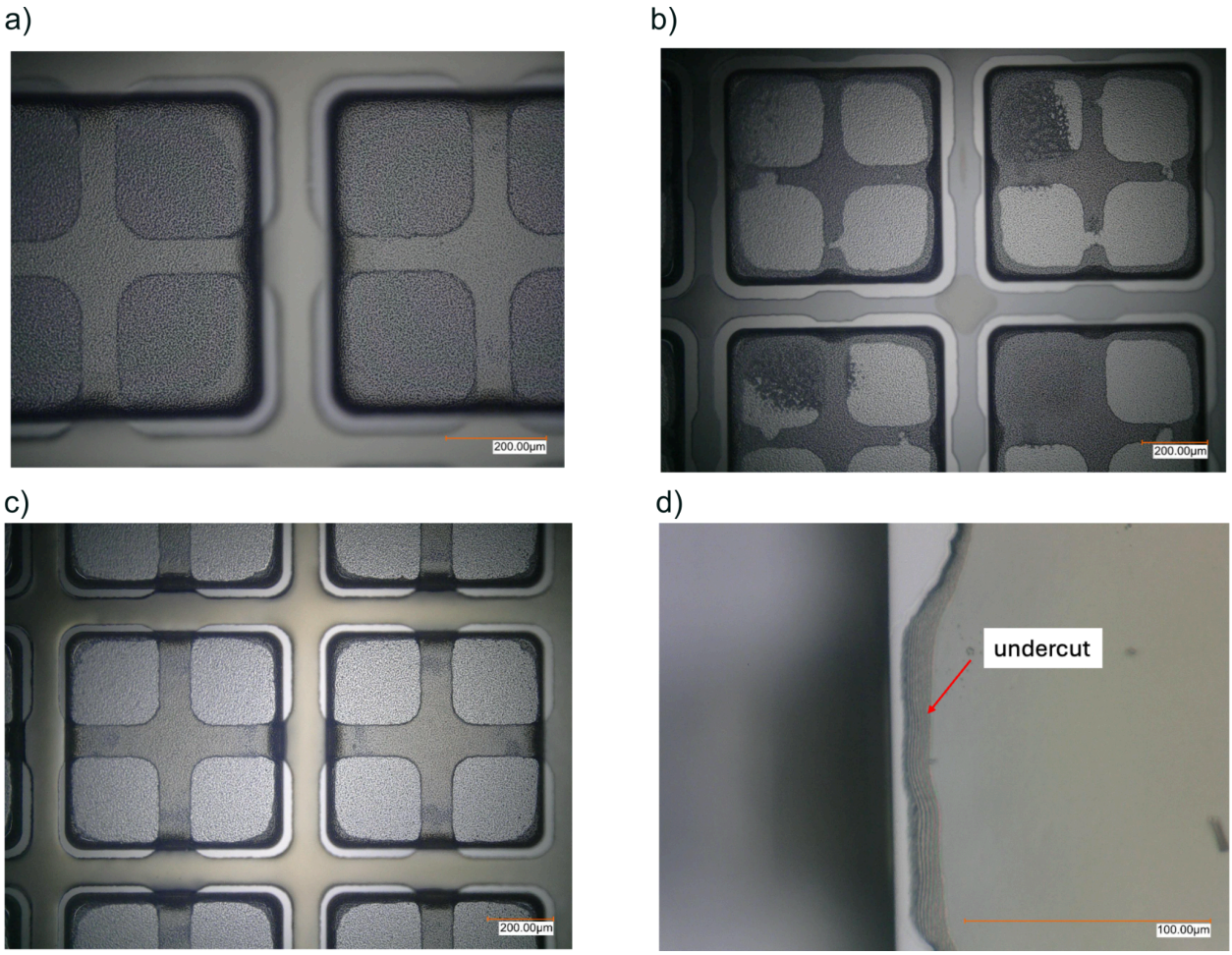


Figure 10: Oxide etching. *a) Pattern before oxide etching. b) Wet etch only–bottom areas underetched, top beams overetched (>3um undercut). c) After dry + wet etching. d) Close-up of wet etch undercut showing sufficient sidewall oxide removal.*

Silicon Etching

The quality of the oxide mask and etching process directly influenced the final geometry of the structure. Figure 11a demonstrates the effect of incomplete sidewall oxide removal. The brighter areas indicate unetched silicon. In this case, the oxide on the left sidewall of the beam was completely etched away, while the oxide on the right side remained, masking the silicon etching. Figure 11b shows the desired outcome, with uniformly etched silicon where the sidewall oxide has been fully removed from all parts of the structure.

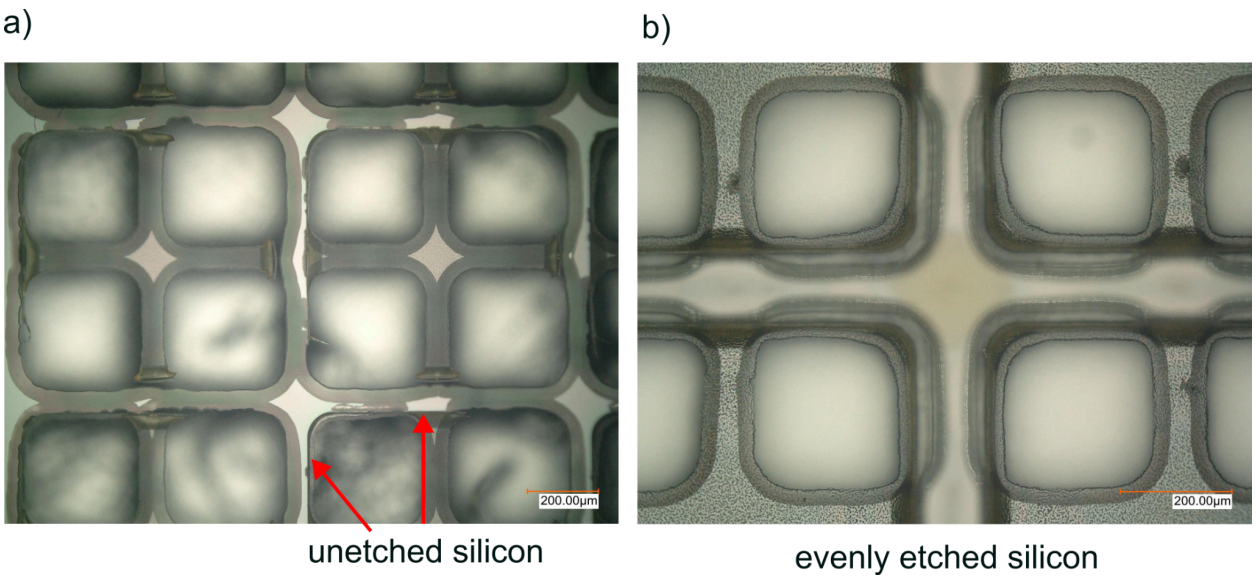


Figure 11: Etched silicon with a) incomplete sidewall oxide removal and b) complete sidewall oxide removal.

We etched both version 1 and version 2 of the multi-level design (see Figure 2 for designs). In version 1, we did not achieve a multi-tiered structure. This was because the tiered design depends on the point where the silicon etch fronts beneath the beams meet. The isotropic etch corners determine this point of intersection. In version 1, the isotropic etch front occurs at the same corner for both the top and bottom tiers. As a result, even if the structure starts at a higher level, the features are "pinched" off at the same plane as the bottom tier. This is shown in Figure 12.

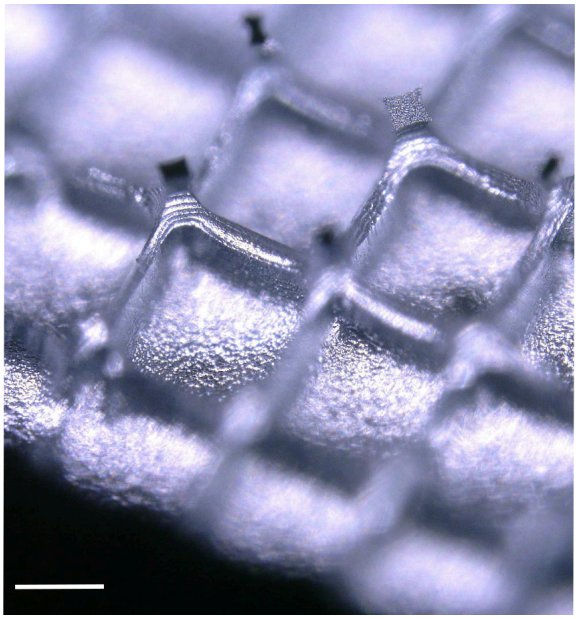


Figure 12: Etched silicon structure. *In the version 1 design, no noticeable height difference is observed between the top and bottom tiers. Scale bar: 200µm*

In version 2, we added a larger beam in the first layer. The mask in layer 2 is smaller than the beam width, creating space for the isotropic etch front to begin at a higher plane than the bottom tiers. This allows the silicon etch fronts to meet above the etch fronts of the bottom tier. This design change successfully resulted in multi-tiered structures. The resulting height difference is shown in Figure 13.

One issue encountered was that the photoresist at the edges and corners was not fully developed, causing the oxide mask in these areas to remain intact. This effectively acted as another beam at the same height as the lower structure. As a result, smaller features at the same plane as the lower structure were observed beneath the taller structure, which is clearly visible in the cross-sectional view.

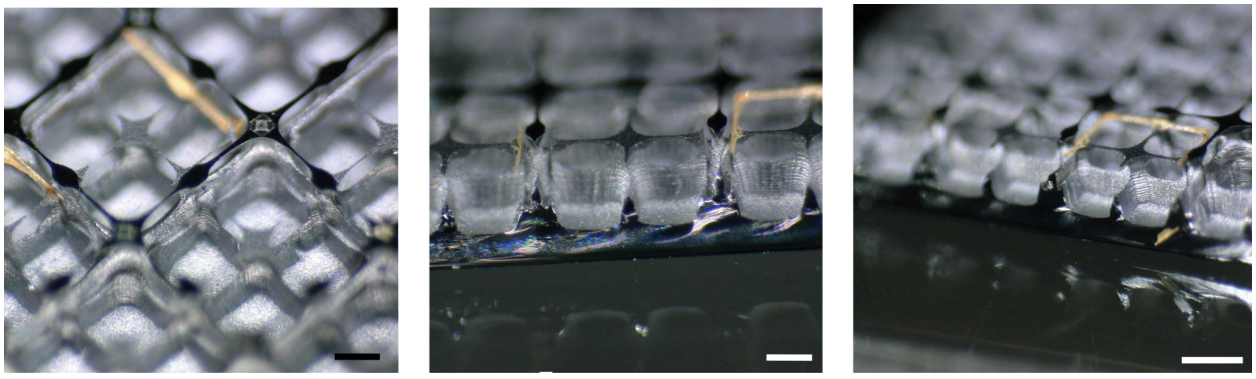


Figure 13: Two-tiered silicon structure. *(Left) Top view of the etched structures. (Middle) Cross-sectional view showing the height differences. (Right) Tilted view of the device cross-section. Scale bar: 200µm*

Pushing Mold Prototype

Wax was initially applied to a 3D-printed resin structure to prototype the demolding process as shown in Figure 14. The wax was first meilted and the 3D-printed resin structure was immersed in it. An air gun was then used to blow out the wax from the inner cavities to prevent blockage. After the wax cooled and solidified, PDMS was poured over the structure, degassed and cured at room temperature for 48 hours. To release the mold, the assembly was gently heated to melt the wax, allowing the PDMS to be demolded cleanly. This process was successful, with the PDMS replicating the expected pattern accurately. The result suggests that the molding approach is viable and compatible with the intended microstructure fabrication process.

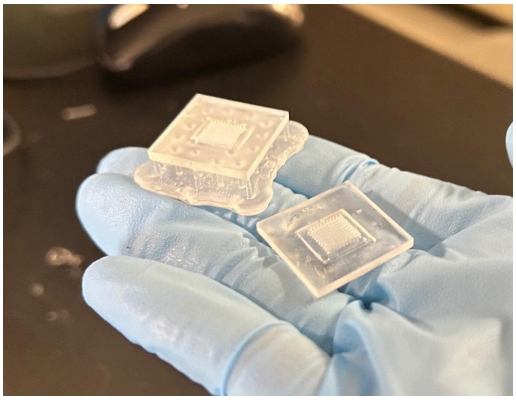


Figure 14. *3D-printed resin structure (left) and the PDMS mold (right) using wax as sacrificial layer*

To further investigate the demolding process, silicon trenches were used to evaluate mold release on a silicon wafer. Initially, silane was applied to the wafer surface, which enabled successful demolding. Spray coated negative photoresist was also tested, and the mold separated easily in that case as well. However, a key challenge arises due to PDMS shrinkage. Approximately 1.5% shrinkage is observed when PDMS is cured at 120 °C for 10 minutes. This shrinkage hinders the ability to reinsert the PDMS mold back into the original microstructure with proper alignment and fit.

To address this issue, it is necessary to carefully characterize the shrinkage behavior of PDMS during curing. Based on the measured shrinkage data. A slightly oversized microstructure can be fabricated to compensate for the dimensional reduction. The resulting PDMS mold after shrinkage would then match the intended dimensions of the original structure and fit upon reinsertion.

Conclusions and Future Work

This work presents the fabrication of a multi-level silicon structure using a double-masking process. Building upon the µDicer technology, we developed an initial fabrication process that successfully produced visible step heights. Moving forward, we aim to refine both the spray coating and masking processes. Specifically, we plan to further optimize the spray coating recipe to achieve a more conformal coating, particularly at the edges of the trenches, which will improve photoresist development. Additionally, we intend to test these devices with real tissue samples to assess their performance in practical applications. Lastly, the molding process shows promise as a reusable support strategy and we will be focusing on compensating for PDMS shrinkage through precise dimensional tuning of the micro structure.

Appendix

Budget

A total of $4,304.62 was spent on this project using the class PTA. The majority of the budget (54%) was allocated to tool usage, followed by 36% for tool training. The remaining expenses were spent on supplies, including wafers and masks. A detailed breakdown of the spending is provided in Table 3.

Table 3. Budget of the project.

Item		**Expense**
Training		$1760
Tools	Etching	$1071.67
	Deposition	$447.74
	Lithography	$642.68
	Characterization	$163.47
Supplies		$219.06
Total		$4304.62

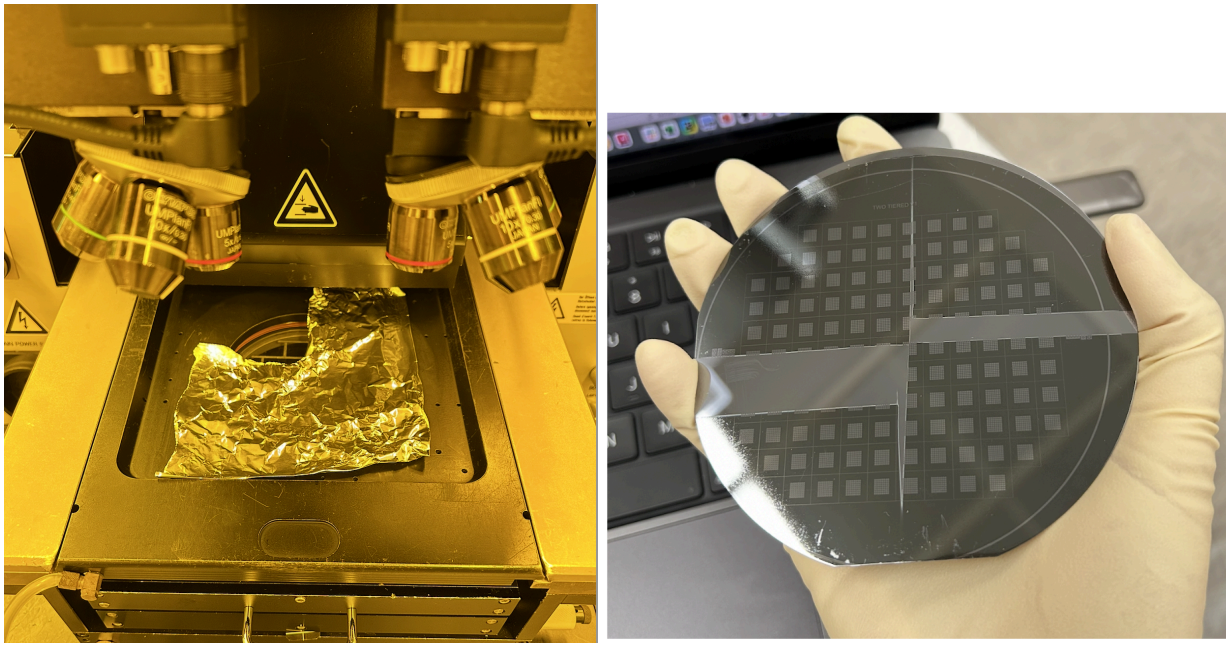
Nuggets

Karl Suss Dosage Test

We used the Karl Suss contact aligner to expose our pattern onto a silicon substrate with irregular topologies. Unlike a direct write tool, such as the Heidelberg, the Karl Suss exposes the entire wafer with the same energy. As it is important to do a dosage test for the resist, we used aluminum foil with a fourth cut out to expose different parts of the wafer at different dosages.

1) Cut a square piece of aluminum foil large enough to cover the mask. Cut one corner of the aluminum foil such that a quarter of the wafer is exposed.
2) Make sure the aluminum foil is flat, as the hood for the Karl Suss comes forward and may move the aluminum foil as it moves.
3) Expose the wafer.
4) Turn the aluminum foil 90 degrees, repeat the process.

Note: this allows you to get 4 different dosages with one wafer. If necessary, you can cut a smaller piece from the aluminum foil to expose smaller sections of the wafer.



Left: Karl Suss contact aligner with aluminum foil covering wafer. Only the top left corner of the wafer will be exposed. Right: 4 in wafer exposed with different dosages.

Hybrid Dry/Wet Oxide Etch

Note: This nugget is part of a longer standard operating procedure (SOP) for the ENGR 241 project "Multilevel Silicon Structure and Fabricated Pushing Mold for Sample Transfer."

When working with oxide removal, it's important to note that while oxide etching on flat wafers is isotropic and uniform, irregular topologies can make controlled etching more difficult. Variations in surface geometry can cause inconsistent etch rates, leading to issues like overetching or underetching.

Step 1: Dry etching for Bottom Oxide Removal

To start, use the PlasmaTherm Versaline LL ICP Dielectric Etcher (PT-Ox) for dry etching the oxide on the bottom of the trenches. Use the standard oxide etch recipe (OX-ER_TEST) to etch the bottom oxide all the way through.

- Important: After the dry etching process, check the oxide thickness using the Nanospec2. If the reading shows "less than 100Å," this confirms that the oxide has been fully removed from the bottom of the trenches.
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Step 2: Wet Etching for Sidewall Oxide Removal

Next, prepare for the wet etching step to clear the oxide from the sidewalls. Use the wbflexcorr benches for this process. Prepare a 6:1 BOE (Buffered Oxide Etch) solution and perform a short, 3-minute wet etch.

- Tip: Gently swirl the BOE container for the first 30 seconds to ensure even wetting. Be careful not to spill the solution during this time.

After the wet etching is complete, rinse the wafer thoroughly in 3 DI water baths and then dry it carefully.

Step 3: Inspect the Etching Process

Use the Keyence Digital Microscope VHX-6000 to verify that the sidewalls have been properly etched. Zoom in to the highest magnification at the top of the pattern and check for any undercutting under the photoresist mask. Note: Ensure that there is no more than 4 μm of undercutting, as excessive undercutting could affect the quality of the structure.

The two-step approach—starting with dry etching for the bottom oxide and following with a short wet etch for the sidewalls—ensures that oxide removal is both efficient and controlled. Dry etching works well for the trench bottoms, while wet etching ensures the sidewalls are uniformly etched without overetching.

Bibliography

[1] B. L. LeSavage, R. A. Suhar, N. Broguiere, M. P. Lutolf, and S. C. Heilshorn, “Next-generation cancer organoids,” *Nat. Mater.*, vol. 21, no. 2, pp. 143–159, Feb. 2022, doi: 10.1038/s41563-021-01057-5.

[2] S. C. Cordts, N. Castaño, S. Koppaka, and S. K. Y. Tang, “Fabrication of a silicon μ Dicer for uniform microdissection of tissue samples,” *Applied Physics Letters*, vol. 119, no. 1, p. 011904, Jul. 2021, doi: 10.1063/5.0053792.

[3] S. C. Cordts, K. Yuki, M. F. Henao Echeverri, B. Narasimhan, C. J. Kuo, and S. K. Y. Tang, “Microdissection tools to generate organoids for modeling the tumor immune microenvironment,” *Microsyst Nanoeng*, vol. 10, no. 1, p. 126, Sep. 2024, doi: 10.1038/s41378-024-00756-8.

[4] N. P. Pham, J. N. Burghartz, and P. M. Sarro, “Spray coating of photoresist for pattern transfer on high topography surfaces,” *J. Micromech. Microeng.*, vol. 15, no. 4, pp. 691–697, Apr. 2005, doi: 10.1088/0960-1317/15/4/003.