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# 3-Dimensional Capacitor Structures for Heterogenous Integration

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## Abstract

We develop a process for fabricating a 3D lateral capacitor that exploits a recently discovered large permittivity enhancement effect at material interfaces, targeting improvements in energy storage applications. By focusing on the development of specialized etch processes for titanium nitride (TiN) and hafnium dioxide ( $HfO_2$ ), as well as a liftoff process for TiN, the project seeks to provide valuable techniques and insights for the Stanford Nanofabrication Facility (SNF) users. These advancements will facilitate the fabrication of novel capacitor structures compatible with complementary metal-oxide-semiconductor (CMOS) devices. The outcomes of this project promise to enhance energy storage capabilities and contribute to the progress of semiconductor technology, offering substantial benefits to both academic research and industrial applications.

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# 1 Introduction

## 1.1 Motivation

The ever-increasing demand for efficient energy storage solutions in modern electronics has driven significant advancements in capacitor technology. Traditional capacitors, while effective, face limitations in terms of energy density and miniaturization, which are critical for the ongoing development of compact and high-performance electronic devices. In response to these challenges, recent discoveries have highlighted the potential of large permittivity enhancement effects at material interfaces, presenting new opportunities for capacitor design.

The primary goal of this project is to harness these advancements by developing a process for fabricating a 3D lateral capacitor. This novel capacitor design aims to leverage the recently discovered large permittivity enhancement effect at interfaces, thereby significantly improving energy storage capabilities. The focus on a 3D lateral structure not only aims to maximize the permittivity benefits but also to integrate seamlessly with current and future semiconductor technologies.

## 1.2 Benefits to the SNF Community

In addition to advancing capacitor technology, this project offers substantial benefits to the users of the Stanford Nanofabrication Facility (SNF). The development of specialized etch processes for titanium nitride (TiN) and hafnium dioxide (HfO<sub>2</sub>), along with a liftoff process for TiN, will enhance the facility's capabilities and serve as valuable resources for a wide range of research and development activities. Furthermore, the knowledge gained from fabricating these novel capacitor structures will provide critical insights for the integration of these components into complementary metal-oxide-semiconductor (CMOS) devices, paving the way for more efficient and compact electronic systems.

Through these efforts, the project not only addresses immediate technical challenges in capacitor fabrication but also contributes to the broader field of energy storage and semiconductor device engineering. By developing innovative processes and expanding the technological toolkit available at SNF, this work stands to significantly impact both academic research and industrial applications.

## 2 Related work

The study of interfacial permittivity in heterogeneous dielectric bi-layers has garnered significant attention in recent years due to its potential implications for energy storage capacitive devices. Mousavi Karimi and Davis (1) have been at the forefront of this research, highlighting the anomalous interfacial polarizability component of common dielectrics, such as SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, and Al<sub>2</sub>O<sub>3</sub>, which has not been extensively explored. Their work emphasizes the importance of the tangential interfacial properties at dielectric interfaces, particularly in the context of solid-state capacitors with higher energy densities. In the study, Mousavi Karimi and Davis extracted interfacial permittivity values that shed light on the anomalous capacitance behavior observed in devices with heterogeneous interfaces of Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub>, or Al<sub>2</sub>O<sub>3</sub>/Si<sub>3</sub>N<sub>4</sub>. The extracted permittivity values for these structures provided insights into the average permittivities within 1-nm thick volumes at the interfaces, revealing unexpected values that deviated from conventional expectations. Their investigation delved into the anisotropic permittivity behavior at the interfaces of heterogeneous dielectric bi-layers, particularly at low frequencies. Their research highlighted the accentuation of the parallel electric field component near vacancies at the interface of dielectric layers, suggesting potential anomalous tangential interfacial properties and underscoring the complex nature of interfacial permittivity in such structures. Using an interdigitated electrode (IDE) test structures, they measured the impact of additional polarizability tensor values in the plane of the interfaces. This approach provided valuable insights into the interfacial polarizability of heterogeneous dielectric bi-layers, offering new perspectives on the behavior of these interfaces under different electric field excitations.

In the field of microcapacitor research, significant strides have been made towards enhancing energy and power density through the exploration of ferroic order superlattices. The study by Cheema and Salahuddin (2) delves into the development of giant energy microcapacitors, shedding light on the potential of utilizing advanced materials and structures to achieve superior performance metrics. By leveraging the HfO<sub>2</sub>-ZrO<sub>2</sub> system within 3D Si capacitors, researchers have been able to push the boundaries of energy storage capabilities, paving the way for innovative solutions in the field. Moreover, the work presented by Cheema and Salahuddin showcases a remarkable achievement in volumetric energy density, setting a new benchmark for BEOL-compatible dielectrics. The incorporation of a superlattice approach has proven to be instrumental in enhancing energy storage properties, offering a promising avenue for further advancements in microcapacitor technology. Furthermore, their study highlights the successful demonstration of field-driven negative capacitance behavior in trench capacitors, a significant breakthrough that has led to a substantial enhancement in electrostatic discharge (ESD) performance. By showcasing over 100 times improvement in ESD capabilities, this work underscores the potential of integrating innovative concepts into practical applications, thereby addressing critical challenges in the realm of microcapacitor design and functionality.

Collectively, these findings underscore the importance of investigating interfacial permittivity characteristics in heterogeneous dielectric bi-layers and their potential implications for the development of advanced energy storage capacitive devices.

## 3 Simulation

## 4 Process Development and Experimentation

The detailed process flow that outlines the steps required to fabricate a 3D lateral capacitor with enhanced permittivity at interfaces is shown in Fig. 2, leveraging advanced materials and precise fabrication techniques and is explained in more detail below:

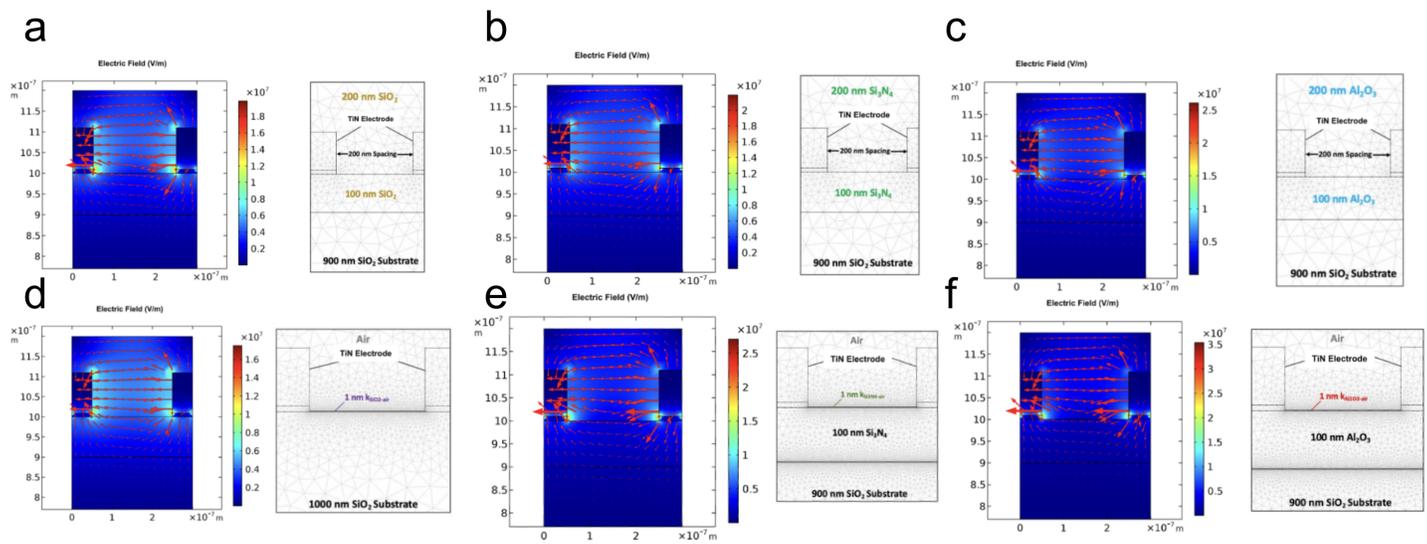


Figure 1: Comsol Multiphysics Simulations of Capacitor.

<b>Structure 1 SiO<sub>2</sub>/Air</b>	Karimi (2022)	1.92 pF	4.16 %
	Simulation	2 pF	
<b>Structure 2 SiO<sub>2</sub>/SiO<sub>2</sub></b>	Karimi (2022)	5.4 pF	53.7%
	Simulation	2.5 pF	
<b>Structure 3 Si<sub>3</sub>N<sub>4</sub> / Air</b>	Karimi (2022)	2.48 pF	20.96%
	Simulation	3 pF	
<b>Structure 4 Si<sub>3</sub>N<sub>4</sub> / Si<sub>3</sub>N<sub>4</sub></b>	Karimi (2022)	6.27 pF	20.25%
	Simulation	5 pF	
<b>Structure 5 Al<sub>2</sub>O<sub>3</sub> / Air</b>	Karimi (2022)	3.27 pF	62.3%
	Simulation	1.23 pF	
<b>Structure 6 Al<sub>2</sub>O<sub>3</sub> / Al<sub>2</sub>O<sub>3</sub></b>	Karimi (2022)	8.98 pF	49.8%
	Simulation	4.5 pF	

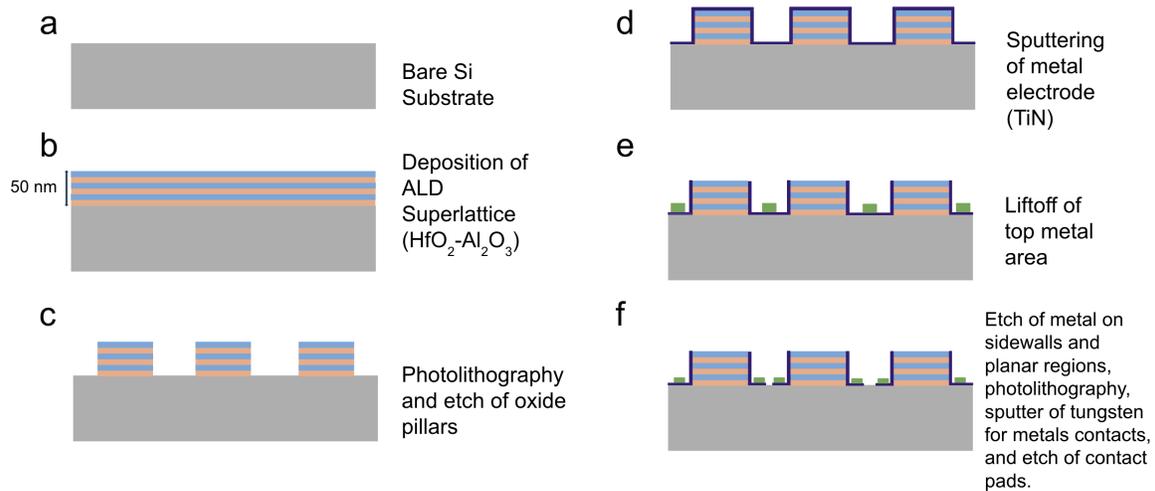


Figure 2: Schematic of the complete process flow proposed to manufacture 3D capacitor-structures.

#### 4.1 Bare Si Substrate from 100 mm Wafer

The process begins with the selection of a bare silicon (Si) substrate sourced from a 100 mm diameter wafer. This substrate serves as the foundational material upon which the entire capacitor structure will be built. Silicon is chosen due to its excellent electrical properties and compatibility with standard semiconductor processing techniques. The wafer is thoroughly cleaned using standard semiconductor cleaning procedures to remove any contaminants or native oxides, ensuring a pristine surface for subsequent deposition steps.

## 4.2 Deposition of ALD HfO<sub>2</sub> Lattice (52.5 nm)

Atomic Layer Deposition (ALD) is employed to deposit a 52.5 nm thick layer of hafnium dioxide (HfO<sub>2</sub>) on the cleaned silicon substrate. ALD is chosen for its precise control over film thickness and uniformity, which is critical for achieving the desired dielectric properties. The HfO<sub>2</sub> layer forms the dielectric material of the capacitor, providing high permittivity and excellent insulating characteristics. The ALD process involves alternating pulses of hafnium precursor and oxygen reactant, allowing for layer-by-layer growth of the HfO<sub>2</sub> film with atomic precision.

## 4.3 Photolithography and Etch of Oxide Pillars to Define Capacitor Structure

Photolithography is utilized to pattern the oxide layer and define the structure of the capacitor. A photoresist (Shipley 3612 1.0 μm) is applied to the HfO<sub>2</sub>-coated substrate, followed by exposure to ultraviolet (UV) light through a photomask that defines the desired capacitor geometry. The mask was designed using the software KLayout as is shown in Fig. 3.

The mask was designed to provide an array of capacitor sizes as show in Fig. 4. These different capacitor sizes allow us to have many capacitors to test and probe for potential size effects. The advantage of photolithography is that a massive number of devices can be fabricated on a single wafer.

After development, the exposed areas of the HfO<sub>2</sub> are removed using a selective etching process, typically involving a dry etch method such as reactive ion etching (RIE). This step creates oxide pillars that will serve as the dielectric regions between the capacitor plates.

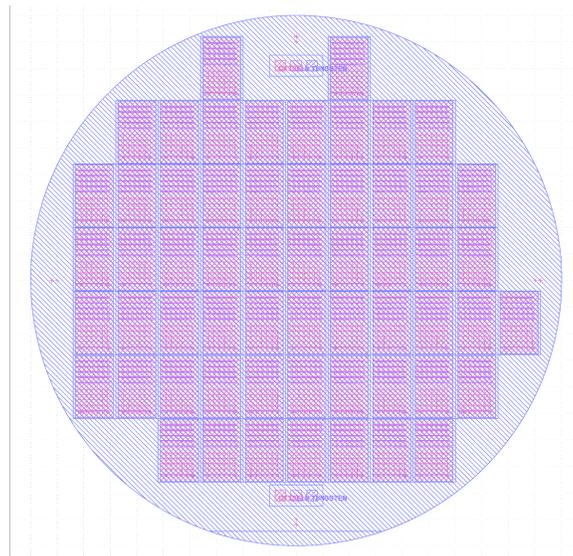


Figure 3: Mask designed using KLayout.

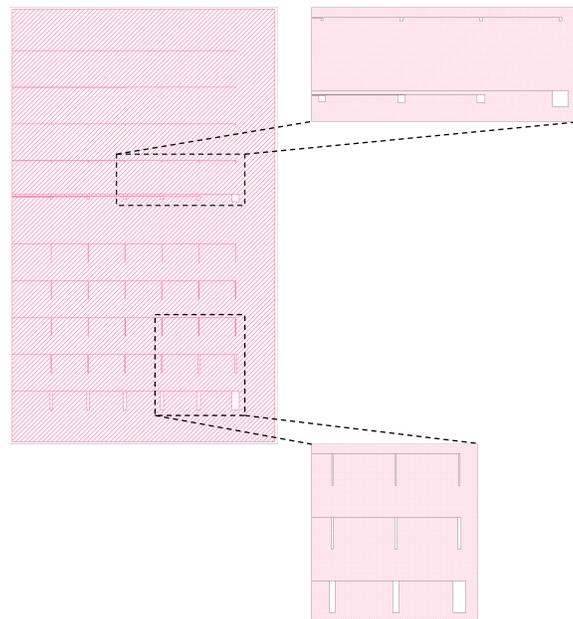


Figure 4: Array of capacitors for testing.

#### 4.4 Sputtering of Metal Electrode (TiN) to Define Parallel Plates

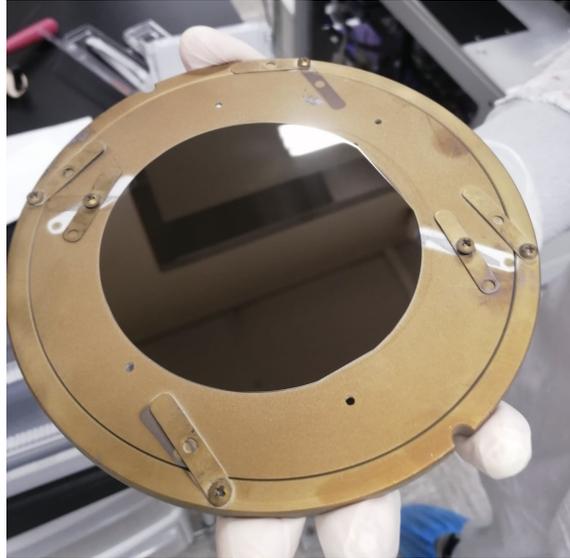


Figure 5: TiN sputtering.

Titanium nitride (TiN) is deposited using a sputtering process to form the metal electrodes of the capacitor. Sputtering is a physical vapor deposition (PVD) technique where TiN is ejected from a target material by high-energy ions and then deposited onto the substrate. TiN is selected for its excellent electrical conductivity and compatibility with high-temperature processes. The sputtered TiN forms a conformal coating over the HfO<sub>2</sub> pillars, creating the parallel plate structure necessary for capacitor functionality. The sputtered wafer is shown in Fig. 5.

#### 4.5 Liftoff of Top Metal Area to Remove the Connection Between Parallel Plates

To isolate the parallel plates and remove any unwanted metal connections, a liftoff process is employed. The TiN that is on the photoresist covered top of the oxide pillars is then removed using acetone as a solvent, leaving behind only the desired electrode regions. To ensure complete liftoff, the wafer was put under sonication for two hours. The liftoff process ensures that the top metal area does not short-circuit the parallel plates, maintaining the integrity of the capacitor structure. The main advantage of the liftoff process in this step is that it removes the potential for overetching the top of the oxide pillar structures. The capacitor structures after liftoff are shown in Fig. 6.

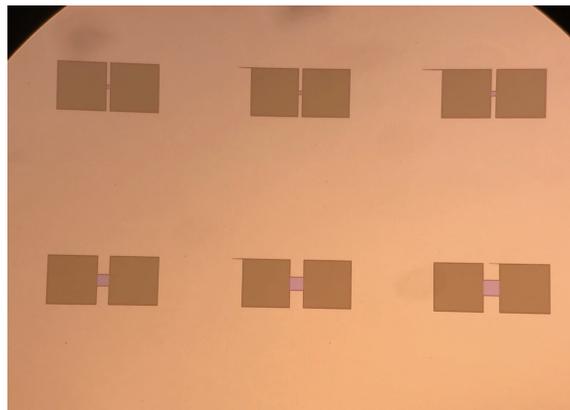


Figure 6: Capacitor structures as observed in optical microscope.

#### 4.6 Etch of Metal on Sidewalls and Planar Regions, Photolithography, Sputter of Tungsten for Metal Contacts, and Etch of Contact Pads

The next step involves further refinement of the metal structures. Photolithography is used to pattern the areas where the TiN metal on the sidewalls and planar regions should be etched away, ensuring that the electrodes are properly defined and isolated. A dry etch process is employed to remove the unwanted TiN.

Subsequently, tungsten (W) is sputtered to form the metal contacts. Tungsten is chosen for its robustness and excellent conductivity. Photolithography is used once more to define the contact pad areas, followed by an etching process to remove excess tungsten and leave behind well-defined contact pads. These contact pads will serve as the electrical connections for integrating the capacitor with external circuitry.

## 5 Conclusion, Discussion and Future Work

In this report, the fabrication process for a 3-dimensional lateral capacitor is detailed. This capacitor structure is designed to utilize an interfacial permittivity effect to store a much larger amount of energy compared to other proposed designs.

Future work will comprise the measurement of these devices to ensure the viability of the fabrication process and their functionality as a microsupercapacitor.

## 6 Acknowledgments

We would like to thank our professors for the course, Prof. Debbie Senesky and Prof. Swaroop Kommera, for their help in conceptualizing the process proposed in this report. We thank our mentors, Don Gardner, Vijay Narasimhan, Michelle Rincon and all other E241 mentors, for their continued help and support throughout the quarter, helping us through the new challenges faced during the development of our process flow. We are also very thankful to all the SNF staff and community who helped us with training and their advice throughout the project.

## 7 Appendices

### 7.1 Budget

We spent a total of \$4509.65 out of a total budget of \$5000.00. The largest expense of this project was the training on the tools, as both of us had to get trained on the SNF equipment for the first time which incurred in significant costs. In terms of the process the most costly part was the ALD step in the Savannah which required 525 cycles in addition to waiting for the equipment to reach the right temperature and vacuum level.

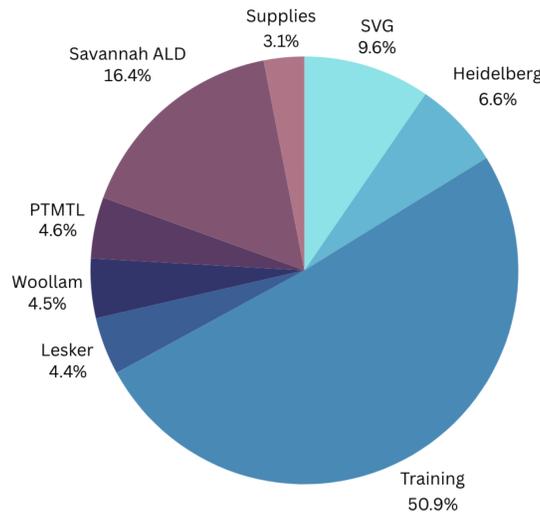


Figure 7: Budget Breakdown for the different tools and items in the projects

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