Gated Hall Bars for Carrier Transport Measurements in Monolayer MoS_2

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1. Introduction

1.1 Motivation

The semiconductor industry continues to push towards smaller and smaller devices while pushing the bounds of what seems possible. As semiconductor devices continue to scale, atomically thin transition metal dichalcogenides (TMDs) such as MoS_2 are promising channel materials. These materials preserve useful electronic properties at thicknesses below 1 nm, breaking the limits set by silicon. However, evaluating carrier transport in monolayer TMDs is difficult. Field-effect and effective mobility measurements require assumptions about capacitance, carrier density, contact resistance, and device geometry, which can make the extracted mobility inaccurate and inconsistent across devices [1]. Hall measurements can directly determine sheet carrier density and Hall mobility, but in monolayer TMDs the true Hall voltage is often very small and can be obscured by misalignment voltage, thermomagnetic effects, offsets, drift, geometry-induced voltage mixing, and device damage [1-3]. This project's goal is to develop gated Hall bar devices and a measurement workflow for carrier transport characterization in monolayer MoS_2.

1.2 Objectives

The goals of this project were to fabricate local-back-gated (LBG) monolayer MoS_2 Hall bar structures, characterize their geometry and electrical behavior, and evaluate whether reliable Hall mobility measurements could be obtained. Process development included a multi-step fabrication flow with alignment markers, local gates, atomic layer deposition (ALD) of HfO_2 for the LBG dielectric, via etching, MoS_2 channel definition, fine contacts, and encapsulation. Characterization included finite-element geometry-error simulations prior to fabrication, optical imaging, atomic force microscopy (AFM) validation of device dimensions, transfer measurements, transfer length method (TLM) device contact analysis, bias-stress stability checks, and Hall measurements under applied magnetic field.

1.3 Benefit to the Stanford Nanofabrication Facility (SNF) or nano@stanford Community

This work provides future SNF and nano@stanford users with a documented process flow for fabricating gated two-dimensional (2D) Hall bar devices and a practical framework for interpreting Hall data in monolayer TMDs. The project clarified common issues including low Hall signal, contact resistance, electro-static discharge (ESD) sensitivity, current-induced damage, geometry error, and the need for field/current reversal protocols.

The statement of process (SOP) and Nano Nuggets will help future users reuse the fabrication sequence, anticipate failure modes (particularly those that are geometry-induced), select safer measurement conditions, and critically compare field-effect and Hall mobility results. Additionally the process for using gate bias and taking AC measurements on the Lakeshore will be outlined.

2. Fabrication Process Development

2.1 Overview of Fab Flow

The final fabrication process produced LBG Hall bar devices for carrier transport measurements in monolayer MoS_2. The completed process flow is shown below in Fig. 1, and includes photolithography for alignment markers, contacts, and back gates; ALD gate dielectric deposition; via etching; fine alignment marker deposition; MoS_2 transfer

and etching; fine contact deposition; and final HfO_2 encapsulation with contact via opening.

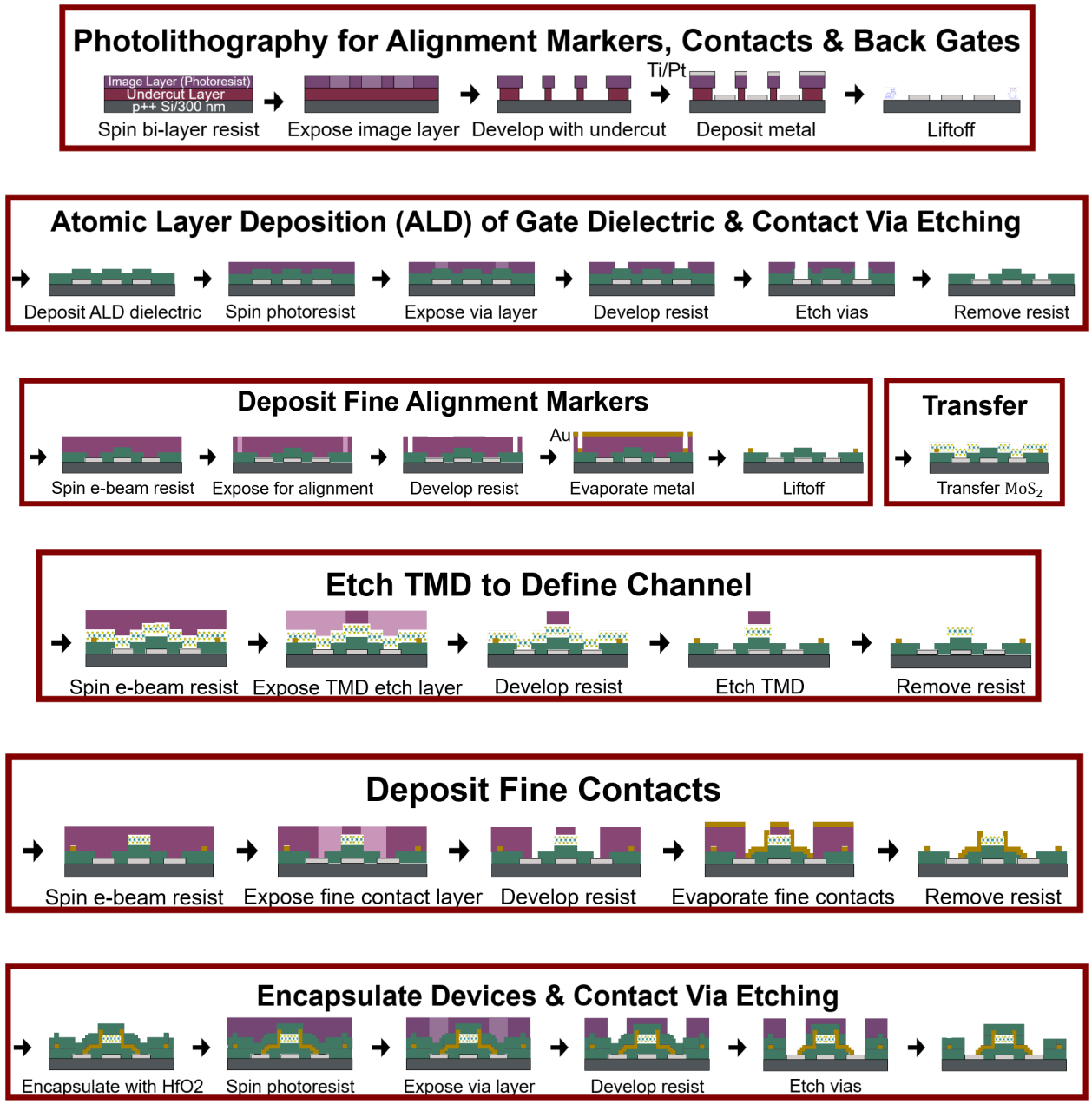


Figure 1: Fabrication process flow for LBG monolayer MoS_2 Hall bar devices

The starting substrate is a Si/SiO_2 wafer. Coarse alignment markers, local back gates, and large-area contacts are patterned by photolithography and metal liftoff. A HfO_2 gate dielectric is then deposited by atomic layer deposition, followed by contact via lithography and dielectric etching to reopen electrical access to buried metal features.

Next, fine alignment markers are fabricated to support later high-resolution lithography. Monolayer MoS_2 is transferred onto the prepared substrate, patterned into isolated Hall bar channels, and etched to define the active device regions. Fine source, drain, and voltage-probe contacts are then aligned to the MoS_2 channels and deposited by evaporation. Finally, the devices were encapsulated with HfO_2, and vias were opened to expose the contact pads for probing and Hall measurements.

2.2 Device/Material/Process Design

The target structure is a gated Hall bar device consisting of a Si/SiO_2 substrate, Ti/Pt local back gates and coarse contacts, HfO_2 gate dielectric, monolayer MoS_2 channels, and Au-based fine metal contacts.

The Hall bar geometry was selected because it enables simultaneous measurement of longitudinal voltage, transverse Hall voltage, drain current, magnetic field response, and gate-dependent transport [4, 5]. An illustration of the hall bar voltages and layout are seen in Fig. 2. In this figure, V_{XY} is the transverse hall voltage, V_{XX} is the lateral voltage, V_{DS} is the voltage from drain to source, and V_{GS} is the gate bias voltage. Here a $\vec{B}$ is the applied magnetic field. From these voltages and resulting current, hall mobility (μ_H) and hall resistivity (R_H) can be calculated according to equations 1 and 2:

$$R_H = \frac{1}{qn} \qquad [1]$$

$$\mu_H = \frac{\sigma}{qn} \qquad [2]$$

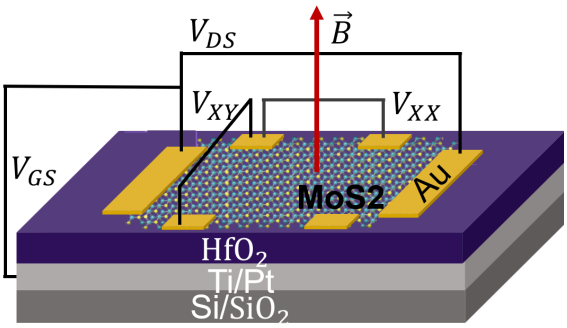


Fig. 2. Schematic and measurement configuration of the gated MoS_2 Hall bar device

Finite-element simulations were used during design to estimate geometry-induced voltage mixing and current distortion. The simulation compared good and poor Hall bar geometries and showed that geometry alone can contribute substantial measurement error due to current non-uniformity if voltage probes or channel dimensions are poorly designed [1, 4, 5, 6]. An example comparing low and high error geometries can be seen in figure 3. This motivated the use of narrow, symmetric Hall bar structures with particular geometric ratios.

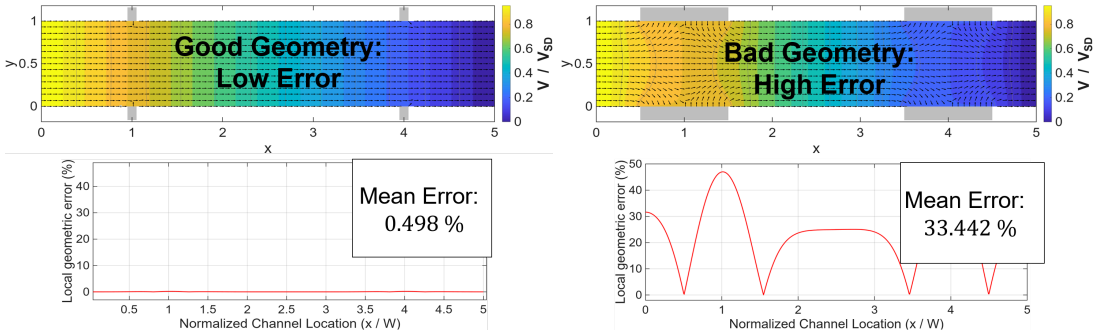


Figure 3: Finite-element simulation of geometry-induced voltage mixing error (using current distortion as a proxy) for optimized and non-optimized Hall bar layouts.

The final fabrication mask included Hall bars, Hall sensors, TLM structures, capacitors, open structures, and short tests, as shown below in Fig. 4. TLM devices were included to estimate contact resistance and distinguish channel-limited behavior from contact-limited behavior. Open and short structures were included as process monitors.

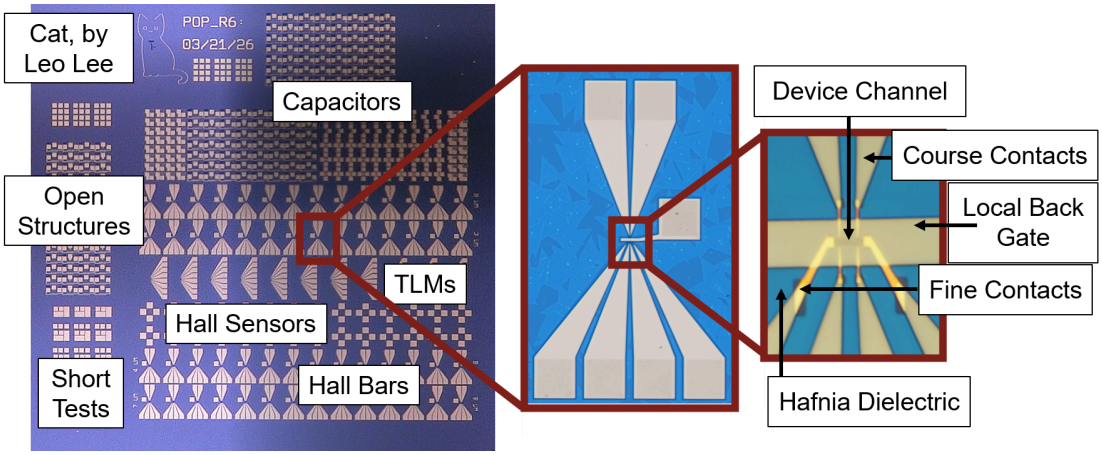


Figure 4: Optical microscopy of the completed chip and representative Hall bar device.

Relevant Hall bar dimensions included micron-scale channels with approximately 1 μm channel width and several-micron channel lengths. There were six variants of Hall bar, each with a different channel length; 2 μm, 3 μm, 4 μm, 5 μm, 7 μm, and 9 μm. The purpose of these varying lengths is to later enable finer tuned mobility testing to see which length gives the most consistent and accurate hall measurements. All of these fine features are validated by AFM. AFM measurements confirmed device dimensions and demonstrated approximately 50 nm alignment accuracy.

Overall, the project successfully fabricated 448 completed devices through 49 fabrication steps using 17 tools over 10 weeks.

2.3 Materials and Tools

The materials used in this process include Si/SiO_2 substrates, Ti/Pt for local back gates and coarse metal features, ALD HfO_2 for the gate dielectric and encapsulation, monolayer MoS_2 as the active semiconductor, and evaporated metal for source, drain, and Hall voltage contacts. The process also required photoresists (LOL2000, and Shipley 3612), e-beam resists (CSAR), developers (Mf-26A and xylenes), etchants (XeF_2), solvents (acetone, IPA), and transfer materials for MoS_2 placement and device patterning. The project used 17 nano@stanford shared tools and took more than 100 paid tool hours, with the largest fabrication costs coming from e-beam lithography (EBL) and atomic layer deposition (ALD)-based processing.

Overall, the tool usage reflects the central process challenge of the project: fabricating micron-scale gated Hall bars required both conventional optical lithography for large features and higher-resolution e-beam lithography for the MoS_2 channel, fine contacts, and, most critically, voltage probes. The combination of ALD, etching, lithography, evaporation, AFM, and Hall measurements created a complete fabrication and characterization workflow that future users can reuse for gated 2D transport devices.

3. Results and Discussion

3.1 Process Iterations (i.e. Design of Experiments (DOE))

The final fabrication process successfully produced two full chips of LBG monolayer MoS_2 Hall bar devices, each separated into four quadrants. Each quadrant contained 56 Hall bar devices for a total of 448 Hall bar devices. The completed chips included Hall bars, Hall sensors, TLM structures, capacitors, open structures, and short-test structures, allowing the Hall devices to be evaluated alongside process-control and critical device parameter measurement structures.

This project was not focused on optimizing a single deposition or etch recipe. Instead, the main goal was to develop a working device fabrication flow. The final flow requires local back-gate fabrication, HfO_2 gate dielectric deposition, via opening, MoS_2 transfer, MoS_2 channel definition, fine contact alignment, contact metallization, encapsulation, and final via opening. Each module is designed to preserve the MoS_2

channel and maintain electrical access to the local gate, source/drain contacts, and Hall voltage probes.

TLM devices were used to evaluate contact behavior, while capacitors, open structures, and short tests provided checks for dielectric integrity, unintended shorts, and process reliability. This helped decouple Hall-bar-specific issues from broader fabrication problems.

Critical design iteration occurred before fabrication through the use of geometry simulations before Hall bar design. Finite-element simulations showed that Hall bar geometry alone can introduce voltage-mixing error (using current-distortion as a proxy). A “good” geometry produced a mean error of approximately 0.498%, while a “bad” geometry produced a mean error of approximately 33.442%. This result motivated careful Hall bar layout, symmetric and very narrow voltage probes, and dimensional validation after fabrication. AFM measurements confirmed the fabricated device dimensions and showed approximately 50 nm alignment accuracy.

The main process issue that remained was electrical robustness, especially when faced with ESD. Fabrication alone was not the only barrier to reliable Hall measurements and future users should avoid treating completed Hall bars as automatically measurement-ready; device integrity should be checked before and after probing or Hall characterization because the devices are particularly sensitive to ESD due to their narrow probes.

3.2 Device/Material/Process Performance

The fabricated devices demonstrated the intended LBG Hall bar platform for monolayer MoS_2 carrier transport measurements. The device structure enabled simultaneous electrical access to the back gate, source/drain contacts, longitudinal voltage probes, and transverse Hall voltage probes. This allowed comparison between field-effect mobility and Hall mobility, which was the main characterization goal of the project.

Electrical measurements showed good on-current (Fig. 5A) and near-linear I_D/V_D behavior, suggesting approximately ohmic contacts (Fig. 5B). Bias-stress measurements showed minimal degradation under the tested conditions, which is important because Hall measurements require stable devices during magnetic-field and current reversal protocols.

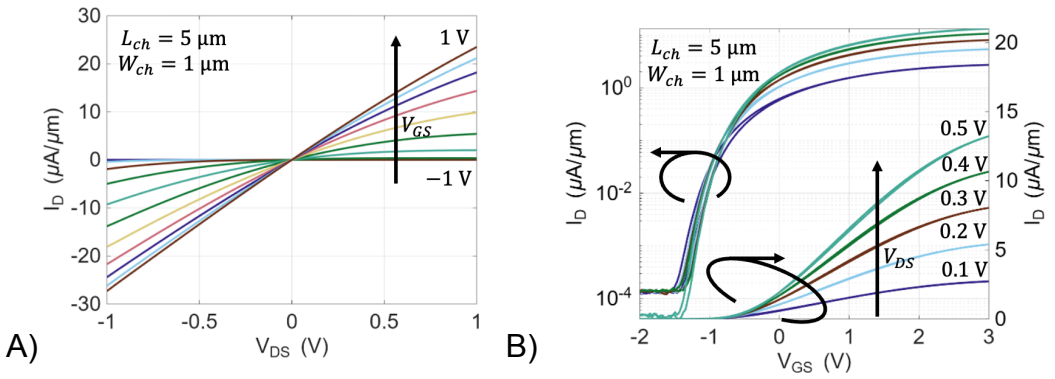


Fig. 5. Electrical output and transfer characteristics of a representative local-back-gated MoS_2 Hall bar (Lch = 5 µm, Wch = 1 µm)

The mobility results were physically reasonable and internally consistent. The preliminary final field-effect mobility values measured on the first successfully tested device this quarter were approximately 8–12 cm²/V·s, with Hall mobility values of approximately 7–12 cm²/V·s, and sheet carrier concentration of approximately 3–5×10^13 cm^{-2}. Literature-reported Hall mobility values for monolayer TMDs vary widely depending on dielectric environment and measurement methodology. For encapsulated WS_2 with hexagonal boron nitride, values exceeding 100 cm²/V·s have been reported, though those devices benefit from dramatically reduced interfacial disorder compared to oxide dielectrics [2]. Further, contact resistance can cause field-effect mobility to be significantly overestimated without four-probe or TLM correction, meaning some literature values may be artificially inflated [3]. The values measured here are therefore physically plausible, and the convergence between field-effect and Hall mobility suggests contact resistance was not a dominant error source in this extraction.

Despite this, Hall measurements in monolayer TMDs remain challenging. The true Hall voltage is small, and the measured transverse voltage contains contributions from misalignment voltage, thermomagnetic effects, Nernst and Righi-Leduc components, Ettingshausen offsets, geometric error, and drift, as shown in Fig. 6D [4]. Isolating the true Hall signal from these artifacts requires careful geometry design, field and current reversal protocols, and device stability; all of which were addressed in this work but remain areas for refinement.

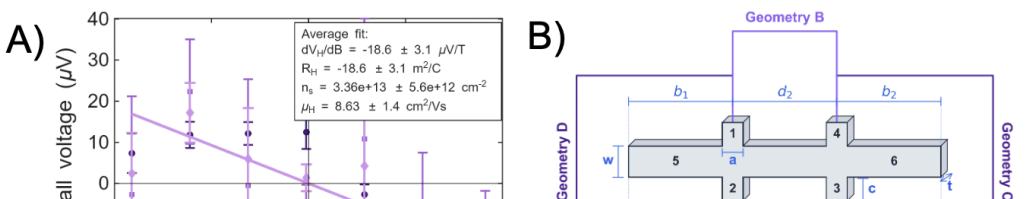


Figure 6: Hall measurement results and voltage contribution analysis for fabricated MoS_2 Hall bar devices

4. Conclusions and Future Work

4.1 Conclusions

This project established a complete, documented fabrication and characterization workflow for LBG Hall bar devices in monolayer MoS_2, producing 448 fully fabricated devices integrating Ti/Pt local back gates, HfO_2 gate dielectric, monolayer MoS_2 channels, Au-based contacts, and HfO_2 encapsulation.

The central result is not simply working devices, but also agreement between field-effect and Hall-based transport metrics. The measured field-effect mobility was approximately 8–12 $cm^2/V{\cdot}s$, Hall mobility was approximately 7–12 $cm^2/V{\cdot}s$, and sheet carrier concentration was approximately 3–5×10^13 cm^{-2}. The main process insight was that Hall measurements in monolayer TMDs require more than a working transistor: geometry, contact quality, device stability, and electrostatic discharge sensitivity all strongly affect whether the extracted Hall signal is meaningful. The geometry

simulations showing mean errors ranging from 0.498% to 33.442% depending on Hall bar layout are particularly instructive in demonstrating that a poorly designed device can produce misleading results even with a perfect fabrication process. In fact, the Hall mobility values reported here may still have geometric artifacts showing up as larger Hall voltages and therefore lower Hall mobility values and this should be explored in more detail in future project iterations.

4.2 Future Work

Future work should first address the electrostatic discharge challenge identified during the project. This includes testing safer probe-handling procedures, improved grounding, and more comprehensive pre-checks. Future devices should also include systematic gate-voltage-dependent Hall measurements to extract sheet carrier density and Hall mobility, rather than only comparing mobility at a limited bias condition. Temperature-dependent Hall measurements should be added to separate

contact-limited behavior, impurity scattering, phonon scattering, and thermally activated transport. Finally, the process should be extended to other TMDs, especially WS_2 and WSe_2, to determine whether the same gated Hall bar design and fabrication sequence can support broader 2D materials characterization. Additionally, larger sample sizes (i.e. more devices) should be measured to build trends and ensure repeatability in measurements.

5. Budget

TABLE 1: PROJECT BUDGET

Category	Tool / material	Percentage of Budget	Purpose
Fabrication	EBPG / electron-beam lithography	29.7%	Fine lithography for Hall bars, voltage probes, contacts, and alignment-critical features
Training	Tool training	20.4%	Required access for fabrication and characterization tools
Fabrication	Heidelberg photolithography	7.9%	Optical lithography for larger features such as pads, back gates, coarse contacts, and via layers
Fabrication	Beneq ALD	7.8%	HfO_2 gate dielectric and encapsulation deposition
Characterization	Lake Shore Hall system	5.2%	Hall voltage, sheet carrier density, and Hall mobility measurements
Fabrication	Pt-Ox	3.5%	Oxide/dielectric etching, including via opening
Fabrication	AJA evaporator	3.3%	Metal deposition for gates, contacts, and pads

Characterization	Woollam ellipsometer	3.2%	Thin-film thickness measurement
Supplies	Supplies	3.0%	Resists, chemicals, wafers, solvents, and other consumables
Characterization	XPS / VersaProbe 4	3.0%	Material and surface chemistry characterization
Fabrication	Headway spinner	2.8%	Photoresist or e-beam resist spin coating
Fabrication	Samco etcher	2.6%	MoS_2 or device-layer etching
Fabrication	SVG developer	2.5%	Photoresist development
Characterization	Cypher AFM	2.4%	Device geometry, morphology, and alignment validation
Fabrication	SVG coater	2.1%	Photoresist coating for photolithography

Total cost was $4999.47 out of the budget of $5000.

6. Acknowledgements

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Yang, Lauren Hoang, Dr. Crystal A. Nattoo, Dr. Zherui Han, Dr. Hao-Yu Lan, Yuan-Mau Lee, Dr. Xiangjin Wu, and Dr. Robert K. A. Bennett (in no particular order).

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