Flip-Chip Indium Bump Bonding for Superconducting Circuit Integration

ENGR 241 SPR23 Final Report

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Contents

1 Acknowledgements

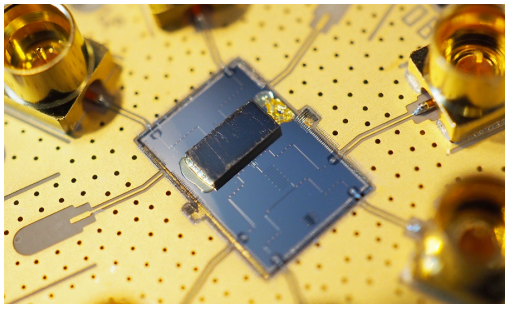
We would like to recognize and thank our industry mentors, Mark and Tony, for the helpful suggestions and feedback that enabled the results we show in this report. They proposed elegant solutions to many of the problems we encountered, which proved critical in demonstrating a successful flip-chip indium bump bond. We would also like to thank Swaroop Kommera, our SNF mentor, for the tool suggestions and for all the last-minute training. Swaroop's rich experience in photolithography and packaging and his knowledge of the SNF tools were essential to our process development.

We also extend thanks to many other members of the Stanford community who helped us to set up experiments, solve fabrication challenges, and helped to guide this project. In particular, we'd like to thank Grant Shao, who developed a thick indium deposition for the KJL evaporator and dealt with the chaos that resulted. We'd also like to thank Takuma, a member of our group, who helped us with low-temperature measurements and packaging and offered practical guidance for the project direction. We'd also like to thank Sandesh Kalantre and Aaron Sharpe from the Goldhaber-Gordon Group, who led cooldowns and transport measurements on our samples as we developed the thick indium and flip-chip bonding recipes. We also thank Pingyu Wang who generously shared with us his notes and knowledge of the single-layer liftoff.

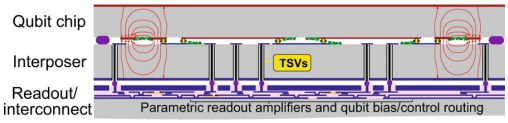
2 Introduction and Motivation

Superconducting quantum systems have been proven advantageous to other physical platforms on many fronts, including quantum sensing, quantum simulation, and secure communications. As the field matures, recent work on superconducting hardware begins to explore the versatility of material platforms, namely *heterogeneous integration* of quantum devices.

While bringing together different units with state-of-the-art performances opens up unique opportunities in quantum science, it also presents the challenge of integrating incompatible materials and fabrication processes. For example, coupled aluminum-on-sapphire qubits and lithographic niobium cavities may offer gate fidelities and memory coherence times unachievable with a single material system and shared fabrication process. However, the metal-based qubits cannot withstand the necessary cleaning steps for mechanical device preparation.



(a) An example of a capacitively coupled flip-chip device: the top chip (mechanics) is secured face down to the bottom (qubit) with adhesive [5].



(b) Envisioned scheme [4] for control and readout of a large-scale, 3D integrated quantum processor.

Figure 1: Example applications of flip-chip quantum systems

Additionally, these GHz-band systems rely heavily on precise manipulation of low-energy states of a circuit, and thus need to be kept at ultra low-temperatures with minimal dissipation. This adds to the technical challenge of co-packaging: any die-to-die interconnect must offer superconducting links with controllable coupling and capacitance. Current solutions, such as capacitive coupling between flip-chips (Figure 1a), offer limited coupling strengths and do not allow for DC currents to pass between chips, as is necessary for some device tuning techniques. Quantum system architectures assume this capability and posit a superconducting galvanic 'bump-bond' connection (Figure 1b) between the top and bottom chips. This type of interconnect has been demonstrated over the past decade [1], but is yet to be introduced to the Stanford Research community.

Our project aims to develop a superconducting flip-chip interconnect for quantum circuits. As a part of the ENGR 241 course, our processes will be available for all users of the Stanford Nanofabrication Facility, and, hopefully, could support the development of integrated quantum systems in general at Stanford University and SLAC.

3 Project Goals and Summary

The most basic requirement of a flip-chip DC-capable qubit interconnects is a superconducting path between the top metal on the bottom chip and the top metal on the top chip. This project demonstrates this interconnect through DC four-point resistance measurements, and

in the process develops the following fabrication steps:

1. Depositing thick (2 µm) superconducting indium → demonstrated in the SNSF KJL evaporator
2. Patterning thick (2 µm) superconducting indium with 100 µm feature sizes → demonstrated with shadowmasks, bilayer lift-off resist lithography, single-stack lithography
3. Flip-chip bonding of indium-on-aluminum structures → demonstrated with the SNF Finetech Lambda (flipchipbonder).

The rest of this report summarizes the technical and scientific aspects of each of these fabrication steps.

The proposed project goals are necessary but not sufficient to build a qubit-compatible flip-chip interconnect. For example, there will be a thermal expansion mismatch between top and bottom chips fabricated from dissimilar materials. As any quantum system will temperature cycle between millikelvin and room temperature, micromechanical systems to accommodate the resulting top chip - bottom chip strain will be necessary for a practical system. We consider this outside of the scope of the quarter-long project, but it will be pursued in future work. Furthermore, real quantum systems operate not at DC, but at GHz frequencies. As AC dissipation is dependent not only on absolute resistance, but on the dielectric / AC behavior of residual photoresists, interfaces, and intermetallics, characterizing the AC behavior of a bump bond will be critical for integration in a real system. Again we will investigate this in future work.

4 Fabrication Flow

This project demonstrates a simple flip-chip indium-to-indium bond on a thin-film aluminum on a silicon substrate. This is representative of a traditional qubit system, in which the qubit and transmission lines are fabricated out of aluminum. A summary of the overall process flow is shown in Figure 2.

The layer stack and a cartoon of our demonstration superconducting device are shown in Figure 4b. The four-point wirebond pads are fabricated in the aluminum mask, and bump bonds form an Al → In → Al path. A ρ-T measurement across this path, therefore, should reveal the superconducting properties of the Al-In interface and of the In-In bump bond interface. Planar versions of this device (Figure 4a) were also fabricated to test the T_c of the In films. Note that the aluminum oxide must be removed prior to indium deposition, which we accomplished using the argon ion mill in the KJL evaporator.

We also fabricated more complex designs with 'chains' of bumps over several millimeters, inspired by a device fabricated at Google Quantum [1]. Here, the top and bottom chips share the Al-In layer stack, with In only deposited at the bump locations. The fabrication flow for these larger designs is identical to that of the four-point designs. A cartoon of this design is shown in Figure 3.

Existing literature on flip-chip superconducting indium bump bonding typically requires

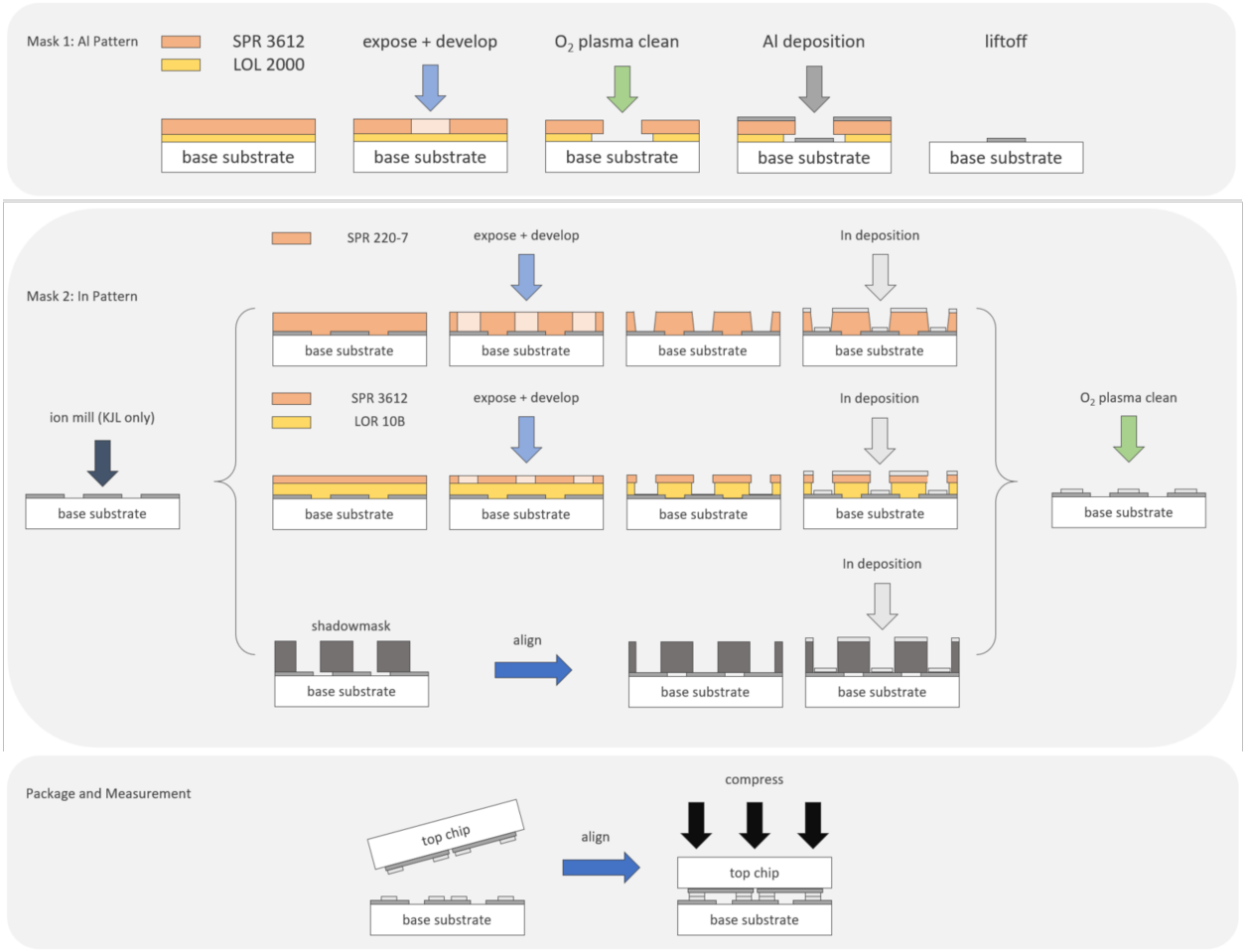


Figure 2: The overall process flow for flip-chip fabrication and bonding. A well-understood liftoff process defines the Al layer. Three techniques - single-stack liftoff, double-stack liftoff, and shadowmasking - were developed to define the In layer. The Finetech Lambda flip-chip bonder is then used to bond the top and bottom chips.

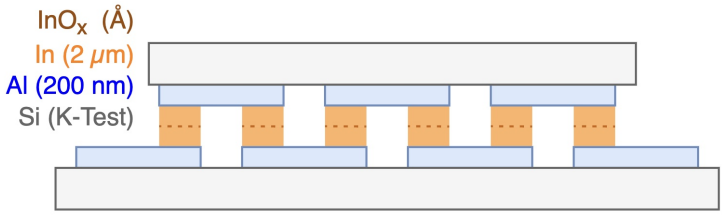
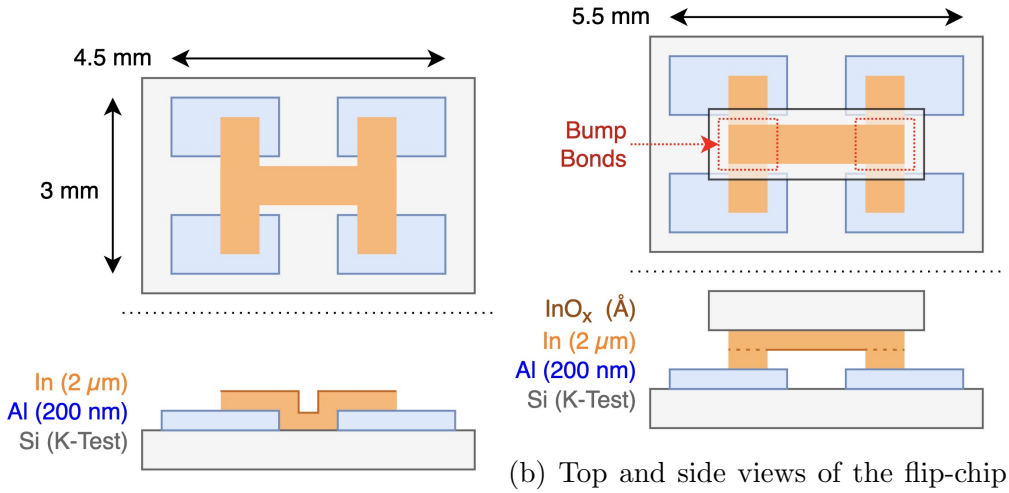


Figure 3: Side view of a four-point array device, where indium only forms the bumps which connect the top and bottom devices. This structure allowed us to test bump yield.



(a) Top and side views of the planar four-point test device.

(b) Top and side views of the flip-chip four-point test device. The indium cold-welds to itself during flip-chip bonding, breaking through the native oxide.

Figure 4: Cartoons of the four-point test devices used in this work.

one or multiple 'UBM'(s), or under-bump metallization layer(s), between the indium and aluminum layers [1]. These metallization layers are theorized to restrict diffusion and to pass superconductivity between materials via proximity effects. However, recent work suggests that a UBM might be unnecessary [6], and we also observed a superconductivity between Al and In at DC with no UBM (see Section 5.2.4). However, we have not studied losses at RF, where the Al-In interface may begin to contribute.

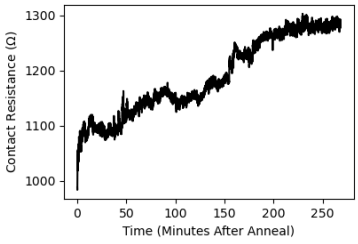
5 Depositing μm-Thick Superconducting In

Successful bump bonding requires that the bump height is larger than any misalignment tolerance in the bonding tool. Large bond heights are also desirable for reducing chip-to-chip capacitance. However, depositing thick indium is challenging. As a reasonable compromise between deposition time and bump height, we targeted 2 μm bumps, for a maximum chip-to-chip spacing of 3 μm with a 25 % crush factor.

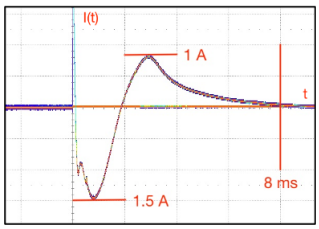
We began by depositing 2 μm In in the Innotec electron-beam (e-beam) evaporator, which was not of sufficient material quality to superconduct. We then proceeded to test the deposition of thinner (200 nm) In films in the KJL evaporator (SNSF), experimenting with shadowmasks, contacts, and adhesion layers. After observing superconductivity, we deposited thick 2 μm films suitable for flip-chip bonding.

5.1 Innotec E-Beam Evaporator

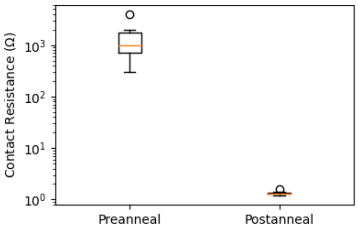
Initial attempts at thick In deposition were done in the Innotec electron-beam evaporator due to the accessibility and flexibility of the tool. A 5N source was acquired from ACI Alloys,



(a) The contact resistance of aluminum-indium wirebonds increases over time.



(b) A high-current pulse anneals the wirebond contact.



(c) The anneal decreases and stabilizes wirebond contact resistance.

Figure 6: Electrical annealing improves aluminum-indium wirebond contact resistance.

suitable for a graphite crucible liner[1], which was then installed in an SNF custom copper crucible. 2 µm films were deposited on K-doped 100 mm test wafers purchased from the SNF stockroom. In general, depositions were done at base pressures of 1×10^{-6} torr, accessible in a 2 h pump-down, and without Ti gettering. All depositions were done at 20 Å s^{-1}, and post-deposition thickness was confirmed through profilometry.

Deposited films appeared uniform by eye and under an optical microscope. Under SEM, film surfaces appeared flaky at a scale of 3 µm with pockmarks between 'flakes'. A representative SEM image of In on Si is shown in Figure 5.

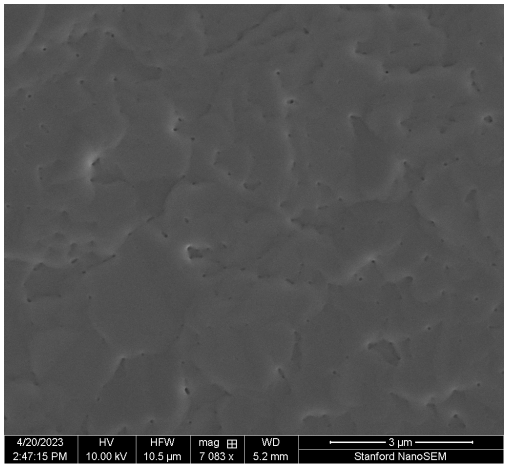


Figure 5: SEM of In deposited on Si. The length scale of the 'flakes' is ≈ 5 µm.

5.1.1 Wirebonding to Indium

Wirebonding to Indium proved to be challenging. Bonding Au wire failed at all power and time parameters and at temperatures up to 100 °C. Bonding with Al wire at room temperature and at power/time of 200/90 was partially successful, but the contact resistance was high, and contacts failed over time. This is shown in Figure 6a. However, annealing with a high-current pulse (Figure 6b) (1 A, 1 ms) drastically reduces and stabilizes contact resistance (Figure 6c). After the anneal, no change in contact resistance was observed on a timescale of days. This annealing technique was then used for all indium on silicon wirebonded samples.

[1]Kurt J. Lesker P/N EVCFABEB-13

5.1.2 Testing for Superconductivity

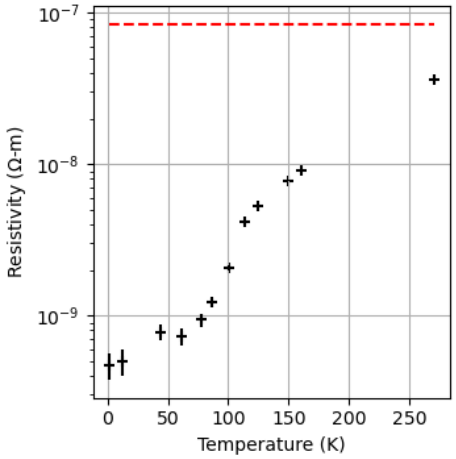


Figure 7: Resistivity of the Innotec-deposited indium film as the temperature is swept to 1.4 K. The red dashed line is the $T = 300$ K resistivity as reported in the literature. No superconducting transition was observed.

We did not observe superconductivity in Innotec-deposited In samples. Two 2 µm thick samples were cooled to 1.4 K in a helium cryostat in David Goldhaber-Gordon's research group, with the cooldown led by group members Aaron Sharpe and Sandesh Kalantre. Measurements were taken by an SR830 in a four-point Van der Pauw configuration with 100 µA bias current during the cooldown, and the $\rho(T)$ trace is shown in Figure 7. No superconducting transition was observed, and so no more low-temperature devices were metalized in the Innotec.

It is possible that a longer pump-down or pre-deposition Ti getter would provide sufficient film quality for superconductivity, but this was deemed outside the scope of this project.

5.2 KJL E-Beam Evaporator

The KJL electron beam evaporator, located in the SNSF nanopatterning cleanroom, offers low base pressures and an in-situ ion mill, both of which are required for high-purity In with an ohmic connection to the underlying aluminum. It, therefore, became the primary deposition tool for this project, using a 4N source provided by ACI Alloys.

All indium deposited in the KJL had an underlying aluminum contact layer, with an optional adhesion layer. This aluminum layer was either defined with lift-off lithography, using a Plassys evaporator in the Safavi-Naeini group (LINQS), or defined through shadowmasks in a prior KJL deposition. Adhesion layers, when used, were deposited in the same pump-down as indium.

5.2.1 Indium and Aluminum Deposition SOP

Here we describe the SOP for a full aluminum and indium shadowmasked deposition, used to create the four-point planar test structures that demonstrated superconductivity. All depositions were on K-doped test 100 mm Si wafers.

1. Clean the wafer. Rinse for 30 s in acetone, followed by 30 s in IPA. Optionally descum using the PX-250 Plasma Asher in the SNSF Flexible Cleanroom. First clean the chamber at 300 W, 3 sccm O_2, for 60 s. Then install the sample on the indirect plate, and descum at 100 W, 10 sccm O_2, for 143 s.

2. Align the Al shadowmask with the wafer using a shadowmask alignment tool, such as

the custom jig described in Section 6.2.3, then kapton tape the shadowmask on the wafer as shown in Figure 8.

3. Secure the wafer and shadowmask on the KJL sample mount using the given tab clamps, load the sample mount in the KJL, and pump down. Typical pumpdown times with the shadowmask and kapton tape ranged from 10-12 minutes.
4. Deposit 100 nm of Al at 3 Å s^{-1}
5. Remove sample, remove the Al shadowmask, and install the In shadowmask. Then, load and pump down.
6. Ion mill the Al oxide. **We used the parameters listed below, but a longer ion mill is suggested to ensure that the Al oxide is removed.**
   - 7.0 sccm Ar (6.9 sccm observed)
   - 0.55 A emission (0.55 A-0.64 A observed)
   - 300 V discharge (114 V-143 V observed)
   - 0.5 A discharge (0.5 A observed)
   - 30 s etch time
7. Ti getter, using the given gettering recipe. Pressure after gettering should be below 1×10^{-7} torr.
8. The adhesion layer was deposited to the desired thickness at the desired rate.
9. Indium was deposited to the desired thickness using the 20 Å s^{-1} recipe. Pressure during deposition was $< 1 \times 10^{-7}$ torr.
10. The sample was removed, the sample mount reinstalled in the evaporator, and pumped down. 30 nm of Ti was deposited using the 3 Å s^{-1} recipe as an In capping layer on the growth chamber and sample mount, after which the sample mount was removed from the evaporator.

5.2.2 Indium Adhesion Layer Failure

Initial KJL experiments only deposited 200 nm of indium due to the cleanliness issues inherent in thick indium depositions. However, In has large surface mobility, and so tends to form 'islands' on the substrate for thin layers, as can be seen in Figure 9. There are two possible approaches to uniform thin-film growth of indium: to reduce substrate temperature, which decreases surface mobility [2], and to introduce an adhesion layer prior to indium deposition. As the substrate temperature in the KJL evaporator is fixed, we therefore **explored several adhesion layers without success**, which are illustrated in Figure 10:

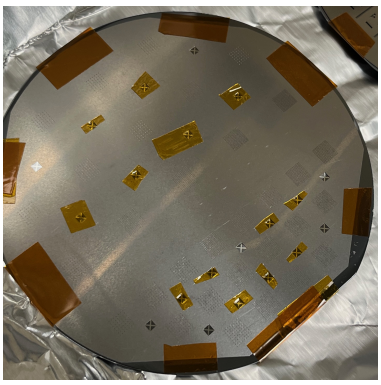
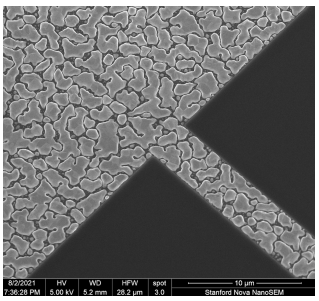
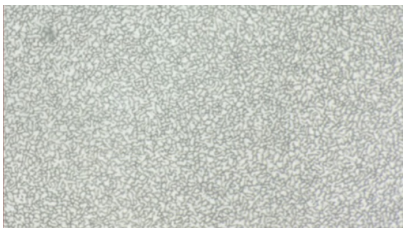


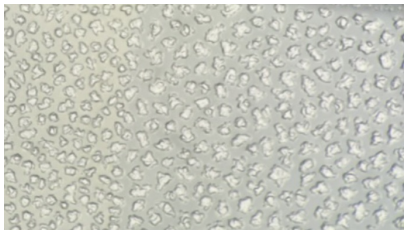
Figure 8: Shadowmask aligned with wafer and fastened with kapton tape.



(a) Indium deposition on a Ti adhesion layer. Deposition and SEM done by Takuma Makihara.



(b) Optical image of indium deposited on an Al adhesion layer. Small islands are visible.



(c) Optical image of indium deposited on a TiPd adhesion layer (right), and on Si (left). Note the larger islands forming on the TiPd layer.

Figure 10: SEM of indium films deposited on various adhesion layers. No adhesion layer offered a coherent film for indium thickness $< 200\,\text{nm}$.

1. No adhesion, 100 nm In (Done by Grant Shao in 2023). In islands of scale 0.5 µm.
2. 10 nm Ti (done by Grant Shao in 2021), 150 nm In: asymmetric In islands still observed of scale 2 µm.
3. 7 nm Al: In islands of scale 2 µm to 3 µm.
4. 5 nm Ti, 5 nm Pd: In islands of scale 10 µm to 100 µm.

We observed that these films were not coherent in electrical transport: no current-carrying path existed between two points spaced by $\approx 1\,\text{cm}$. We briefly explored reflowing these films in the atmosphere, at a maximum temperature of 150 °C. This increased grain size and grain nonuniformity (as seen under an optical microscope), but did not lead to a coherent film.

In contrast, aluminum stuck well to the cleaned Si+SiO_2 wafer surface, with all films measured displaying good uniformity in SEM and low resistance in transport. No further characterization (profilometry, AFM) was done.

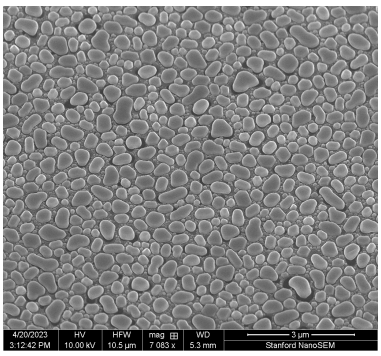


Figure 9: Indium islands on a silicon substrate. Deposition and SEM done by Grant Shao.

5.2.3 Homogeneous In films in 2 µm KJL Deposition

Following the observation of superconductivity, we performed a shadowmasked 2 µm indium deposition on an aluminum contact layer which had been defined via lift-off lithography. This was the only 'thick' indium deposition done in the KJL as a part of this project and included indium lift-off sample chips, four-point planar and flip-chip, and large flip-chip devices. Detail on the patterning process is available in later sections.

Thick indium deposition has several advantages. First, >1 µm indium is necessary for bump bonding. Second, the indium 'island' grains observed during thin growths arise from stronger indium-indium than indium-substrate interactions, so thick growths can span gaps between 'islands', therefore providing a coherent film.

SEM images of the resulting film (Figure 11) confirmed coherence, without the pockmarks observed in the earlier Innotec deposition. Transport measurement showed resistivity similar to the literature on bulk indium.

5.2.4 Superconductivity Observed in Transport Experiments

A four-point planar device was fabricated in the KJL using shadowmasks, using the device design shown in Figure 4a and the layer stack shown in Figure 12. 200 nm of indium was deposited on 100 nm aluminum contacts with no adhesion layer, which led to an insulating film composed of disconnected In droplets. To solve this, the indium droplets were mechanically 'crushed' by rubbing the film with a cleanroom swab. Indium has a native oxide, but it is relatively brittle. Furthermore, indium cold welds to itself, so this 'crush' operation which cracks through the native oxide on droplet surfaces will provide a metallic indium interface between droplets. While this 'crushing' is a relatively uncontrolled process, it is relatively insensitive to the force applied - images and four-point resistance of a planar device during the 'crush' process are shown in Figure 13. It is easy to 'crush' droplets together, but difficult to remove the droplets from the wafer: so subsequent crush operations do not significantly increase resistance. Note that this process is also shown in a Nano Nugget.

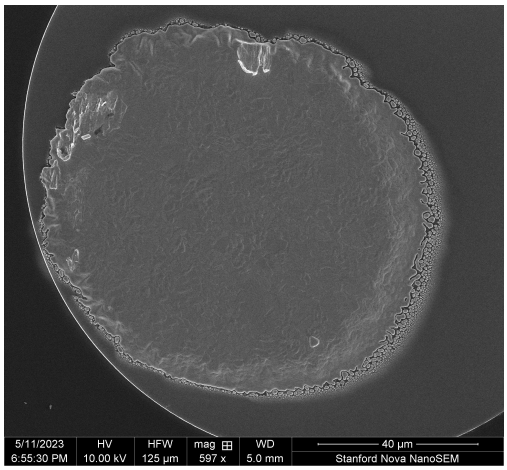


Figure 11: A 2 µm thick indium bump deposited on an aluminum pad in the KJL evaporator. Note how the surface is uniform, only forming island structures at the edges of the feature.

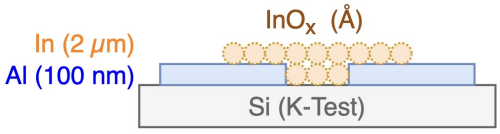


Figure 12: Layer stack of the 'crushed' four-point device. Islands (orange) were mechanically cold-welded together by the applied force.

The planar device was packaged in a four-point configuration with wirebonds on the Al contact pads. Observed contact resistance was 5-10 Ω, suggesting a good interface between Al and In, and therefore a successful ion mill of Al_2O_3 prior to In deposition.

The device was cooled to 1.4 K in the Goldhaber-Gordon group helium cryostat, with the cooldown led by Aaron Sharpe and Sandesh Kalantre. A superconducting transition was observed at $T \approx 3.5\,\mathrm{K}$ with overall $R_{300\,\mathrm{K}}/R_{1.4\,\mathrm{K}} \approx 25$ (Figure 14). This T_c matches the literature value of the bulk In transition, but residual resistance still existed in the system - likely due to In-InO_x-In grain boundaries

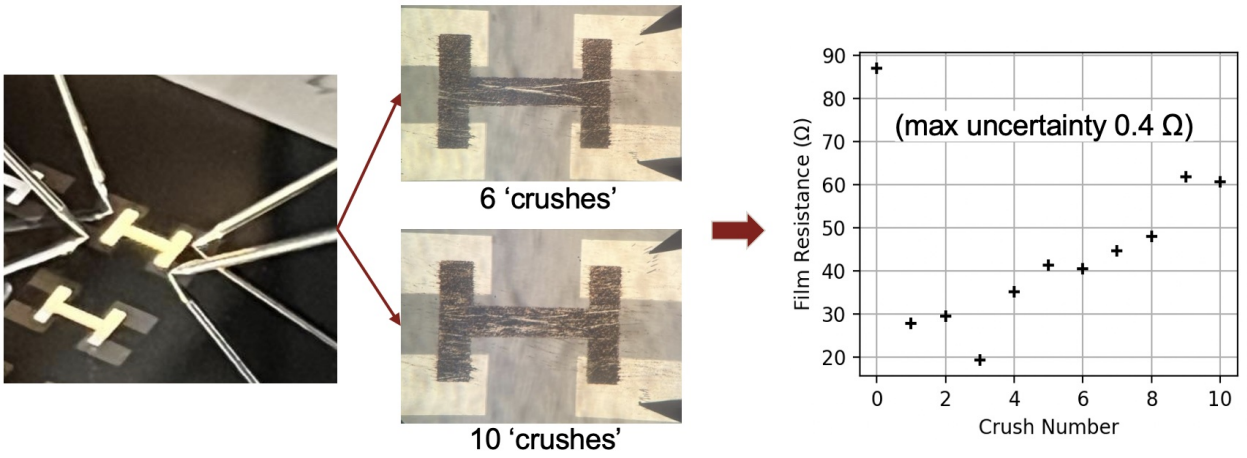


Figure 13: Mechanically 'crushing' the indium cold-welded islands together, forming a low-resistance film with a quasi-continuous current path from contact to contact.

which remained after the 'crush' operation. This hypothesis of a semi-continuous film with large variance in thickness is further supported by the large room-temperature resistivity of $R_{xx}(T = 273\,\mathrm{K}) = (3.6 \pm 0.1)\,\Omega$, about 20 times what would be expected of a uniform film.

However, this experiment demonstrated that the fundamental material quality of KJL-deposited In is sufficient for superconductivity, justifying experiments with thicker indium, as well as the development of a flip-chip process.

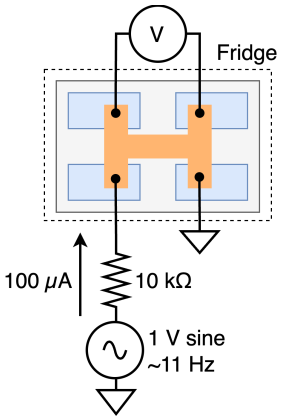
5.3 Post-Evaporation Anneal and Reflow

Several annealing and reflow experiments were done on thick In films deposited in the Innotec and in the KJL, to both change bump geometry and to remove any AlO_x at the Al-In interface. These are described in this section.

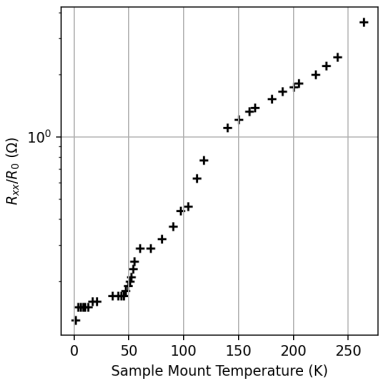
5.3.1 Annealing to Improve Al-In Contact Resistance

The 2 µm indium deposition in the KJL displayed uncontrolled contact resistance of order 10 kΩ between the aluminum contacts and indium patterns. We suspected this was due to an incomplete ion mill that left AlO_x at the aluminum-indium interface. This was supported by the very low resistance measured when directly probing the indium bars, and the similar In-Al resistance measured in an identical Innotec deposition, in which no ion mill was available. These experiments are summarized in Figure 15. Furthermore, the IV behavior was highly non-ohmic, and dependent on illumination (Figure 16). This photogeneration of carriers would expect a semiconducting InO_x interface, which may be formed by the interaction of indium and aluminum oxide.

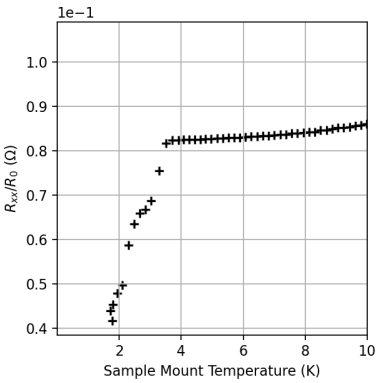
An anneal at 250 °C under forming gas (N_2,H_2) for 120 s was found to reduce this contact resistance to $\approx 1\,\Omega$, as is shown in Figure 17. As bulk indium melts near 150 °C, the hypothesized mechanism is that molten In allows H_2 access to the AlO_x interfacial layer, which reduces the oxide, and thereby allows In contact to the base surface. Notably, there



(a) Schematic of the four-point cooldown experiment.

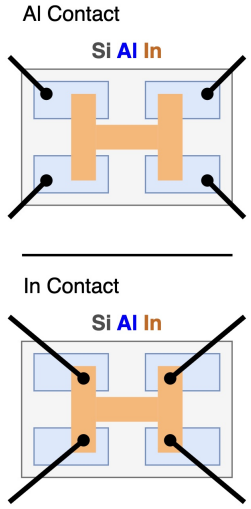


(b) Full $R(300\,\mathrm{K})$ / $R_{xx}(T)$ sweep, with $R(300\,\mathrm{K})$ / $R(1.4\,\mathrm{K}) \approx 25$, likely limited by remaining interfacial InO_x.

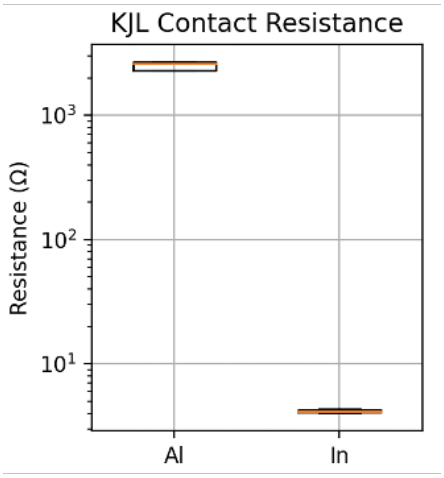


(c) A fine sweep of resistance around base temperature. A superconducting transition is observed for $T_c \approx 3.4\,\mathrm{K}$.

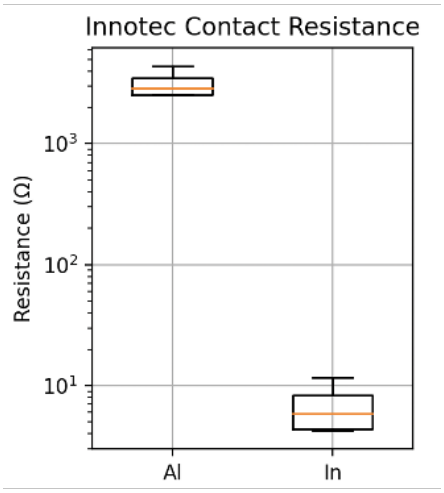
Figure 14: A schematic of the experimental setup and $R_{xx}(T)$ for a cooldown of mechanically 'crushed' indium, in which a superconducting transition was observed. An SR830 lock-in amplifier output and load resistor were used as a current source, and the SR830 demodulated the induced voltage across the device.



(a) Four-point contact resistance experiment, probing at the aluminum contacts or on the indium bar.



(b) Contact resistance of KJL-deposited four-point planar devices as a function of probe location.



(c) Contact resistance of Innotec-deposited four-point planar devices as a function of probe location.

Figure 15: A large increase in contact resistance in KJL-deposited devices is observed when probing aluminum contacts vs. the indium bar, suggesting some interfacial oxide. The observed contact resistance is similar to that for Innotec-deposited devices, in which an interfacial oxide is expected.

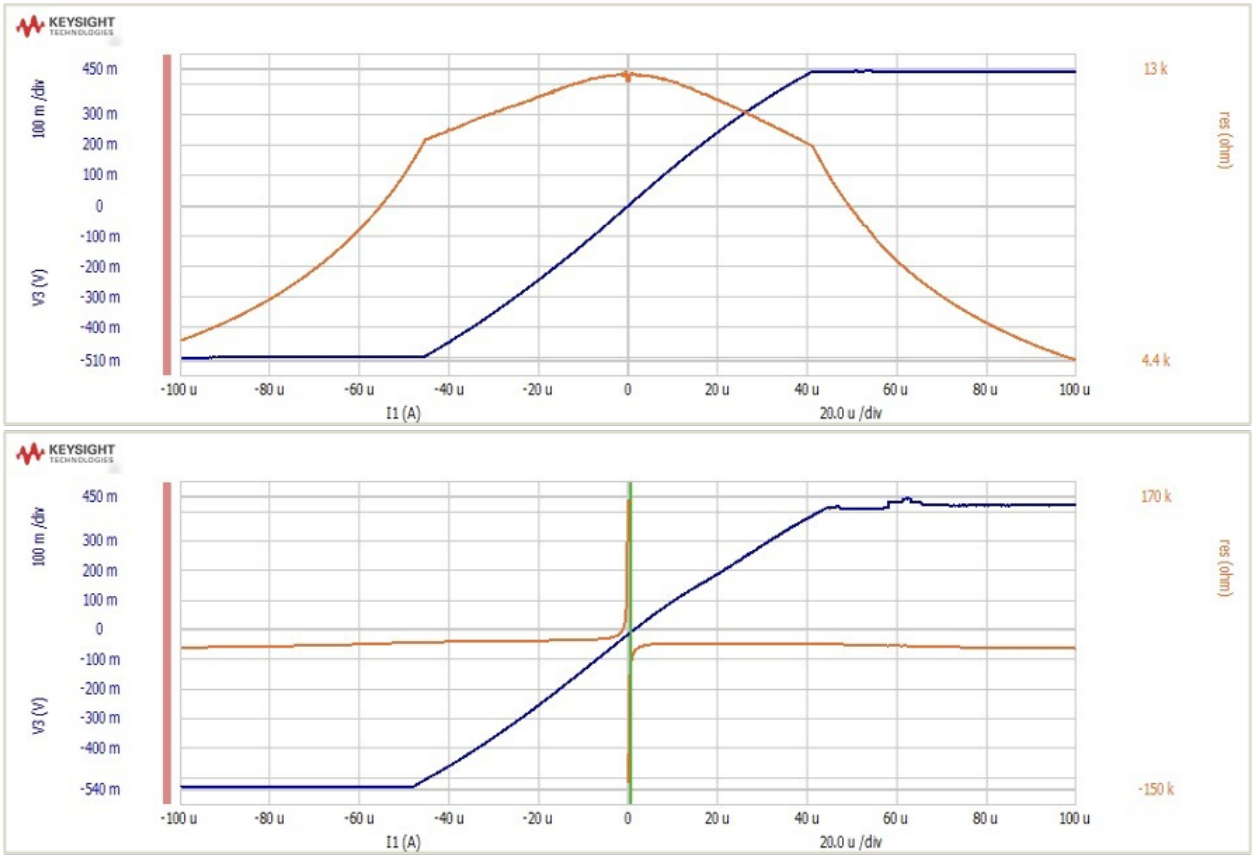
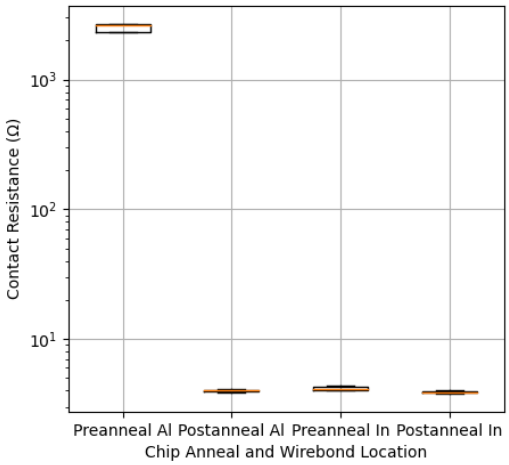
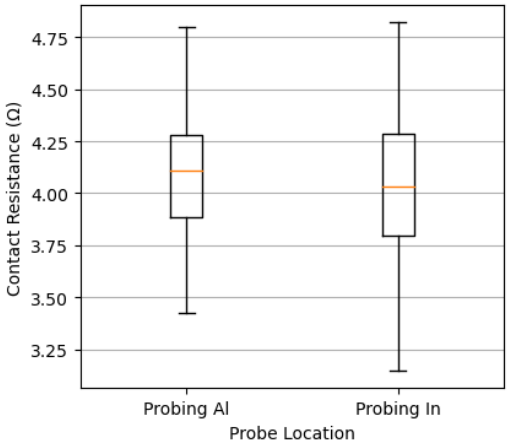


Figure 16: Four-point IV sweeps probing on aluminum contacts without (top) and with (bottom) illumination from the microscope objective. The orange trace, corresponding to resistance, drops in magnitude with the light off, signifying the photogeneration of carriers which decreases resistance.



(a) Contact resistance probing indium and aluminum before and after an anneal. A uniquely large contact resistance is observed when probing aluminum pads.



(b) Contact resistance probing indium and aluminum is indistinguishable after the anneal.

Figure 17: Contact resistance of a planar KJL device before and after an anneal under forming gas. After the anneal, the contact resistance through the aluminum pads is indistinguishable from that observed when directly probing the indium pads, suggesting good contact between the aluminum pads and indium bar.

was no visible change in the indium surface under an optical microscope, so the annealing process did not lead to 'clumping' of indium as was later seen in the reflow of an Innotec deposition.

This anneal was done in the SNF gold-contaminated Allwin 610 Rapid Thermal Annealer (RTA) using the temperature and gas profile shown in Figure 18. Note, however, that this same anneal failed for indium of identical thickness and geometry deposited in the Innotec evaporator. The indium fully reflowed, forming islands on the chip surface. This is likely due to some difference in the Al-In interface or in the indium composition itself between the KJL and Innotec depositions.

It is important to emphasize that this anneal was only developed to solve the insufficient ion mill specific to this deposition attempt. We generally try to avoid high temperatures (>100 °C) which can unintentionally anneal quantum devices (ex. transmons) fabricated in some previous process.

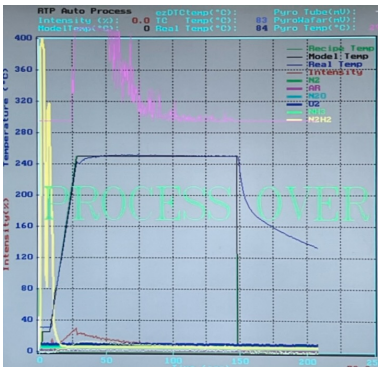


Figure 18: Photo of temperature / gas trace for the 250 °C, 120 s, N_2,H_2 anneal done in the SNF RTA.

5.3.2 Reflowing to Increase Bump Height

Full reflow of the indium bump bonds may be desirable for chips that do not contain devices sensitive to high temperatures (for example, a wiring interposer chip). This is because a reflow can increase effective bump height, as is demonstrated in an indium bump process (Figure **??**) developed for CMS detectors at the Paul Scherrer Institut [3]. This avoids the need for very thick In depositions when large chip-to-chip spacing is necessary, thereby saving source material and decreasing evaporator maintenance requirements.

We performed a reflow temperature/time DoE under forming gas to find the minimum parameters necessary to fully reflow 2 µm In on Al, with In deposited in the Innotec. The pattern tested was 100 µm diameter In circles on 150 µm Al pads. The minimum temperature required for full reflow was found to be 280 °C, for a reflow time of 120 s. A lower temperature and longer reflow may be possible, and visible signatures of reflow appeared at 250 °C, but 120 s was the longest time tested.

The In/Al pattern after reflow is shown in Figure **??**. Reflow was not uniform, and likely had a dependence on the nonuniformity of the In and Al depositions, but this could be overcome with a better Al pad design or a multi-layer contact stack. These reflow parameters will depend on any contaminants at the Al-In interface and on the geometry of the Al pads, but this experiment demonstrates that this type of reflow is possible.

6 Patterning µm-Thick Superconducting In

Creating a superconducting indium flip-chip bump bond requires both the deposition and patterning of thick superconducting In. While the target feature sizes are large (10 µm reported in literature [1], 100 µm in this work), patterning µm-thick metal remains challenging.

Two approaches were taken for patterning and were pursued in parallel. We attempted lift-off lithography with both single-stack SPR and SPR+LOR double stacks. We also experimented with shadowmasking. The masks were fabricated in-house and ordered from low-cost PCB stencil manufacturers, and aligned to the wafer with a 3D printed custom jig.

At the time of writing this report, the SPR+LOR and shadowmask processes are both mature, with the SPR+LOR capable of better alignment and finer feature sizes.

6.1 Lift-Off Photolithography

The majority of Indium patterning in literature is performed with a combination of photolithography and lift-off processes. The patterning process includes, generally, coating the substrate with photoresist, and then exposing the resist stack, followed by developing in the appropriate chemicals to define the geometries. The sample can then be taken to metalization where the Indium gets deposited across the sample, some directly on the substrate and some on the resist. Then, by submerging the sample in the correct solvents, one could lift-off metals that are deposited on top of the resists which dissolve in the lift-off solution, leaving behind only desired geometry in Indium.

Lift-off-based lithography often suffers from inconsistency before the recipe is well-tuned. However, a good lift-off is still achievable, especially if the following features could be met

1. Resist thickness:metal thickness is at least $\approx$ 3:1.
2. Resist sidewall shows a negative profile or an overhang.

An additional project-specific restriction to the litho process is that we'd like to keep the bake temperatures low ($< 120\,^{\circ}\mathrm{C}$). This is because superconducting Josephson junctions anneal under high temperatures and could cause the characteristics of the fabricated devices to drift significantly from the designed target values.

We will discuss in detail in the following sections our explorations with 2 µm In lift-off with single-stack SPR 220-7 and with double-stack LOR 10B/SPR 3612. All samples are spun at the exfab spinner bench (headway3) and developed at the exfab developing bench (wbexfab_dev).

6.1.1 Spinning Single-Stack SPR 220-7

Part of the reason for developing a single-layer lift-off recipe based on SPR 220-7 is because the bake temperature of this resist is only 90 °C, as opposed to 180 °C for LOR. Additionally, SPR could be lifted with room-temperature acetone, simplifying the process furthermore.

The problem with single-layer lift-off with a positive resist, such as SPR 220-7, is that the sidewall often show a positive profile. This is simply an artifact of the exposure and development process of positive resists. Positive sidewalls are more prone to incomplete lift-offs dues to residual sidewall depositions but could be potentially mitigated by further increasing the resist-to-metal layer thickness ratio. In our case, we spin SPR 220-7 on silicon wafers, targeting 10 µm on a Headway manual resist spinner (headway3) following the corresponding recipe for SVG resist coat track (svgcoat):

1. Take the sample (mostly 4" wafer in our case) and solvent clean with 20 sec acetone spray, 20 sec IPA spray.
2. (Optional) sonicate (sonicator at wbexfab_solv) the sample with acetone for 5 min and then IPA for 5 min, at max strength.
3. Dehydration bake at 115 °C for 10 min, and then let the sample chill on tin foil (on spinner bench) for another 1 min.
4. From the center, dispense SPR 220-7 with a pipette or pour straight from the resist bottle to cover most of the sample area. Spin at 500 rpm with 4000 rpm/sec ramp for 0.5 sec, then 1700 rpm with 500 rpm/sec for 40 sec.
5. Check for edge beads and backside resist after unmounting the sample and clean with acetone if needed.
6. Bake at 90 °C for 100 sec, let cool for 60 sec, and then at 90 °C for another 200 sec.
7. Wait at least 8 h before writing the sample. Cleave or dice if needed.

This recipe is expected to coat the sample with 10 µm of SPR 220-7, and we verified a film of roughly 11 - 12 µm with profilometry (alphastep) and reflectometry (nanospec2).

6.1.2 Exposing and Developing Single-Stack SPR 220-7

We performed all of our exposure in a Heidelberg MLA 150 (heidelberg2) with laser wavelength of 375 nm. Exposing thick single-stack resist turned out to be quite challenging. The rule of thumb for lifting off thick resist stack is to overexpose just a little and also overdevelop 'just a little'. This is, however, a fine line to straddle between incomplete lift-off and delamination during developing. We were able to pattern our features generally truthfully (see Figure 19(a)). Other problems include focusing issues, exposure drift, and nitrogen bubbling from exposure with high doses. We show some of the failure modes in the following Figure 19(c), where you could see pattern drifting and what appears to be overexposure, despite that the exposure and development parameters are *strictly* the same as with the successful lift-off sample show in (a).

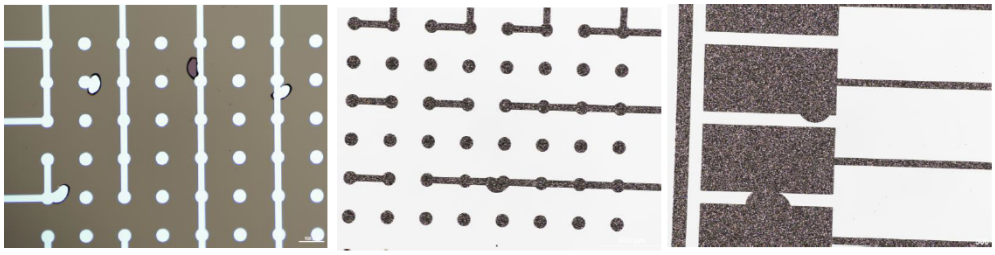
The main variables for this process are the dose, defocus, and developing time. After exploring the parameter space, we eventually settled for a consecutive high-dose triple exposure with no adjustment for defoc between writes for our 10 µm stack. The following images are taken with a sample written with a triple shot exposure using dose/defoc of 600 mJ/cm^2 and 0, and then developed in MF 26-A for 60 sec + 15 sec. After indium is deposited, the resist layer is lifted off with an overnight room-temperature acetone soak.

While this process works to first order, the consistency of exposure quality and sample yield is yet to be improved. During our discussion with other SNF users, it was brought to our notice that the total dose of our write is extraordinarily high and the developing time low. For future tune-ups, we'd like to keep this current set of parameters as a backup and go to lower doses and longer developing times in exchange for recipe robustness. Also note that a potentially better process is to iterate with exposure/developing as a whole unit, instead of multiple exposures followed by one single development. This way might give Heidelberg an easier time focusing on the *actual* plane of exposure and allows us to check pattern definition midway through, but would require alignment marks.

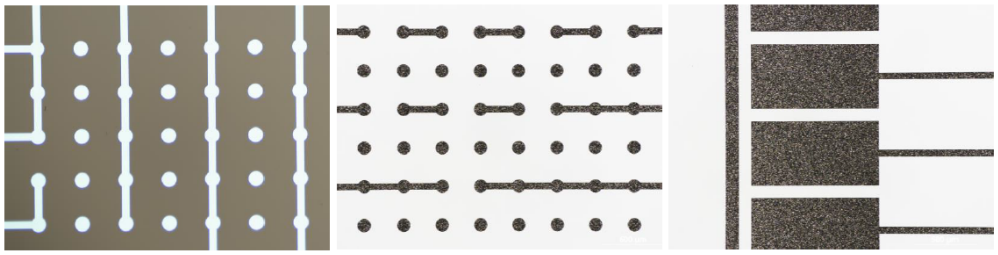
6.1.3 Spinning Double-Stack LOR 10B/SPR 3612

Although LOR traditionally requires a higher bake temperature (180 °C) than the junction annealing tolerance, we decided to try a LOR/SPR double stack as it's the standard lift-off stack and should have a higher success rate. To coat LOR 10B, we used the suggested spin speed, ramp, and time per the data sheet. The only adjustment was to tune down the bake temperature from 180 °C to 90 °C, while doubling the bake time from 5 min to 10 min. According to the LOR datasheet, the development speed would roughly triple as a result. To coat SPR 3612, we adapted a well-adjusted bilayer lift-off recipe widely used for patterning superconducting Al in our lab.

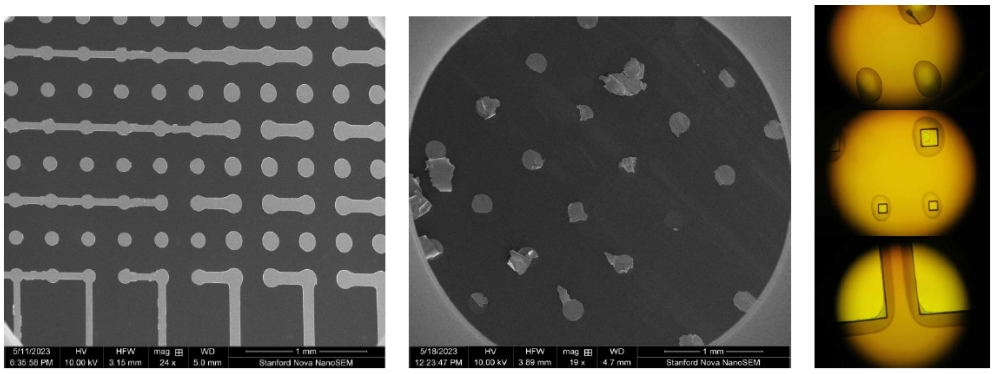
1. Take the sample (mostly 4" wafer in our case) and solvent clean with 20 sec acetone spray, 20 sec IPA spray.



(a) Optical microscope images of single-stack SPR 220-7 lift-off.



(b) Optical microscope images of double-stack LOR 10B/SPR 3612 lift-off.



(c) SEM and optical images of various failure modes with single-stack SPR 220-7 lift-off. From left to right: drifting in pattern, incomplete lift-off, and suspected overexposure.

Figure 19: Optical microscope images of photolitho lift-off results. 2 µm of indium (deposited in Innotec) is patterned via lift-off photolitho directly on silicon substrate

2. (Optional) sonicate (sonicator at wbexfab_solv) the sample with acetone for 5 min and then IPA for 5 min, at max strength.
3. Dehydration bake at 115 °C for 10 min, and then let the sample chill on tin foil (on spinner bench) for another 1 min.
4. From the center, dispense LOR 10B with a pipette or pour straight from the resist bottle. Make sure all area is covered. Spin at 500 rpm with 10000 rpm/sec ramp for 5 sec, then 2000 rpm with 10000 rpm/sec for 45 sec, then decelerate to 300 rpm with 10000 rpm/sec ramp for 0.5 sec.
5. Check for edge beads and backside resist after unmounting the sample and clean with acetone if needed.
6. Bake at 90 °C for 10 min, and let cool for 60 sec or however long it takes for the sample to thermalize back to room temperature. The steps above are expected to give $\sim 1\,\mu m$ of LOR 10B.
7. Repeat steps 4 - 6 a number of times until the desired height for LOR 10B is reached (4 times in total in our case).
8. Mount the sample onto the spinning chuck and blow away any particles on the surface. From the center, dispense SPR 3612 with a pipette or pour straight from the resist bottle to cover the majority of the sample area.
9. Spin at 1800 rpm with 1000 rpm/sec for 0.5 sec, 3600 rpm with 1000 rpm/sec for 0.5 sec, and finally at 5500 rpm with 1000 rpm/sec ramp for 40 sec. Decelerate to 2700 rpm with 1000 rpm/sec for 0.5 sec.
10. Bake at 90 °C for 1 min, and let cool for 60 sec. The second SPR 3612 coat is expected to be $\sim 1\,\mu m$ thick.

We verified 2000 rpm would give a single layer of LOR 10B of $\sim 1.4\,\mu m$ of with profilometry (alphastep) and reflectometry (nanospec2).

6.1.4 Exposing and Developing Double-Stack LOR 10B/SPR 3612

We also did a mini DOE for exposing and developing LOR 10B/SPR 3612. Essentially, the question is to lift off a much thicker layer, does the SPR stack need to be scaled too and if so, how would the exposure dose and developing time change. We soon realized that the SPR layer is only there to create a structural overhang, and if anything, should be thinner if the metalization is thicker to allow for overdeveloping of the LOR base stack. We eventually settled on following the SPR spin/exposure/develop number for the Al mask.

Images in Figure 19(b) are taken with a sample exposed in Heidelberg with dose 105 mJ/cm^2 and defocus -2, developed in MF 26-A for 30 + 30 + 10 sec. This bilayer lift-off recipe has worked relatively robustly. The next step would be to tune up the recipe with LOR 30B instead, which allows for single spin of thick LOR layer and could significantly accelerate the process.

6.1.5 Patterning Al with Bilayer LOL 2000/SPR 3612

To pattern the 200 nm Al base layer, we adapted arecipe which uses a slightly different spin stack of LOR 5A/SPR 3612. Here we substituted LOR 5A with LOL 2000 as both are designed for lift-off processes and spin similarly in terms of height profile. We adjusted the spin speed to aim for the same target height and adjusted develop time per LOL datasheet using a single MF-26A puddle, a DI water puddle, and running DI water rinse.

6.2 Shadowmasks

The simplest method to pattern metal on a wafer is by using a shadowmask: a sheet of material with patterned holes that is held on top of the wafer during metal deposition (Figure 20). This method can be used for arbitrarily thick depositions, provided that the material preferentially adheres to the wafer over the shadowmask. However, it is difficult to use shadowmasks for small features, as the shadowmask aperture must match the desired feature size, and as the shadowmask must be aligned to within a feature size with any underlying patterns. As we aimed for large features with coarse alignment, shadowmasks allowed for quick iteration of deposition recipes with standardized patterns.

6.2.1 Fabricating Shadowmasks On-Campus

Initial four-point tests required standardized geometry for repeatable estimations of film resistivity. The feature size was large (>1 mm), and so shadowmasks were fabricated using the Protomax CNC waterjet[2] available in the Stanford Product Realization Lab. The waterjet is a coarse instrument intended for cutting inch-thick pieces of material, and so is ill-suited for fine shadowmask fabrication. The finest feature size we were able to demonstrate was 1.5 mm on 100 µm thick steel sheet, limited by the aperture of the waterjet. An image of the resulting masks mounted on a 100 mm Si wafer is shown in Figure 21.

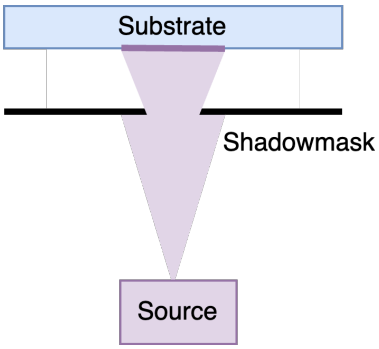


Figure 20: Cartoon of a shadowmask used in an e-beam evaporation. Features are defined by evaporated material passing through apertures in the mask.

Converting a .gds CAD file into a waterjet-cut steel sheet is a niche task, but one that may someday again prove useful, so the process is documented in the SOP below:

1. Open the .gds in KLayout, and export as a .DXF. DXF export is restricted to a single top sell, so ensure the CAD tree is compatible.
2. Open the .DXF in Inkscape, and save as a .DXF. Both the R12 and R14 revisions of the file type seem to work. This is a little convoluted, but is necessary due to some subtly incompatibilities of the file format between KLayout and the CNC control software.

[2] https://productrealization.stanford.edu/processes/waterjet-cutter

3. Process the .DXF as is described in the waterjet SOP[3], and prepare the waterjet until material load.

4. Tape or otherwise attach the sheet steel to a backing material. We used 5 mm MDF, but anything stiff will work. This is critical to prevent oscillations of the sheet steel which will clog the waterjet head.

5. Mount the sheet steel and backing material using as many clamps as possible as near as possible to the cut path, then proceed with the cut as normal.

6. After the cut is complete, spray down the shadowmask to remove excess garnet, and blow dry.

7. In the cleanroom, rinse the shadowmask in acetone, then sonicate for five minutes in isopropyl alcohol, then N_2 dry.

6.2.2 PCB Stencils as Shadowmasks

In later stages of the project, we needed to fabricate arrays of 100 µm bumps. These features are within the tolerances of PCB stencil vendors (we used OSHStencils[4]), who generally laser-cut stencils to 25 µm minimum aperture size. These stencils arrive as polished 100 µm-thick stainless steel, and are then cut to size using a sheet metal shearing machine. These are accessible in Lab64, the Product Realization Lab, and in machine shops across campus. However, PCB stencil vendors general accept Gerbers, the standard PCB file type, and conversion from GDS to Gerber is again nontrivial. An SOP for stencil generation is therefore provided below:

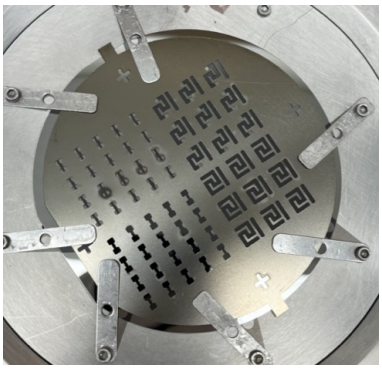


Figure 21: A waterjet shadowmask mounted on a 100 mm Si wafer prior to deposition in the KJL evaporator.

1. Open the .GDS in LayoutEditor. KLayout cannot generate universally compatible Gerber files, while LayoutEditor can. Ensure that one of the layers in the .GDS corresponds with the aperture layer in the shadowmask.

2. Save the design as a 'Gerber Including Load-Macro'. This exports a Gerber (.gdx)file for each layer in the design, as well as a '.gerber.layout' file, which can be ignored. While the free version of LayoutEditor may warn that a watermark be generated, this is not present in the exported file for the '20230301' version of the tool.

3. Choose the '.gdx' file corresponding to the shadowmask apertures. This file can be uploaded to a PCB stencil service of your choice.

[3]https://prl.sites.stanford.edu/sites/g/files/sbiybj21511/files/media/file/waterjet_cutter_instructions.pdf
[4]https://www.oshstencils.com

OSHStencils offers 25 µm minimum aperture sizes. The shape of an aperture at 25 µm is not guaranteed to be perfectly circular. However, optical microscope images revealed generally circular apertures at 100 µm, the size relevant for this project, with some surface scoring from the laser cutting process. A representative optical image is shown in Figure 22.

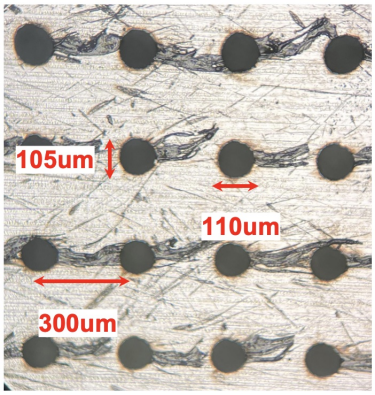


Figure 22: An annotated optical image of 100 µm holes in an OSHStencils shadowmask. Holes were 5 µm to 10 µm than as defined in CAD.

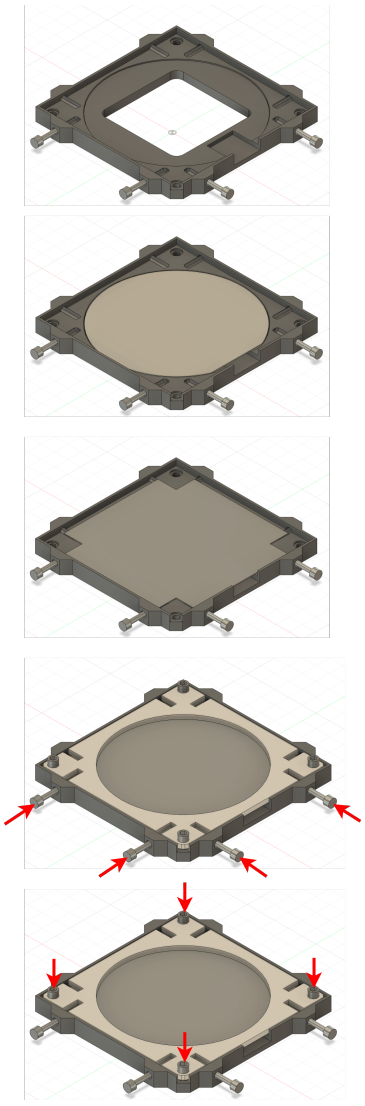
6.2.3 Aligning Shadowmasks to Pre-Existing Patterns

Shadowmasks were generally used for patterning indium bumps or bars on pre-existing aluminum patterns. It was therefore necessary to align the indium pattern to the aluminum. As the feature sizes used in this project are large, the target alignment tolerance was 10 µm, with a a maximum acceptable alignment tolerance of 25 µm. These tolerances are very coarse, and so unsophisticated alignment techniques provided satisfactory performance.

A prototype shadowmask alignment jig was designed and tested to meet 10 µm alignment tolerances on 100 mm wafers. The jig consists of a bottom plate, with a cutout matching the dimensions of the wafer, and adjustment screws to move the shadowmask relative to the wafer. A top plate then clamps the shadowmask against the wafer once alignment has been achieved. Cartoons of this process are shown in Figure 23, and a video of the process is available in a Nano Nugget. After alignment, the shadowmask must be secured to the wafer. We used small pieces of polyimide tape to do this, and we found this method durable to transfer of the shadowmask and wafer to the deposition tool.

A brief SOP is given below:

1. Clean particulates off of the top and bottom of the shadowmask jig with an N_2 gun.
2. Install alignment screws in the bottom shadowmask jig, ensuring that they do not protrude into the shadowmask cavity. We typically install eight screws, which overconstrains the shadowmask, but practically makes alignment easier.
3. Install the wafer in the cutout in the bottom shadowmask jig. About a millimeter of slop is expected. This is not an issue for alignment due to the relatively high coefficient of static friction between the wafer and jig.
4. Carefully place and coarse align the shadowmask on the wafer using tweezers.
5. Place the top plate of the shadowmask jig in the larger cutout, and install, but do not tighten the top screws.
6. Under a microscope, rotate the alignment screws until the shadowmask is aligned with features on the wafer. Try to avoid moving the shadowmask too much - it is in direct contact with the wafer, and so can scratch the surface.



0.3

Figure 23: Assembling the shadowmask jig and aligning the shadowmask to underlying features on the wafer (top to bottom). The red arrows denote adjustment of screw position.

7. When the shadowmask is aligned, tighten the top screws so the mask is locked to the wafer. Then remove the alignment screws.
8. Use pieces of polyimide tape, PMMA, or a similar adhesive to attach the shadowmask to the wafer for deposition.
9. Remove the top screws and the shadowmask-wafer assembly from the jig, and transfer to the deposition tool.

The shadowmask alignment jig was designed for FDM printing in PLA. Brass heat-set M3 inserts[5] were used along with 20 mm M3 bolts[6] to create the adjustment screw system for shadowmask alignment.

Many improvements are possible to this shadowmask alignment system. The most major weakness is that plastic plates cannot be cleaned in solvent, and therefore likely deposit organics on the wafer backside. Furthermore, the plastic plates outgas heavily and have a glass transition temperature of $\approx 70\,^{\circ}\mathrm{C}$, preventing direct installation of the alignment jig in an evaporator. Therefore, the shadowmask must be attached to the wafer with adhesive, which may lead to misalignment, and which introduces organics into the deposition. This can be solved by machining the jig out of aluminum or stainless steel, after which the entire shadowmask, wafer, and jig can be installed in a deposition tool. This also allows for spacers to be introduced into the design, which would prevent the shadowmask from coming into contact with the wafer surface. Additionally, the relatively large pitch (0.5 mm) of the M3 screw threads limits alignment precision. This is easily solved with fine-pitch alignment screws, such as those offered by Thorlabs[7].

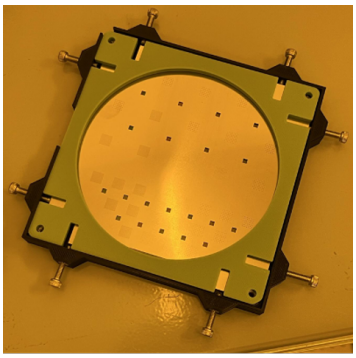
6.2.4 Shadowmask Patterning Results

Depositions with the shadowmask alignment jig provided alignment error between 10 µm and 25 µm, within the tolerances of our designs. Images from a shadowmasking flow providing 10 µm alignment are shown in Figure 24.

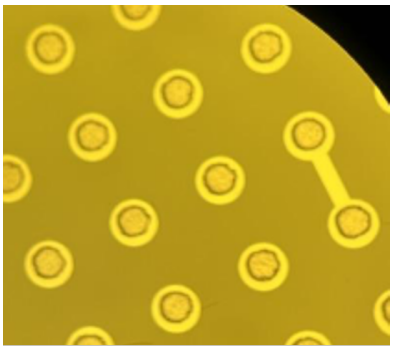
We observed three main issues with shadowmasked deposition of indium. The first is that the removal of the shadowmask can lead to damage as the aperture pulls on the deposited indium film. In cases where the shadowmask is lifted diagonally, rather than vertically, off the wafer surface, this damage can be extreme. A few examples are shown in Figure 25.

The second issue is that indium has a very high surface mobility, and so droplets migrate across the wafer surface during deposition. Surface mobility is increased as the temperature of the wafer increases, and so deposition without a cooled wafer mount leads to large indium diffusion from the aperture. This is the case for the Innotec evaporator, in which we observed indium droplets ≈ 40 µm from the edge of the bump (2 µm deposition, $20\,\mathrm{Å\,s^{-1}}$). In the KJL evaporator, where the wafer mount is water-cooled, indium diffusion was observed ≈ 10 µm from the bump edge with the same deposition parameters. Examples of indium diffusion in KJL and Innotec depositions are shown in Figure 26.

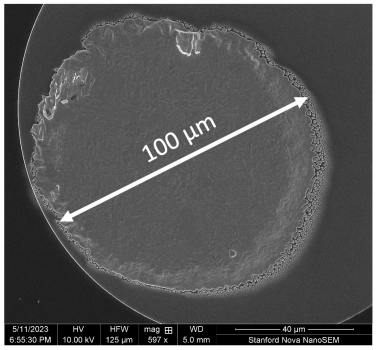
[5] https://www.amazon.com/dp/B08K38BFZB
[6] https://www.amazon.com/dp/B0714FLXND
[7] https://www.thorlabs.com/newgrouppage9.cfm?objectgroup_id=13987



(a) Shadowmask aligned with wafer in the alignment jig.

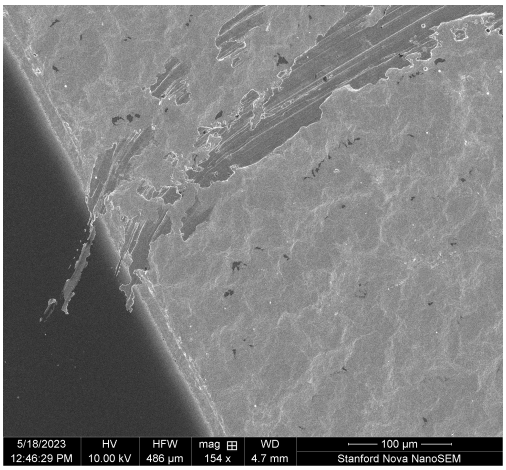


(b) Post-deposition optical image demonstrating $\approx$ 10 µm alignment.

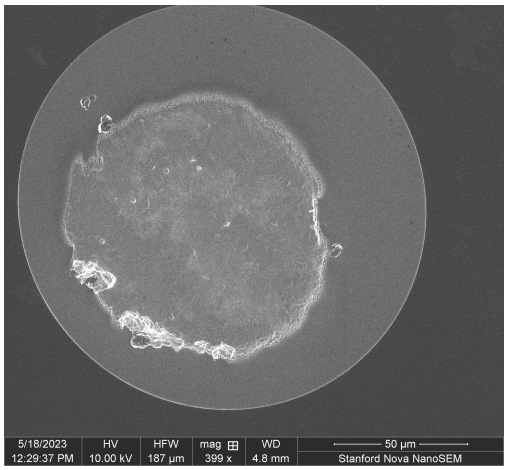


(c) SEM image of a indium bump deposited on an aluminum pad. The bump is $\approx$ 100 µm, the intended feature size.

Figure 24: Images taken during a shadowmasked indium deposition flow.

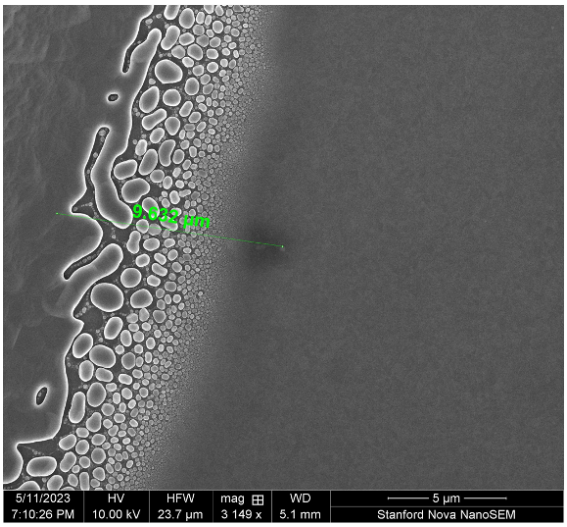


(a) A mm-scale scratch caused by shadowmask removal on a KJL-deposited indium film.

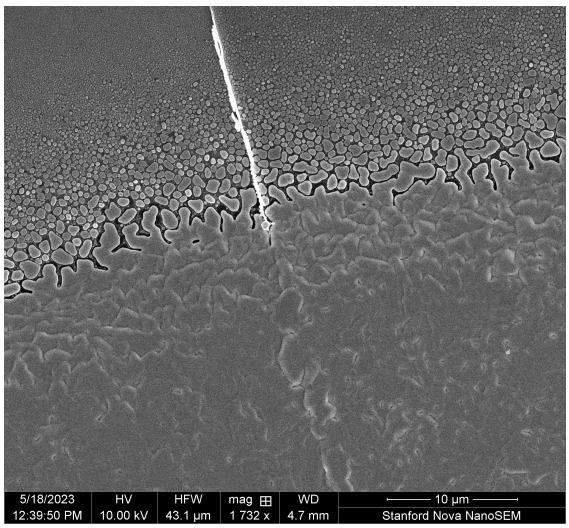


(b) Shadowmask-induced damage is visible on the bottom-left corner of a 100 µm bump deposited in the Innotec

Figure 25: Examples of damage to indium films occuring during shadowmask removal.



(a) Diffusion of indium in the KJL, captured with a scale bar of 5 µm. No indium islands were observed greater than 10 µm from the edge of the coherent film.



(b) Diffusion of indium in the Innotec, with a scale bar of 10 µm. Indium islands were observed up to 40 µm from the edge of the coherent film.

Figure 26: Indium diffusing from a coherent film into islands near feature edges during depositions in the KJL and Innotec. The length scale of this diffusion is much longer in the Innotec due to the increased deposition temperature and therefore increased surface mobility.

The high surface mobility of indium leads to soft feature edges - it is not possible to obtain sharp sidewalls, and brims of 5 µm to 10 µm surrounded the bump. This led the total size of the bump and brim to be 5 % to 10 % larger than intended. A representative SEM is shown in Figure 27.

The only real solution to creating sharper feature profiles would be to reduce the mobility of indium. This can be done two ways: by depositing an adhesion layer and by cooling the substrate. As discussed in previous sections, we were unable to develop an adhesion layer that was noticeably better than the bare Si/SiO_2 substrate surface, and we did not have access to a tool with a cooled wafer holder. **Indium diffusion may therefore be the ultimate restriction of feature size attainable with shadowmasking in SNF/SNSF**.

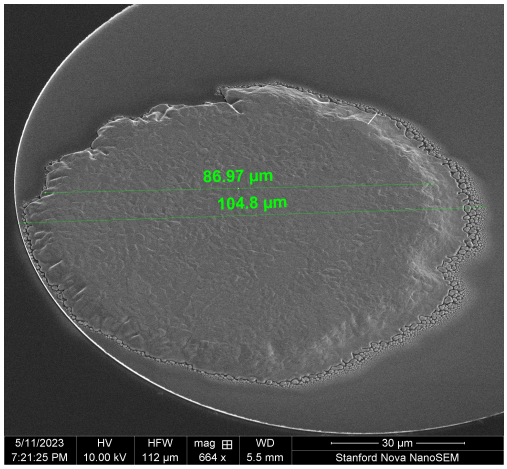
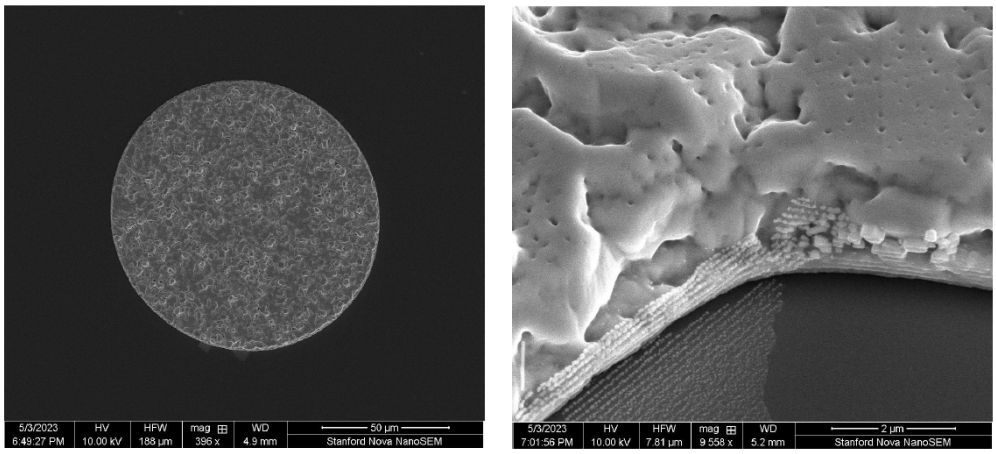
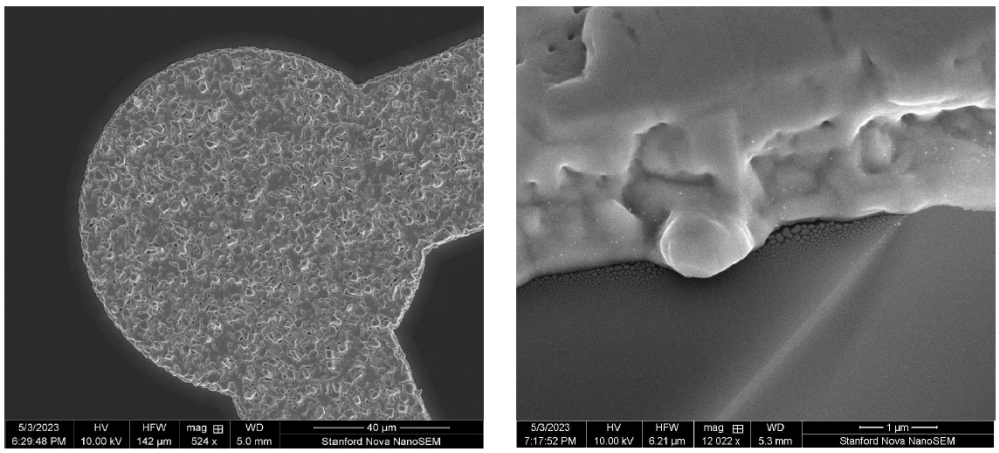


Figure 27: a 'top hat' profile is visible in shadowmasked depositions, due to the diffusion of indium during growth. The annotations here note that the 'brim' of this feature extends ≈ 10 µm beyond the central raised region.



(a) SEM images of single-stack SPR 220-7 lift-off. Notice on the silicon substrate the translucent film with periodically organized lines.



(b) SEM images of double-stack LOR 10B/SPR 3612 lift-off. Notice the tiny indium skirt around the pattern sidewall.

Figure 28: SEM images of photolitho lift-off results. 2 µm of indium (deposited in Innotec) is patterned via lift-off photolitho directly on silicon substrate

6.3 Summary and Comparison of Lift-Off Lithography and Shadowmasking for Indium Deposition

We'd like to include here a brief discussion on a comparison between lift-off-based photolithography and shadowmasking in Indium deposition. The photolitho method, having been more widely used and better adjusted, provides a much cleaner indium boundary with finer feature sizes. We show here SEM images of sidewalls and boundaries of patterned indium with both single and double-layer lift-off in Figure 28.

See that there are some periodic residual structures both along the sidewall and flat on the substrate. Our hypothesis is that these layer structures, formed during deposition, are thin layers of indium organized in small islands, clinging onto the resist film. During lift-off some

resist films delaminated vertically and eventually fell flat from the lack of structural support, creating this periodic film. This could be potentially taken care of with a blanket plasma clean or a gentle dry etch.

Compared to photolitho, shadowmasking completely bypasses the introduction of organics to the preexisting structures and platforms, including both the photoresists and the lift-off solvents (NMP or acetone). Additionally, shadowmasking drastically simplifies the patterning process as opposed to the spin/exposure/developing/lift-off cycle, allowing for fast turnarounds. These advantages all contributed to why we chose to pattern our test structures with shadowmasks. However, our current shadowmasking techniques inevitably damage the surface during mounting and deposition as our shadowmasks sit *directly* on the sample. Another limiting factor, which has been discussed extensively in the previous sections, is the thermal overspray of indium. This wouldn't be a problem with lift-off as the structure boundaries are defined during the exposure.

Going forward, we would like to keep parallelizing both photolitho and shadowmasking to balance between rapid process development and fine feature sizes.

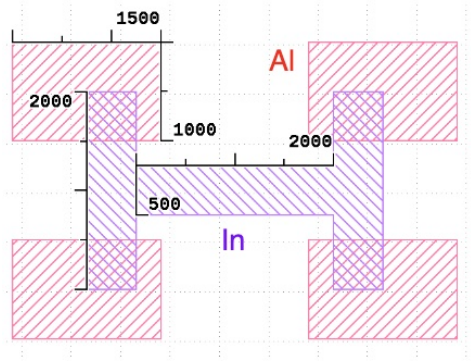
7 Overview of Test Structures and Electrical Characterization

This project aimed to develop a bump bonding system that provided superconductivity through bumps and bump-metal interfaces, and which is scalable to large arrays of bumps. We developed test structures that we could use to independently benchmark progress towards these goals. These generally fell into two categories: 'four-point' devices with large feature sizes that were used to characterize the electronic properties of the bump interconnects, and 'array' devices with smaller feature sizes that were used to benchmark patterning and to test bond yield.

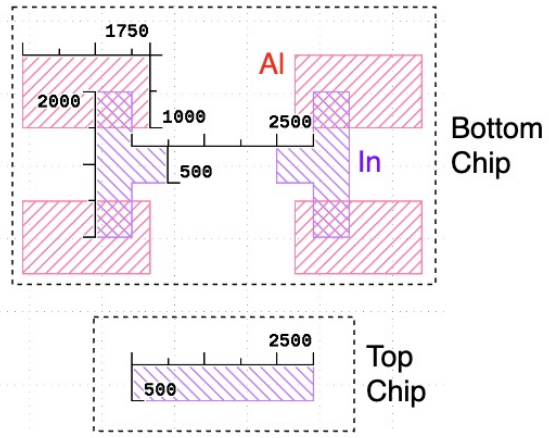
7.1 Four-Point Devices

All four-point devices consisted of an indium 'H' contacted by four aluminum pads. The smallest feature size was 500 µm, allowing for unsophisticated lithography and hand alignment of shadowmasks. These devices were developed in both planar and flip-chip versions, as is shown in the cartoon in Figure 4.

These devices were used to measure the electrical transport properties of the indium films, the In-In bump interface, and the In-Al interface. There were two types of electrical measurements: two-point and four-point DC IV sweeps were taken to characterize room-temperature film resistivity and to confirm ohmic behavior, and low-temperature measurements were taken to identify superconducting transitions. These controlled sample temperatures while probing resistances in four-point with a lock-in amplifier. Depending on the position of the source and sense leads, the resistivity of the In-In bump interface or the In-Al interface (both added to the resistivity of the In material itself) could be measured.



(a) CAD of a planar four-point device. The central 'bar' is 0.5 mm × 2 mm.



(b) CAD of a flip-chip four-point device. The top chip is cleaved and bonded to the bottom chip, providing a 'bar' of 0.5 mm × 2.5 mm.

Figure 29: CAD of planar and flip-chip devices.

7.1.1 Planar Devices

Initial electrical measurements of the indium films used planar devices, with the aluminum contacts defined through lift-off lithography or shadowmasks, and the indium contacts defined through shadowmasks. By the time the deposition recipe provided superconducting indium, the CAD for the four-point planar devices had matured, shown in Figure 29a.

A perfect four-point measurement of these devices (Figure 30) with an ideal current source and the voltmeter will provide $R_{xx} = K_{\text{geo}}(V_x^{\text{bar}}/I_x^{\text{bar}})$. Here, K_{geo} is some geometric factor very close to 1, due to for example y dependence on V_x^{bar}. As we are mostly interested in the proportional change in $R_{xx}(T)$, we assume $K_{\text{geo}} = 1$.

It is then possible to estimate the $R_{xx}(T = 273\,\text{K})$ from bulk resistivity values. $\rho_{\text{indium}} \approx 8 \times 10^{-6}\,\Omega\,\text{cm}$, so the central indium bar of the planar device will have resistance, where d is the indium film thickness in µm:

$$R_{xx}(T = 273\,\text{K}) \approx \frac{8 \times 10^{-6} \times 4}{d \times 1 \times 10^{-4}\,\text{cm}\,\mu\text{m}^{-1}}.$$

This provides $R_{xx}(T = 273\,\text{K}, d = 2\,\mu\text{m}) = 0.16\,\Omega$, and $R_{xx}(T = 273\,\text{K}, d = 200\,\text{nm}) = 1.6\,\Omega$, values comparable to what was observed experimentally. More

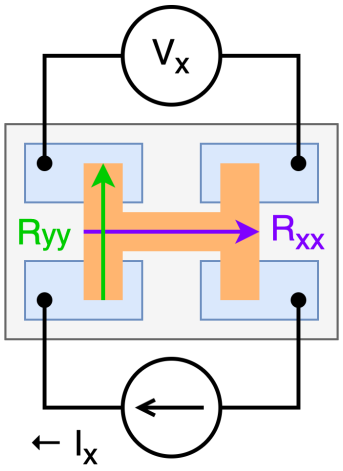
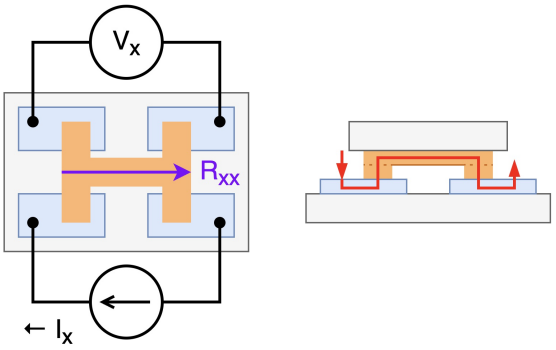
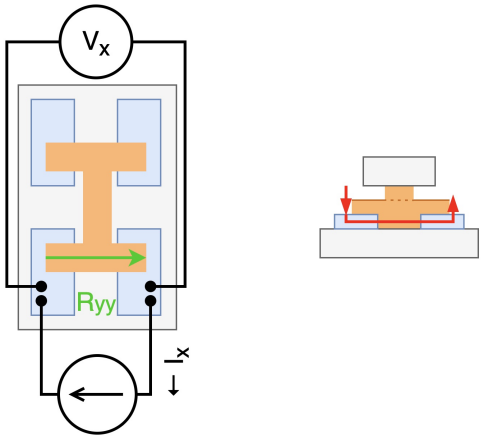


Figure 30: Example of a four-point resistance measurement. Current is applied across one pair of contacts, and the induced voltage is measured across the other pair. By changing the contact pairs R_{xx} and R_{yy} can be measured.



(a) Schematic of a four-point measurement across the flip-chip and bumps. The current path passes through both bumps, but the four-point measurement ignores the Al-In interface.



(b) Schematic of a four-point measurement across the aluminum contacts and indium. Here, the measurement includes the Al-In interface.

Figure 31: Schematics of four-point flip-chip device experiments.

experimental detail is given in Sections 5.2.4 and 8.1.3.

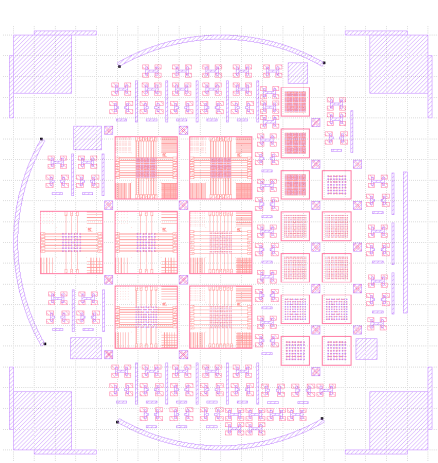
7.1.2 Flip-Chip Devices

A flip-chip variant of the four-point device allowed us to measure the electrical properties of the In-In bump interface. The CAD, shown in Figure 29b is broadly similar to that of the planar device. The central region of the bar, however, is present on a separate top chip, which is cleaved and flip-chip bonded to the bottom chip. The full top bar is slightly larger than on the planar devices, for an estimated $R_{xx}(T = 273\,\mathrm{K}, d = 2\,\mu\mathrm{m}) = 0.2\,\Omega$ assuming a single point of conduction for each bump.

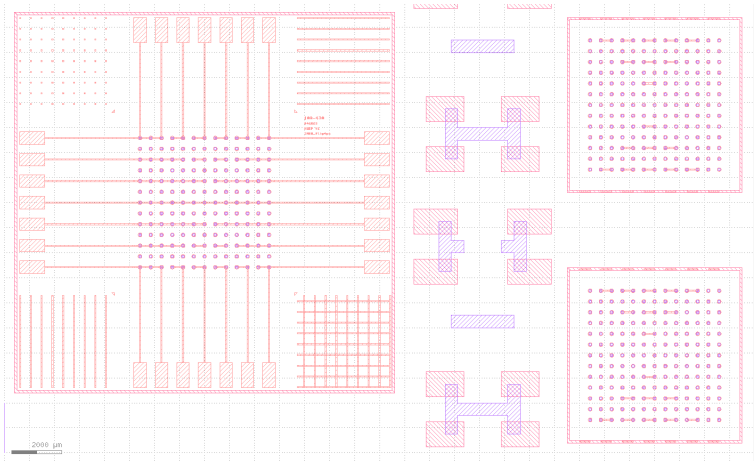
Two types of four-point cryogenic experiments were done, and are shown schematically in Figure 31. The first was identical to resistance measurements of the planar devices and measured R_{xx} through the top bar and bumps. This allows us to characterize the presence of the In-In bump interface. The second experiment measured R_{yy} through the aluminum pads and indium contacts, so the measurement captures the indium-aluminum interface.

7.2 Array Devices

Aside from the four-point devices, we also designed and fabricated bump-connection array devices. Inspired by the Google devices, the purpose of these is to give us a better understanding of the yield and bump quality of our process. When properly flip-chip bonded, the connection on the top and bottom chip should collectively form a close path from the left bond pad to the right. The quality of the individual connections in the top and bottom lines could be resolved with the breakout connections (see Fig.32).



(a) CAD of a wafer with mixed array and four-point devices fabricated.



(b) CAD of an example flip-chip array device.

Figure 32: Schematics of four-point flip-chip device experiments.

Among different geometric designs, We varied the size and separations of bumps in the array while keeping the fill-factor relatively constant. We experienced some difficulties in patterning the Al base layer of the denser patterns as the small separation between the bond pads sometimes results in breakage and shorting. We show here a wafer we fabricated with array devices spanning the bump size and separation parameter space. In general, the bump sizes are $\sim$ 100 - 200 µm in diameters and $\sim$ 500 - 1000 µm in separations.

8 Flip-Chip Bonding and Electrical Characterization

All flip-chip bonding was done in the Finetech Lambda in SNF ExFab at base temperature and with no ultrasonic force. While we have performed coarse scans of contact resistance over bond force, most of the flip-chip bonding parameter space remains unexplored.

8.1 Four-Point Devices

Several four-point devices from a shadowmasked 2 µm KJL indium deposition on lifted off aluminum were flip-chip bonded and characterized with DC IV sweeps and low-temperature AC resistance measurement.

In general, the four-point devices were bonded using the 2 mm × 2 mm × 1 mm bond head, using a 0.2 mm and 0.3 mm spacer washers to match the Finetech Lambda die height requirement. The temperature of the stage remained at 40 °C, the minimum temperature available, and no ultrasonic was used. We did not use any advanced features of the bonder, such as bond height adjustment, and so the bonding SOP remains simple:

1. Cleave or dice top and bottom chips. It is important that the top chip be cleaved as close as possible to the indium bar, such that excess wafer material does not obstruct

the Al contacts of the bottom chip.

2. Set up the flip-chip bonder with the 2 mm × 2 mm × 1 mm bond head.
3. Load a dummy piece of wafer onto the bonder base stage such that the unpolished side faces towards the bond head. This helps to prevent the indium from cold-welding to the wafer surface if pressure is accidentally applied. Turn on the base vacuum.
4. Load the top chip face-down onto the dummy wafer, and pick it up using the bond head vacuum.
5. Turn off base vacuum and replace the dummy wafer with the bottom chip, then turn the vacuum back on.
6. Use the cameras to coarsely align the top and bottom chips, then precisely align with micrometers, as shown in Figure 33.
7. Set the bond force to the desired value, lower with the coarse arm, and rest the top chip on the bottom chip for 60 s. This is an arbitrary time value - as is demonstrated later, bonding occurs immediately on contact.
8. Turn off vacuum, raise the bonding arm, and remove the bonded assembly.

Several other experiments aimed to improve the quality of the Al-In contact interface through annealing, obtaining contact resistance indistinguishable from the four-point resistance of the indium bar.

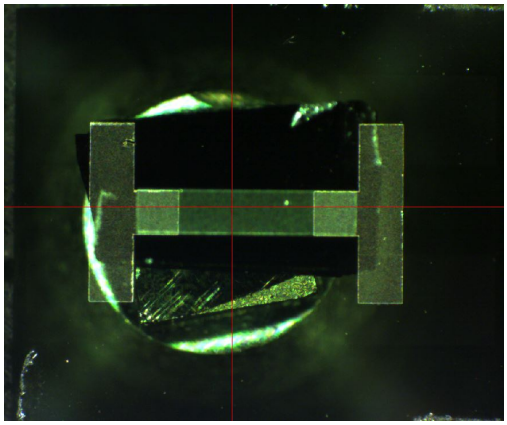


Figure 33: Top chip aligned on the bottom chip before flip-chip bonding. Image taken using the Finetech Lambda camera and beamsplitter system.

8.1.1 Bond Force Process Window

The process window for flip-chip bonding is extremely large. Successful bonds were observed for practically all sets of bond conditions, provided force is $> 10\,\mathrm{N}$, or $> 20\,\mathrm{N\,mm^{-2}}$. The time-response of bonding was also characterized by measuring two-point resistance across the bar during the bond, using the experimental setup and described in Section 10.4. This resistance was tracked (Figure 34) during initial bonding at $1\,\mathrm{N}$ ($2\,\mathrm{N\,mm^{-2}}$), and then when bond force was instantaneously increased to $10\,\mathrm{N}$ ($20\,\mathrm{N\,mm^{-2}}$). The drop in resistance occurred over $< 200\,\mathrm{ms}$, the sampling interval of the ohmmeter, as the indium likely instantaneously cold-welds to itself. Note that larger bond forces produced no change in bond resistance.

8.1.2 Bond Annealing

In parallel with the In-Al interface anneal described in Section 5.3.1, we explored an anneal of the indium-indium bump interface. However, we found that a post-bond anneal under

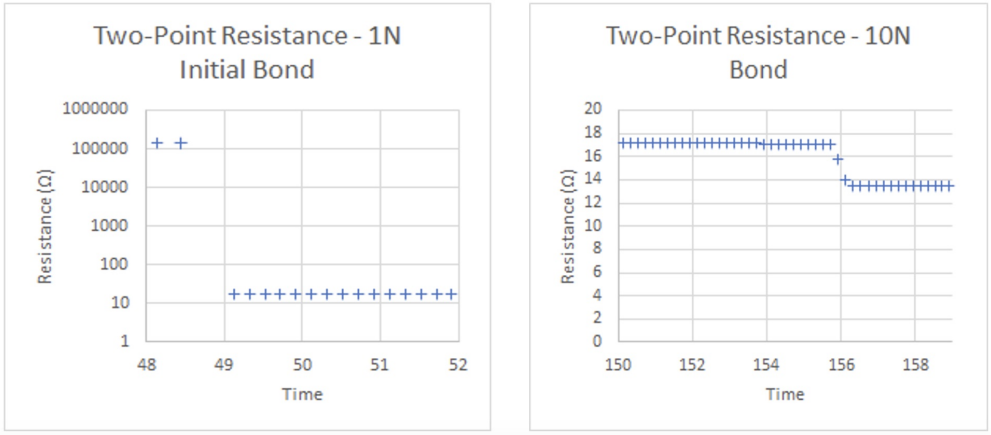


Figure 34: Bond resistance during an initial 1 N bond, followed by an increase in force from 1 N $\rightarrow$ 10 N.

the same conditions (N_2H_2, 250 °C, 120 s) increased resistance through the bump bonds and indium bar (Figure 35). The mechanism here is not well understood, and this was tested only on a single device, so it is worthy of further study. The increase in resistance could, for example, be due to wicking of the indium from the bar to the bumps, leading to bar area with very low film thickness, rather than degradation of the bond interface itself.

8.1.3 Packaging and Full Flip-Chip Superconductivity

Flip-chip bonding provides low-resistance bumps, justifying low-temperature electrical transport measurements to search for a superconducting transition. The device was therefore packaged and brought to low temperature in three experiments, which demonstrated superconducting transitions through the indium-indium bump interface and the aluminum-indium contact interface.

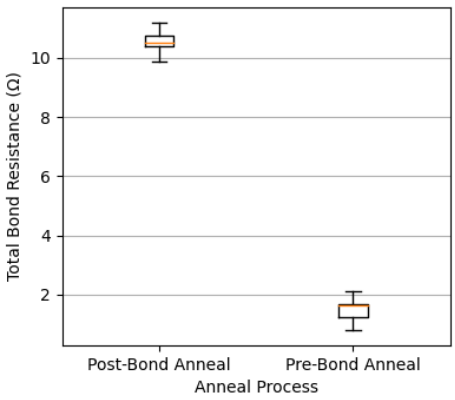
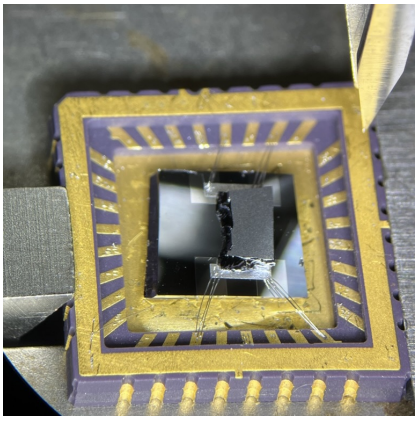


Figure 35: Four-point (through-bump) resistance is greater for the post-bond annealed device than for the pre-bond annealed device.

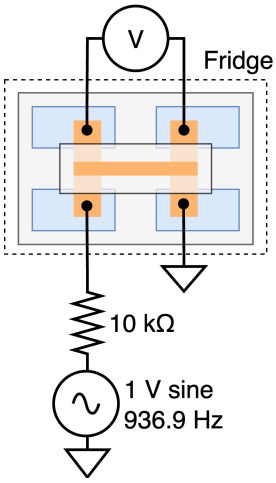
Temperature Sweep from 300 K $\rightarrow$ 1.4 K: Bump Characterization

The device was packaged into a chip carrier with aluminum wirebonds (Figure 36a). The four-point bar+bump resistance after bonding was found to be $R_{xx}(T = 300\,\mathrm{K}) \approx 0.16\,\Omega$, validating the bulk resistivity estimate.

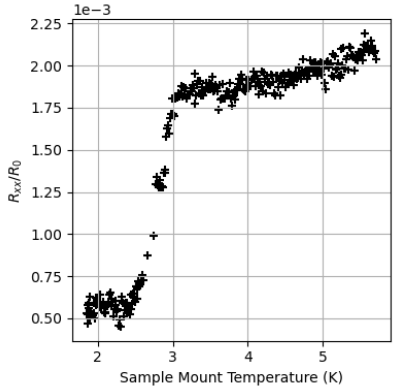
The device was then cooled down in the Goldhaber-Gordon group cryostat, with the cooldown again led by Aaron Sharpe and Sandesh Kalantre. A temperature sweep around base temperature revealed a su-



(a) Packaged flip-chip device after wirebonding.



(b) A schematic of the four-point through-bump resistivity experiment.



(c) R/R of the preannealed flip-chip device cooled to 1.4 K.

Figure 36: The device, measurement setup, and results of the 1.4 K flip-chip device cooldown.

perconducting transition near $T_c = 3\,\mathrm{K}$ (Figure 36c), corresponding to a superconducting transition in the indium film. All measurements were done with a SR830 lock-in amplifier providing bias current through a 10 kΩ load resistor (Figure 36b).

There was strong frequency dependence to the measured low-temperature voltage, signifying that complex impedances in the measurement chain added to the measured resistance, and that the intrinsic $R_{300\,\mathrm{K}}/R_{1.4\,\mathrm{K}}$ may be larger than the observed $R_{300\,\mathrm{K}}/R_{1.4\,\mathrm{K}} \approx 1 \times 10^4$. Regardless, the presence of this transition was sufficient for us to proceed to lower-temperature experiments.

Temperature Sweep from 300 K → 10 mK: Bump Characterization

We wire-bonded the pre-anneal four-point device onto a PCB suitable for measurements in a Safavi-Naeini lab dilution refrigerator (Figure 37), and measured resistance through the indium bump and bars as we swept from room temperature to a base temperature of 20 mK. Notably, the room-temperature four-point resistance remained at $R_{xx}(T = 300\,\mathrm{K}) \approx 0.2\,\Omega$, suggesting little mechanical damage due to the temperature cycling of the prior experiment.

During the cooldown, two superconducting transitions were observed, around the literature T_c of indium and aluminum. Some temperature offset is ex-

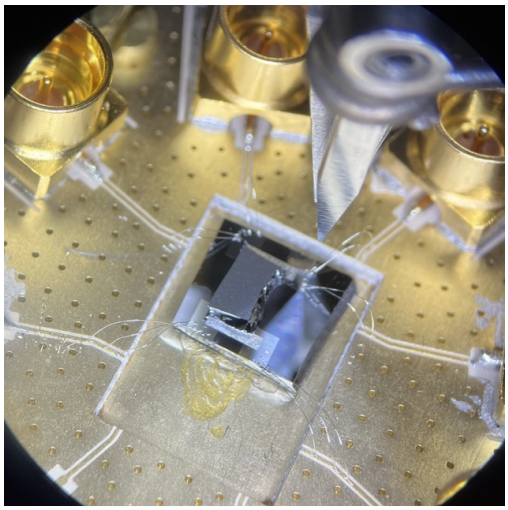


Figure 37: The packaged flip-chip device for dilution refrigerator measurement

pected due to the phase lag in temperature between the temperature sensor and the sample itself. The presence of the aluminum phase transition was unexpected, as an ideal four-point measurement would fully separate the contacts from the indium bar and bumps. It is plausible that damage to the film or contacts drove some current through the aluminum, or that some other interface in the system sees a superconducting transition near the T_c of aluminum.

As with the 1.4 K experiments, all measurements were done with an SR830 lock-in amplifier. However, the current bias is now provided by a low-pass filter that provides a 400 Ω impedance at DC, and a cutoff of 40 kHz. This helps to suppress high-frequency leakage into the fridge. Furthermore, all non-superconducting lines have low-pass filters with cutoff frequencies of ≈ 1 kHz, restricting lock-in modulation frequencies.

The low-temperature resistivity measured during the temperature sweep is strongly dependent on the kinetic inductance of the superconducting (NbTi) cable used as a voltage sense line (Figure 38a): this is supported by the large increase in phase around the T_c of NbTi (Figure 38b), and the drop to $R_{300\,\mathrm{K}}/R_{10\,\mathrm{mK}} \approx 1 \times 10^4$ after rewiring the voltage sense lines to use non-superconducting lines (Figure 38c,38d). The remaining impedance may be dominated by noise power at the lock-in frequency, or by other complex impedances in the system. This is supported by the lack of temperature dependence on the resistivity below the aluminum transition temperature, in which a non-superconducting system should display some temperature response.

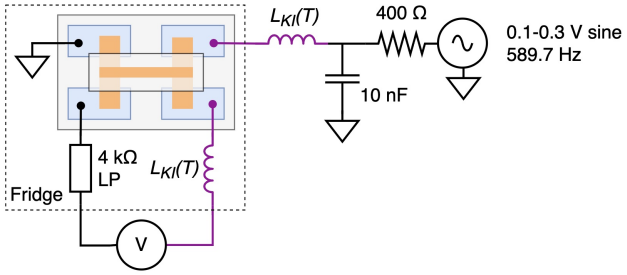
This experiment supported the 1.4 K observation of superconductivity through the bumps, and demonstrate a second phase transition in the system.

Temperature Sweep from 10 mK → 300 K: In-Al Interface Characterization

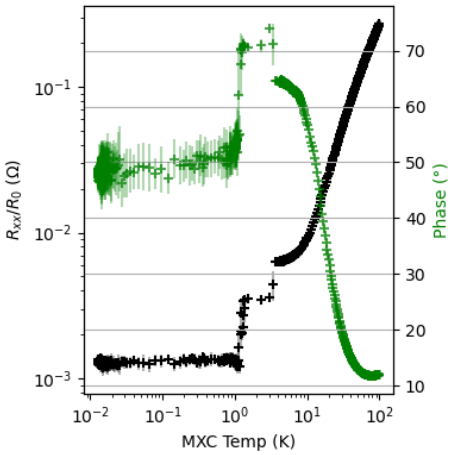
During the warm-up (from 10 mK → 300 K) of the preannealed four-point flip-chip device, we measured the four-point resistance across the indium-aluminum interface (Figure 39a). No superconducting lines were used for voltage sensing in this measurement, so the resistivity data is limited only by noise power and residual complex impedance.

Dilution refrigerator warm-up consists of several discrete steps, with no guarantees of linear temperature rise or even of monotonicity. The $R_{xx}(T)$ data (Figure 39b) is therefore spotty, but still displays a clear superconducting transition. at a fridge temperature of ≈ 1 K. As with prior experiments, $R_{300\,\mathrm{K}}/R_{10\,\mathrm{mK}} \approx 1 \times 10^4$. Given the complicated time dependence of temperature in fridge warm-up, the corresponding sample temperature at the phase transition is unknown. However, the most likely candidate for this transition is the aluminum contacts or indium pads - which could be resolved in a monotonic cooldown experiment.

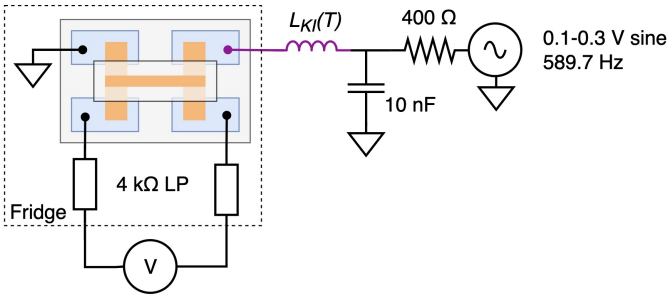
This experiment showed superconductivity through the aluminum pads. As superconductivity was also observed through bumps and in bulk indium, we have confidence that the bump bond system superconducts from contact to contact.



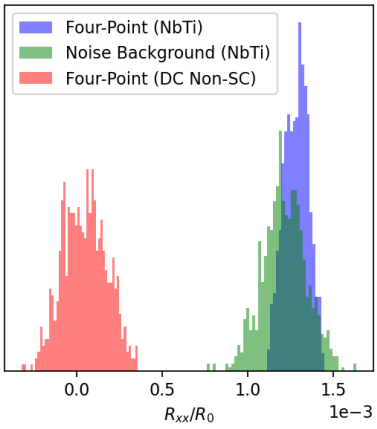
(a) The dilution refrigerator through-bump four-point measurement schematic during the cooldown. Here, $L_{KI}(T)$ represents the kinetic inductance of the superconducting cables (purple).



(b) R/R and phase response sweep from 100 K to 10 mK. Two superconducting transitions are visible. Note the large increase in phase near the T_c of NbTi cable.

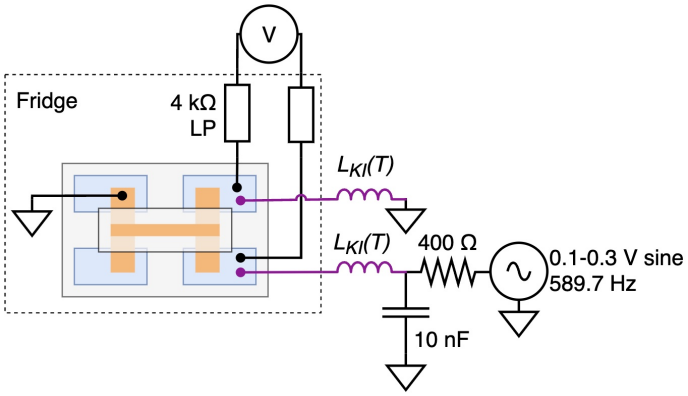


(c) The experiment setup after rewiring. Here, the superconducting cables have been removed from the sense leads.

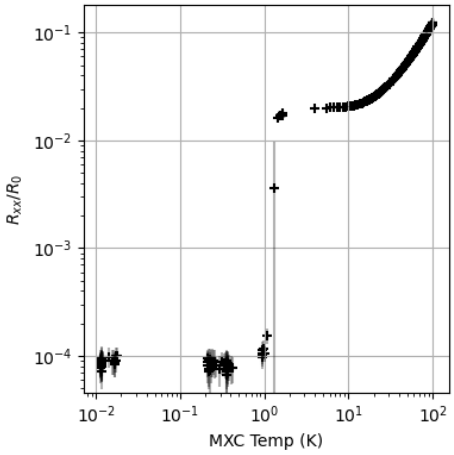


(d) Histograms of resistance data that illustrate measured impedance at base temperature pre-rewire, post-rewire, and across the superconducting cable. We see that impedance is dominated by the cable.

Figure 38: Measurement setup and experiments during the 20 mK cooldown of the flip-chip sample.



(a) The dilution refrigerator through-contact four-point measurement schematic during the warm-up. Note that no sense contacts were routed through the superconducting cable, avoiding kinetic inductance contributions.



(b) R/R sweep from 10 mK to 100 K, with one superconducting transition visible.

Figure 39: Measurement setup and experiments during the 20 mK cooldown of the flip-chip sample.

8.2 Array Devices

All array devices tested were fabricated with the combination of shadowmasking and Innotec indium deposition. We note that the quality of the film may not be up for cryogenic tests and characterized the devices under room temperature.

8.2.1 Bond Force Process Window

The process window for array devices is a little more restricted compared to the four-point devices. Successful bonds were observed when the maximum force on the standard arm (20 $\mathrm{N \cdot mm^2}$) is applied with a few (3 - 5) additional taps to further assist the bonding. We were able to achieve temporary bonding success with lower forces before some chip pairs break apart. We also experimented with heating and sending in ultrasonic pulses (power/pulse length: 100, 1000 ms). We observed no significant improvement with these assisting features. Specifically, samples where bonds were not able to form remain unbonded with heating and ultrasonoics. We'd like to note that it's empirically discouraged to send strong ultrasonics through indium, as the metal is extremely soft and could disintegrate easily.

We evaluated the bonding with two criteria: mechanical integrity and electrical connections. The mechanical soundness could be tested by

1. *Not* release the top chip arm vacuum after bonding and see if the top chip remains bonded to the bottom chip without being moved by the vacuum, and/or
2. After bonding, unmount the chip and turn it upside down to see if the bonds could

hold the weight of the top chip.

We characterized the electrical connection under room temperature by probing with a multimeter under resistance mode at the bond pads.

Across all seven pairs of bottom and top chip pairs that we fabricated for this test run, one of them (large, sparse bump design) was used as an initial test structure and remained unbondable and unbonded. All other six passed our initial mechanical test, although one of them, after roughly one week of aging, popped off during handling. Note that the actual bonding force might be lower or higher than the intended, as the filp-chip bonder was experiencing some top chip stage alignment issues at the time of the test, and the only way to ensure full contact between chips is to jam the stage into each other. A future objective is to develop a robust process and sensible rubric for evaluating the bonding quality, with the secondary goal to recycle bonding samples.

8.2.2 Bond Yield

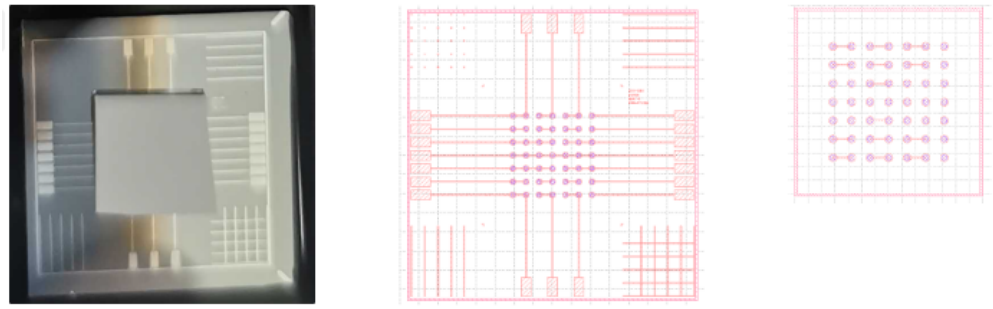
Out of all six successfully bonded samples, we tested three, all with distinct geometries, for bump bonding yield. The other three are saved for more future characterizations with a more rigorous scheme involving wirebonds. A problem with the current testing setup us that the multimeter pens tend to damage the thin aluminum contact layer and result in fluctuating or drifting measurements.

We observe from the electrical tests that a through Al connection is around 25 - 30 Ω, a through In-In connection is around 50-150 kΩ, while an open In-In connection is on the order of MΩ. These numbers are obtained by resolving the top and bottom lines on each chip. Because the ohmic measurements are orders of magnitude parts, we were able to use these values to back out the number of functioning connections in each line. Across all three test devices, we report 11/14, 13/18, and 10/20 success rates, which range from roughly 50% to 80%. Figure 40 below shows the test structures.

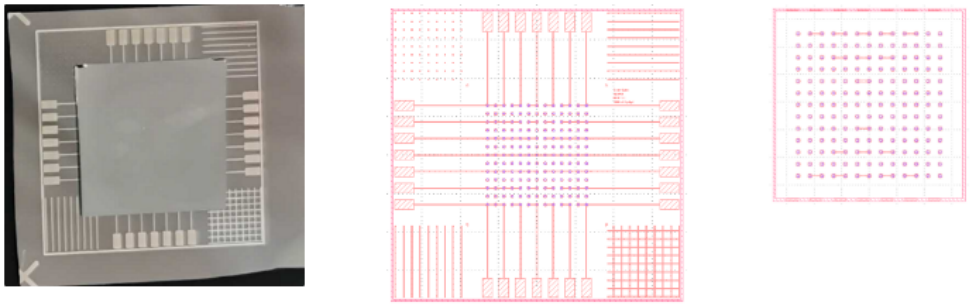
9 Discussion and Next Steps

Compiling all previous results, we've generally established a working process flow for patterning superconducting indium connections between Al-based chips. Note that the cryogenic characterizations were conducted at very low frequency (approaching DC), so a natural next step is to study the behavior of indium bumps at RF frequencies and learn how they affect the performances of the devices fabricated underneath. This would involve patterning indium bumps around superconducting Al resonators and measuring their frequency responses. Depending on the results, it may turn out that we need a UBM after all even tho In on Al directly proved to superconduct at around DC.

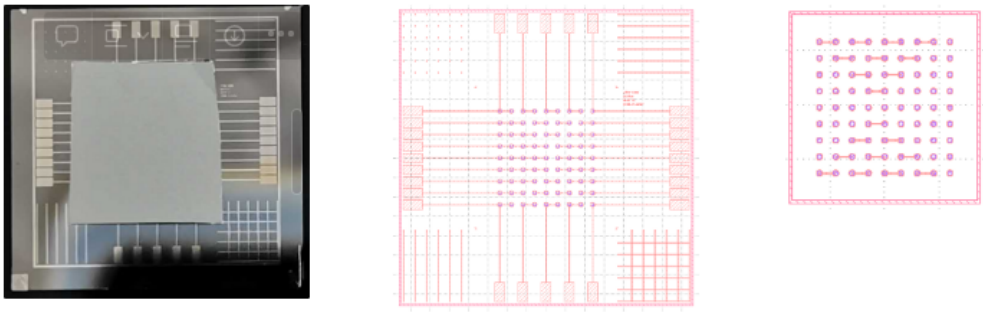
Going forward, another potential issue we might encounter is the mismatch between thermal expansions of different materials. Consider a flip-chip device with different coefficients of thermal expansion (CTE), bonded with indium bumps. During cool-downs or warm-ups, the chips will experience shrinking or expanding at different rates, creating a planar displacement



(a) Test devices with 14 In-In connections in total, out of which 11 are closed.



(b) Test devices with 18 In-In connections in total, out of which 13 are closed.



(c) Test devices with 20 In-In connections in total, out of which 10 are closed.

Figure 40: Photo and CAD of flip-chip bump array test devices. From left to right: photo after bonding, CAD of the bottom chip, CAD of the top chip.

between pre-aligned bumps. If large enough, the displacements might shear open the indium connections.

In terms of the patterning steps, we'd like to tune up the photolitho processes to the point that we can resolve $\sim 10\,\mu m$ leven features consistently across fabrications. We'd also like to improve the current shadowmask alignment scheme, potentially switching from 3D printed structures to machined parts to help with stabilizing and securing the masks with respect to the wafers. This could reduce the shearing and other damages caused by the mounting/unmounting process.

10 Appendix

The main sections of this report cover the essential fabrication and characterization involved in this project. However, these steps required additional technical work that may not be useful to future bump bonding projects. In the interest of completeness, this work is documented in this appendix.

10.1 Shadowmask Alignment Fixture

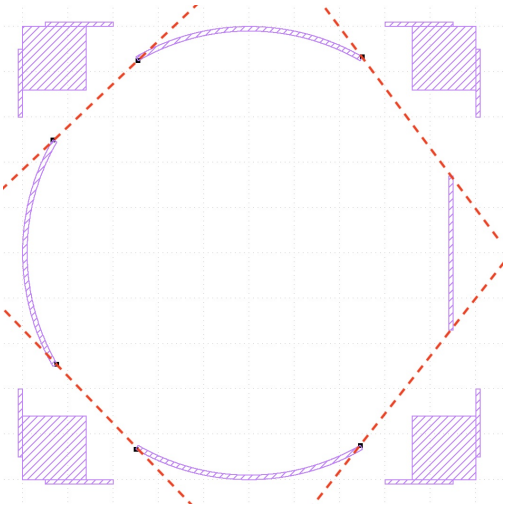
While our shadowmask alignment tolerance was coarse, at a maximum of $25\,\mu m$, it was still unfeasible to do alignment entirely by hand. This drove us to develop a simple 3D printed shadowmask alignment jig, as is described in Section 6.2.3.

Here, we document how to build one of these jigs:

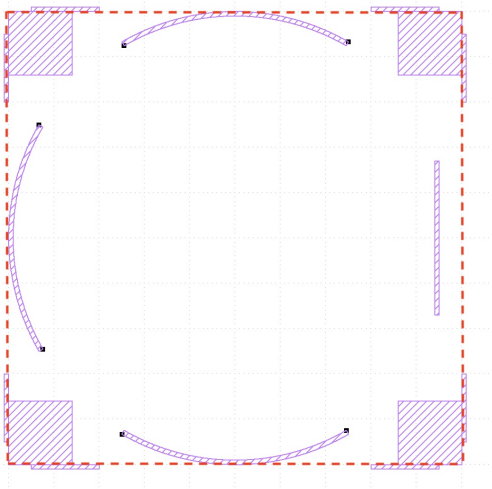
1. Print the top and bottom pieces out of PLA with $100\,\%$ infill and no supports. We used the Prusa i3 Mk3 FDM printers available in Lab64.
2. File down any sharp edges on the prints, clean with DI water, and blow-dry with an N_2 gun.
3. Install the heat-set M3 inserts with a soldering iron. We used a clean conical tip resting inside the insert, with the iron temperature set to $150\,^\circ C$. Ensure that the inserts are inserted until they are level with the outer surface of the bottom plate. Similarly, ensure that the inserts are installed straight (normal to the installation plne).
4. File down the ends of the M3 screws, rinse, and sonicate if necessary. Without filing, residual threads on the end of the screw may 'catch' on the edge of the shadowmask, making it difficult to do small adjustments to the shadowmask position.
5. Test fit the top plate and bottom piece of the jig, and ensure that all screws can be installed in the inserts.

CAD for the shadowmask jig has been uploaded to Google Drive in .stl format[8][9].

[8] https://drive.google.com/file/d/1VC9N-1N8OZ_fpsCOpKNiu27ElE7S31Dk/view?usp=sharing
[9] https://drive.google.com/file/d/1Uno1qBYwek9lR4ue8RAu7t0-DyR4C8yJ/view?usp=sharing



(a) Innotec shadowmask cut locations. The entire shadowmask remains within the boundaries of the 100 mm wafer.



(b) Cut locations for the KJL. Here, tabs are left for simple shadowmask alignment with the jig adjustment screws.

Figure 41: Shadowmask cut locations shown in red for the KJL and Innotec shadowmasks.

10.2 Ordering PCB Stencils

While earlier sections described the process of converting a GDS file into a Gerber file suitable for PCB stencil production, the shadowmask jig that we developed requires a specific profile for alignment with the adjustment screws, which is available in .GDS format on Google Drive [10]. These are negative files, so the shaded polygons are removed by the shadowmask production house.

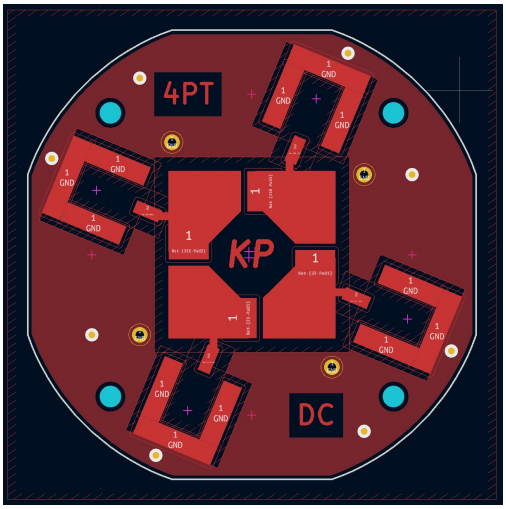
It is possible to then cut along the edges of the mask, using scissors or a shearing tool, to reach the correct profile. For depositions in the Innotec, the shadowmask must fit within the profile of a 100 mm wafer, and so must be trimmed differential. These cuts are shown graphically in Figure 41.

OSHStencils returned shadowmasks in 3-4 days, including shipping, for $50 per mask. The cost per mask decreased to about $30 per mask in quantities of two or three.

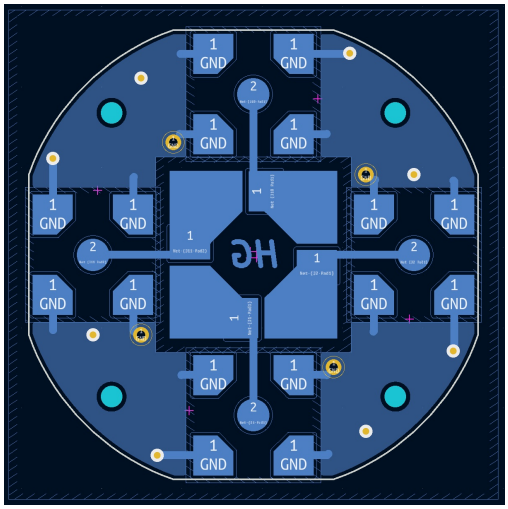
10.3 Four-Point PCB Designs

PCBs compatible with the Safavi-Naeini and Schuster Group dilution refrigerators were designed for this project. They provide a large wirebondable area of 10 mm by 10 mm with four bond pads. On one side of the PCB, these are broken out to surface-mount SMP connectors. On the other side of the PCB, these are broken out to surface-mount SMA connectors (Figure 42). The PCB geometry and mounting hole locations are designed for the packaging typical for the Safavi-Naeini group, but may be adaptable to other projects.

[10] https://drive.google.com/file/d/1qc05Mq4G0mlXiuPnTeQFGJruUi-2PB6o/view?usp=drive_link



(a) Front copper of the four-point PCB, with footprints for SMP connectors.



(b) Back copper of the four-point PCB, with footprints for SMA connectors.

Figure 42: Images of the front and back copper layers of the four-point PCB.

The KiCAD design files and Gerber files for PCB production are available on Google Drive[11]. 25 PCBs were ordered from JLCPCB with a 0.6 mm substrate and ENIG surface finish for about $1 per PCB.

10.4 In-Situ Flip-Chip Bond Characterization

While optimizing the flip-chip bond parameters, we measured two-point resistivity through the bottom chip while increasing bond force. This capability is not natively available in the Finetech Lambda - instead, a four-point PCB was modified such that a wirebonded chip matches the height restriction on the Finetech Lambda. A hole was drilled in the PCB, and 100 µm stainless steel backing plate was installed. The chip was then glued the backing plate, such that its top surface was approximately level with the PCB surface. A standard two-point ohmmeter (current source, voltage measurement) then measured the resistance of the sample.

A schematic of this setup is shown in Figure 43, and some images are shown in Figure 44.

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[1] Foxen, B., et al. “Qubit compatible superconducting interconnects”. Quantum Science and Technology, 3(1), 014005 (2017).

[2] Mo, Zhao-Hong, et al. “Superconductivity of bilayer titanium/indium thin film grown on SiO_2/Si (001)”, Chinese Physics B 27, 6 (2018).

[3] Rohe, T. et al. “Indium Bumping at PSI”, 2008.

[11] https://drive.google.com/file/d/12SJ-cYPHTSs2qaFQt5YYPssXFcO62OoM/view?usp=sharing

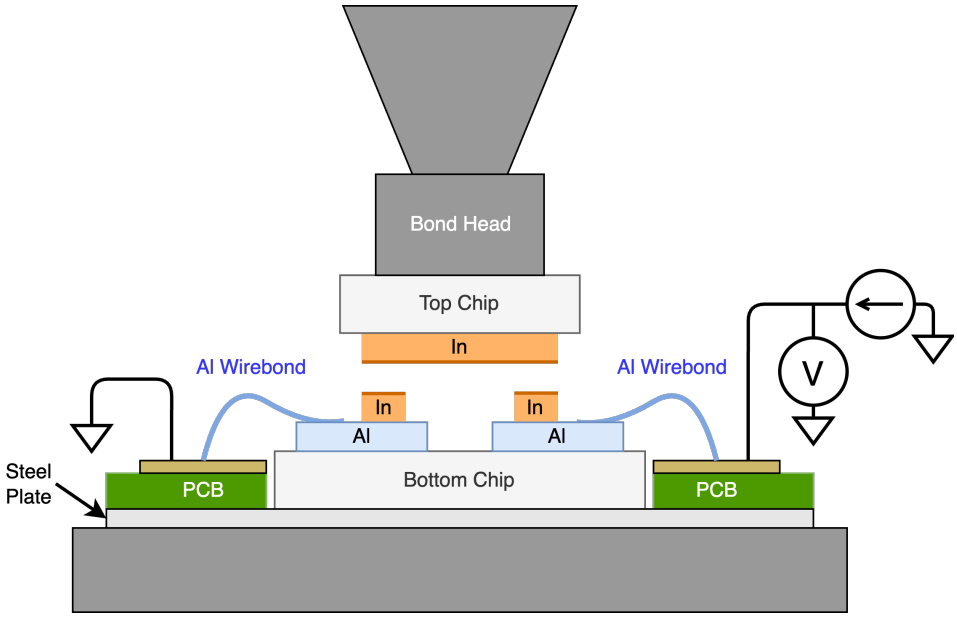
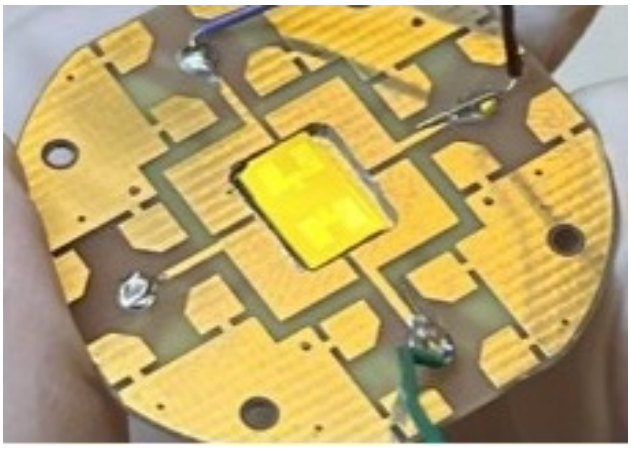
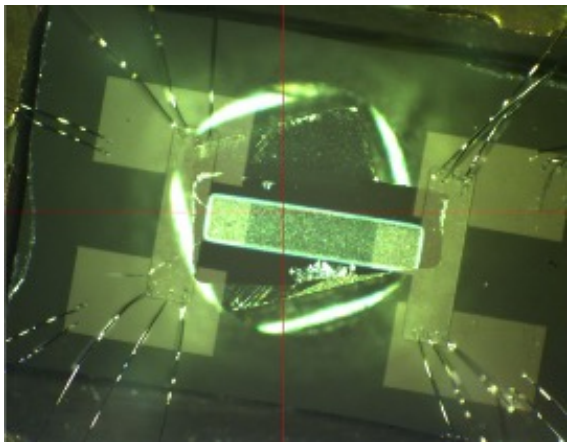


Figure 43: Experimental setup for resistance measurement during bonding.



(a) Bottom four-point chip in PCB cutout prior to bonding.



(b) Bond alignment with the in-situ resistance measurement apparatus.

Figure 44: Images of the in-situ flip-chip bond resistance measurement apparatus.

[4] Rosenberg, D., Kim, D., Das, R. et al. “3D integrated superconducting qubits”. npj Quantum Inf 3, 42 (2017).

[5] Wollack, E.A., Cleland, A.Y., Gruenke, R.G. et al. “Quantum state preparation and tomography of entangled mechanical resonators”. Nature 604, 463–467 (2022).

[6] Krayzman, L.V., “Thin-film 3D Resonators for Superconducting Quantum Circuits”. Ph.D. Thesis, Yale University, December 2022.