2015 EE410-LOCOS 0.2µm Poly CMOS Process Run Card Lot ID:_____

STEP 0.00 - PHOTOMASK #0- ZERO LEVEL MARKS
Starting materials is n-type silicon (5-10 ohm-cm). Add four test wafers labeled T1-T4. T1 and T2 will travel with the device wafers and get all of the processing steps. T3 and T4 will be added at Gate Ox and LTO Dep to be used for thickness measurements and for etch rate determination. For Zero Level Marks, all device wafers are processed, plus T1 and T2. Use T1 and T2 to optimize focus and exposure.

STEP 0.01 – SCRIBE & CLEAN
Hand-scribe wafers on the front side near the flat. Angle the lettering so no lines are drawn perpendicular or parallel to the flat.

Piranha Clean in **wbnometal -** 120°C; 10min; Dump rinse; SRD
Date _____ Time_____ Operator_____

STEP 0.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments_____

STEP 0.12 - SPIN COAT RESIST
Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).

System used: ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date_____ Time _____ Operator _____

Comments_____

STEP 0.13 – Spin Rinse Dry
All device wafers plus T1 and T2; Inspect backside of wafers for particles/ resist, clean w/ q-tip if needed prior to SRD

LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

STEP 0.14 – NON-ALIGNED EXPOSURE
Expose using ASML stepper:
Job name: ee410LOCOSR1
Layer ID: GLOBALMARKS
Layer Number: 0
Image ID: XPA
Reticle ID: 45023981A009

Exposure used:_____

Date _____ Time _____ Operator _____

Comments_____

STEP 0.16 – POST EXPOSE BAKE
Bake using SVG Dev track, bake program 1 (bake only)

System used: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments_____

STEP 0.18 - RESIST DEVELOP
Develop using SVG Dev track, develop program 3 (develop) and bake program 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments_____

STEP 0.20 – VISUAL INSPECTION
Visual microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

Comments_____

REWORK DONE? ❑***yes*** ❑***no***

Wafers reworked: _____
If yes, attach REWORK sheet here.

STEP 0.24 – ALIGNMENT MARK SILICON ETCH
All device wafers plus T1 and T2.

amtetcher, Program 4 for 0:05:00.

Date_____ Time _____ Operator _____

Comments_____

STEP 0.25 - RESIST ASH
All device wafers plus T1 and T2
gasonics, recipe sequence 014
Date_____ Time _____ Operator _____
Comments_____

STEP 0.26 – STANDARD RESIST STRIP
All device wafers plus T1 and T2

wbnonmetal, Piranha @ 120°C, 30', dump rinse, spin dry
Date_____ Time _____ Operator _____
Comments_Measure step ht (Spec 1200+/-200A)_____

STEP 0.28 - STANDARD PRE-DIFFUSION CLEAN
All device wafers plus T1 and T2.

Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH @ 50°C, 10',dump rinse; 50:1 DI:HF @ Room Temp, 30 sec, dump rinse
5:1:1 DI:H2O2:HCl @ 50°C, 10',dump rinse, spin dry

Date _____ Time _____ Operator _____

Comments_____

STEP 0.30 - BLANKET SUBSTRATE IMPLANT
All device wafers- Add one bare Si (N-type) TW per box (scribed w/ implant ID) for monitoring; Store test wafers after implant.
Implant Services: 150 keV, P31, 1.5 x10^{13} cm^{-2}.

Date _____ Time _____ Operator _____

Comments_____

STEP 0.32 - STANDARD PRE-DIFFUSION CLEAN
All device wafers plus T1 and T2

Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH, 50°C, 10', dump rinse, 50:1 DI:HF @ Room Temp, 30 sec, dump rinse
5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse, spin dry

Date _____ Time _____ Operator _____

Comments_____

STEP 0.34 - LOCOS PAD OXIDATION GROWTH
All device wafers plus T1 and T2. Ramped process 850°C, wet for 12min., ≈ 200Å,
Thermco1: 1WETOX
thermco2: 2WETOX Tube Used: _____

Date _____ Time _____ Operator _____

Oxide Growth Time: _____

Comments: _____

STEP 0.36 - LOCOS NITRIDE DEPOSITION
All device wafers plus Test Wafers. 785°C, 2,000 Å
Wafers must go in to Nitride deposition within 1 hour of oxide growth.
thermcoNitride: Program: N2
tylannitride: Program Nitride2 Tube used_____

Date _____ Time _____ Operator _____

Nitride Deposition Time:_____

Comments: _____

STEP0.38 –THICKNESS MEASUREMENT
Use Woollam, WVASE program EE410 / LOCOS to measure the oxide and nitride thickness and uniformity on T1.

Oxide: T_____ C_____ B_____ R_____ L_____

Nitride: T_____ C_____ B_____ R_____ L_____

Thk % Uniformity: Oxide_____ Nitride_____

Comments_____

STEP 1.00 - PHOTOMASK #1- ISO
All device wafers plus T1 and T2. Use T1 and T2 to optimize focus and exposure.

STEP 1.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments_____

STEP 1.12 - SPIN COAT RESIST
Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).

System used: ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date_____ Time _____ Operator_____

Comments_____

STEP 1.13 – Spin Rinse Dry -All device wafers plus T1 and T2
Inspect & clean backside of all wafers for particles/ resist residue

LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

STEP 1.14 – ALIGNEDFOCUS-EXPOSURE MATRIX
Expose using ASML stepper:
Job name: ee410LOCOSR1
Layer ID: 1
Layer Number: ISO
Image ID: ISO
Reticle ID: EE410 2008 1

Focus Minimum: 0.0 um Focus Step: 0.2 um

Exposure Min.: 40 mJ Exposure Step: 10 mJ

Focus Used: _____ Exposure Used: _____

Date _____ Time _____ Operator _____

Comments_____

STEP 1.16 - ALIGNED EXPOSURE
Expose using ASML stepper:
Job name: ee410LOCOSR1
Layer ID: 1
Layer Number: ISO
Image ID: ISO
Reticle ID: EE410 2008 1

Focus Used: _____ Exposure used:_____

Date _____ Time _____ Operator _____

Comments_____

STEP 1.18 – POST EXPOSE BAKE
Bake using SVG Dev track, bake program 1 (bake only)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments_____

STEP 1.20 - RESIST DEVELOP
Develop using SVG Dev track, develop program 3 (develop) and bake program 1 (bake)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments_____

STEP 1.22 – VISUAL INSPECTION
Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

Comments_____

REWORK DONE? ❑*yes* ❑*no*

Wafers reworked: _____
If yes, attach REWORK sheet here.

STEP 1.24 – LOCOS NITRIDE DRY ETCH
All device wafers plus T1 and T2. Use T1 to establish the etch time

Drytek 2: Recipe: Nitride

Total Etch Time _____

Date_____ Time _____ Operator _____

Comments _____

STEP 1.26 - THICKNESS MEASUREMENT
Use Nanospec program 7 to measure the Pad oxide thickness and uniformity on T1.

Oxide: T_____ C_____ B_____ R_____ L_____

Thk % Uniformity: Oxide_____

Comments_____

STEP 1.27 - RESIST ASH
All device wafers plus T1 and T2

gasonics, recipe sequence 014

Date_____ Time _____ Operator _____

Comments_____

STEP 1.28 - STANDARD RESIST STRIP
All device wafers plus T1 and T2

wbnonmetal, Piranha @ 120°C, 20', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 1.30 - STANDARD PRE-DIFFUSION CLEAN
All device wafers plus T1 and T2

Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH @ 50°C, 10', dump rinse; 50:1 DI:HF @ Room Temp, 30 sec, dump rinse;
5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 1.32 - FIELD OXIDATION
All device wafers plus T1 and T2. Ramped process

Wet Oxide at 1000C, 1hr:40 min, ~5,400 Å

Thermco1 or 2: WETOX ❑***Thermco1*** ❑***Thermco2***

Date _____ Time _____ Operator _____

Comments _____

STEP 1.34 – THICKNESS MEASUREMENT
Use Nanospec program 1 to measure the Field oxide thickness and uniformity on T1.

Oxide: T_____ C_____ B_____ R_____ L_____

Thk % Uniformity: Oxide_____

Comments_____

STEP 1.36 – OXIDIZED NITRIDE STRIP
6:1 BOE, ~45sec.

WBNONMETAL

Etch Time: _____

Date _____ Time _____ Operator _____

Comments: _____

STEP 1.38 – NITRIDE WET STRIP
All device wafers plus T1 and T2.

wbnitride, Hot Phosphoric Acid, 155C, ~60min. , dump rinse, spin dry

Etch Time: _____

Date _____ Time _____ Operator _____

Comments: _____

STEP 1.40 – THICKNESS MEASUREMENT
Use Nanospec program 1 to measure the field oxide and program 7 to measure the Pad oxide and uniformity on T1.
FieldOx: T_____ C_____ B_____ R_____ L_____

Thk % Uniformity: FieldOx_____

PadOx: T_____ C_____ B_____ R_____ L_____

Thk % Uniformity: PadOx_____

Comments_____

STEP 2.00 - PHOTOMASK #2 – P-WELL IMPLANT
All device wafers plus T1 and T2. Use T1 and T2 to optimize focus and exposure.

STEP 2.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments_____

STEP 2.12 - SPIN COAT RESIST
Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).

System used: : ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date_____ Time _____ Operator_____

Comments_____

STEP 2.13 – Spin Rinse Dry
All device wafers plus T1 and T2
Inspect backside of wafers for particles and resist residue & clean prior to SRD

LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

STEP 2.14 - ALIGNED EXPOSURE
Expose using ASML stepper:
Job name: ee410LOCOSR1
Layer ID: 2
Layer Number: P-WELL
Image ID: P-WELL
Reticle ID: EE410 2008 1

Exposure used:_____

Date _____ Time _____ Operator _____

Comments_____

STEP 2.16 – POST EXPOSE BAKE
Bake using SVG Dev track, bake program 1 (bake only)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments _____

STEP 2.18 - RESIST DEVELOP
Develop using SVG Dev track, develop program 3 (develop) and bake program 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

STEP 2.20 – VISUAL INSPECTION
Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

REWORK DONE? ❑***yes*** ❑***no***

Wafers reworked: _____
If yes, attach REWORK sheet here.

STEP 2.22 - P-WELL IMPLANT
All device wafers- Add one bare Si (N-type) TW per box (scribed w/ implant ID) for monitoring; Store test wafers after implant.

Implant Services: 180keV, 4e13**,** B11 cm^{-2}.

Date _____ Time _____ Operator _____

Comments _____

STEP 2.23 - RESIST ASH
All device wafers plus T1 and T2

gasonics, recipe sequence 014

Date_____ Time _____ Operator _____

Comments_____

STEP 2.24 - STANDARD RESIST STRIP
All device wafers plus T1 and T2

wbnonmetal, Piranha @ 120°C, 20', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 2.26 - STANDARD PRE-DIFFUSION CLEAN
All device wafers plus T1 and T2

Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH, 50°C, 10', dump rinse; 50:1 DI:HF @ Room Temp, 30 sec, dump rinse; 5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 2.28 – Kooi Oxidation and P-WELL Drive-In
All device wafers plus T1 and T2.

Thermco1: 1WTOXAN
Kooi: 15min, 850C in steam
Drive-in: 300min, 1000C in nitrogen

Date_____ Time _____ Operator _____

Comments_____

STEP 2.30 – THICKNESS MEASUREMENT
Use the Nanospec program 1 to measure the Kooi oxide thickness and uniformity on T1.

Oxide: T_____ C_____ B_____ R_____ L_____

Thk % Uniformity: Oxide_____

Comments_____

STEP 2.32 - STANDARD PRE-DIFFUSION CLEAN
All device wafers plus T1, T2 and T3 (for Gate Ox measurement)

Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH, 50°C, 10', dump rinse; 50:1 DI:HF @ Room Temp, 30 sec, dump rinse; 5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 2.34 - SACRIFICIAL OXIDE STRIP
All device wafers plus T1,T2 & T3

Wbclean-1 or -2 50:1 DI:HF @ Room Temp, dump rinse, spin dry

Etch Time: _____mins

Date_____ Time _____ Operator _____

Comments_____

STEP 2.36 - THICKNESS MEASUREMENT
Use Nanospec program 7 (thin oxide) to measure T1 to ensure complete Sacrificial oxide removal.

System used: ❑***nanospec*** ❑***nanospec2***

T_____C_____B_____R_____L_____

Date_____ Time _____ Operator _____

Comments _____

STEP 2.38 - GATE OXIDATION
All device wafers plus T1, T2 and T3. Ramped process 20min @ 900°C, dry for ~100Å

NOTE: Run (1/2)TLCCLEA program on Thermco 1/2 to clean tube before GATEOX. This will take about 4 hours to complete. Wafers must go immediately into thermcopoly after GateOx with no cleaning steps. This is to ensure contamination is minimal.

Thermco1 or 2: (1/2) DRYOX ❑***Thermco1*** ❑***Thermco2***

Oxidation Time: _____

Date _____ Time _____ Operator _____

Comments: _____

STEP 2.40 - POLYSILICON DEPOSITION
All device wafers plus T1 and T2. T3 has been removed for Gate Ox measurement.

LPCVD @ 550°C, ≈ 2,000Å

Thermocpoly Program P550POLY

Deposition Time: _____

Date _____ Time _____ Operator _____

Comments: _____

STEP 2.42 – THICKNESS MEASUREMENT
Use Woollam, WVASE program EE410 / GATE POLY to measure the oxide and nitride thickness and uniformity on T1.

Poly: T_____ C_____ B_____ R_____ L_____

Oxide: T_____ C_____ B_____ R_____ L_____

Thk % Uniformity: Poly _____ Oxide _____

Comments_____

STEP 3.00 - PHOTOMASK #3 - GATE
All device wafers plus T1 and T2. Use T1 and T2 to optimize focus and exposure.

STEP 3.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments_____

STEP 3.12 - SPIN COAT RESIST
Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).

System used: : ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date _____ Time _____ Operator _____

Comments_____

STEP 3.13 – Spin Rinse Dry -All device wafers plus T1 and T2
Inspect and clean backside of wafers for particles/ resist residues

LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

STEP 3.14 – ALIGNED EXPOSE
Expose using asml stepper:
Job name: ee410LOCOSR1
Layer ID: GATE
Layer Number: 3
Image ID: GATE
Reticle ID: EE410 2008 1

Date _____ Time _____ Operator _____

Exposure used:_____

Comments_____

STEP 3.16 – POST EXPOSE BAKE
Bake using SVG Dev track, bake program 1 (bake only)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments_____

STEP 3.18 - RESIST DEVELOP
Develop using SVG Dev track, develop program 3 (develop) and bake program 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____ Time _____ Operator _____

Comments_____

STEP 3.20 - INSPECTION
Inspect and clean backside of all wafers for particles/ residues. Visual and microscope inspection. Check for defects, alignment AND exposure quality.

Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

Comments _____

REWORK DONE? ❑***yes*** ❑***no***

Wafers reworked: _____
If yes, attach REWORK sheet here.

STEP 3.22 - POLY ETCH
All device wafers plus T1 and T2. Use T1 to establish end point time.

P5000 Program: POLY ETCH
End Point Algorithm: SU_POLY1.alg

End Point Time: _____ Over Etch Time _____

Date _____ Time _____ Operator _____

Comments_____

STEP 3.23- RESIST ASH
All device wafers plus T1 and T2

gasonics, recipe sequence 014

Date_____ Time _____ Operator _____

Comments_____

STEP 3.24 - STANDARD RESIST STRIP
All device wafers plus T1 and T2

wbnonmetal, Piranha @ 120°C, 20', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 4.00 - PHOTOMASK #4 – N-DOPE
All device wafers plus T1 and T2. Use T1 and T2 to optimize focus and exposure.

STEP 4.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments_____

STEP 4.12 - SPIN COAT RESIST
Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).

System used: : ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date _____ Time _____ Operator _____

Comments _____

STEP 4.13 – Spin Rinse Dry -All device wafers plus T1 and T2
Inspect and clean backside for particles and resist residues

LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

STEP 4.14 - ALIGNED EXPOSE
Expose using asml stepper:
Job name: ee410LOCOSR1
Layer ID: N-DOPE
Layer Number: 4
Image ID: N-DOPE
Reticle ID: EE410 2008 1

Date _____ Time _____ Operator _____

Exposure used:

Comments_____

STEP 4.16 – POST EXPOSE BAKE
Bake using SVG Dev track, bake program 1 (bake only)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments_____

STEP 4.18 - RESIST DEVELOP
Develop using SVG Dev track, programs 3 (develop) and 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____ Time _____ Operator _____

Comments_____

STEP 4.20 – VISUAL INSPECTION
Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

Comments _____

REWORK DONE? ❑***yes*** ❑***no***

Wafers reworked: _____
If yes, attach REWORK sheet here.

STEP 4.22 - RESIST HARDENING (for implantation)
Hard bake 30 mins @ 110C.

Date _____ Time _____ Operator _____

Comments_____

STEP 4.24 - N-SOURCE/DRAIN IMPLANT
All device wafers- Add one bare Si (N-type) TW per box (scribed w/ implant ID) for monitoring; Store test wafers after implant.

Implant Services: 50 keV, As75, $2x10^{15}$ cm^{-2}

Date _____ Time _____ Operator _____

Comments _____

STEP 4.26 - RESIST ASH
All device wafers plus T1 and T2

gasonics, recipe sequence 014

Date_____ Time _____ Operator _____

Comments_____

STEP 4.26 - STANDARD RESIST STRIP
All device wafers plus T1 and T2

wbnonmetal, Piranha @ 120°C, 20', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 5.00 - P-DOPE BLANKET IMPLANT
All device wafers- Add one bare Si (N-type) TW per box (scribed w/ implant ID) for monitoring; Store test wafers after implant.
Implant Service: 50 keV, BF_2 49, $5x10^{14}$ cm^{-2}
Date _____ Time _____ Operator _____
Comments _____

STEP 5.30 - STANDARD PRE-DIFFUSION CLEAN
All device wafers plus T1, T2 and T4.

Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH @ 50°C, 10', dump rinse; 50:1 DI:HF @ Room Temp, 30 sec, dump rinse; 5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 5.32 - LTO DEPOSITION
All device wafers plus T1, T2 and T4 (for LTO measurement after Densify). Undoped, LPCVD @ 400°C, ≈ 6000Å

tylanbpsg, Program LTO400PC

Date_____ Time _____ Operator _____

Comments_____

STEP 5.34 – MODIFIED PRE-DIFFUSION CLEAN

Note: The Modified Pre-Diffusion clean may be omitted if wafers move from LTO dep to LTO densification in less than one hour. All device wafers plus T1, T2 and T4 (for LTO measurement after Densification)

Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH @ 50°C, 10', dump rinse; 5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 5.36 - LTO DENSIFICATION
All device wafers plus T1, T2 and T4. Ramped process 30' min @ 950°C, in steam

Thermco1, 2 or 3: 1/2/3WETOX Tube_____

Date _____ Time _____ Operator _____

Comments_____

STEP 5.38 –THICKNESS MEASUREMENT
Use Nanospec program 1 to measure the LTO thickness and uniformity on T1.

Oxide: T_____ C_____ B_____ R_____ L_____

Thk % Uniformity: Oxide_____

Comments_____

STEP 6.00 - PHOTOMASK #6 – CONTACT
All device wafers plus T1,T2, and T4. Use T1 and T2 to optimize focus and exposure. T4 will be used as a test wafer at SiO_2 RIE and so needs to be patterned.

STEP 6.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments_____

STEP 6.12 - SPIN COAT RESIST
Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).

System used: : ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date _____ Time _____ Operator _____

Comments _____

STEP 6.13 – Spin Rinse Dry- All device wafers plus T1 and T2
Inspect and clean backside for particles and resist residues

LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

STEP 6.14- ALIGNED EXPOSE
Expose using asml stepper:
Job name: ee410LOCOSR1
Layer ID: CONTACT
Layer Number: 6
Image ID: CONTACT
Reticle ID: EE410 2008 2

Date _____ Time _____ Operator _____

Exposure used:_____

Comments_____

STEP 6.16 – POST EXPOSE BAKE
Bake using SVG Dev track, bake program 1 (bake only)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments_____

STEP 6.18 - RESIST DEVELOP
Bake using SVG Dev track, programs 3 (develop) and 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____ Time _____ Operator _____

Comments_____

STEP 6.20 - VISUAL INSPECTION
Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

Comments _____

REWORK DONE? ❑***yes*** ❑***no***

Wafers reworked: ______________________________
If yes, attach REWORK sheet here.

STEP 6.22- PLASMA OXIDE ETCH
All device wafers plus T1, T2 and T4. Establish the etch rate using T4.

amtetcher, Program 3, CHF_3/O_2

Etch Rate: _______________ Etch Time:_________________

Date _________ Time _________ Operator ______________

Comments____

STEP 6.24 - THICKNESS MEASUREMENT
Use Nanospec program 7 (thin oxide) to measure T1 to ensure complete oxide removal.

System used: ❑***nanospec*** ❑***nanospec2***

T_________C_________B_________R_________L__________

Date_________ Time _________ Operator _______________

Comments ____

STEP 6.24 - RESIST ASH

gasonics, recipe sequence 014

Date_________ Time _________ Operator _______________

Comments____

STEP 6.26 STANDARD RESIST STRIP
All device wafers plus T1 and T2. T4 may be omitted at this point.

wbnonmetal, Piranha @ 120°C, 20', rinse, spin dry

Date_________ Time _________ Operator _______________

Comments____

STEP 6.28 - STANDARD PRE-METAL CLEAN
All device wafers plus T1 and T2

Wbclean-1 or-2, 5:1:1 H2O:H2O2:NH4OH @ 50°C, 10', dump rinse; 5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse
50:1 DI:HF @ Room Temp, 30 sec, dump rinse; spin dry

Date_________ Time _________ Operator _______________

Comments____

STEP 6.30 - METAL DEPOSITION

Intlvac_sputter, 10,000A of Al-1%Si; Program: STANDARD B

Date_________ Time _________ Operator _______________

Comments____

STEP 7.00 - PHOTOMASK #7 - METAL
All device wafers plus T1 and T2. Use T1 and T2 to optimize focus and exposure.

STEP 7.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date_________ Time _________ Operator _______________

Comments____

STEP 7.12 -1.6 micron SPIN COAT RESIST
Apply 1.6 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track program 8 (coat and softbake).

System used: : ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date _________ Time _________ Operator ______________

Comments ____

STEP 7.13 – Spin Rinse Dry- All device wafers plus T1 and T2
Inspect and clean backside for particles and resist residues

LithoSRD

Date_________ **Time** _________ **Operator** _______________

Comments____

STEP 7.14 - ALIGNED EXPOSE
Expose using asml stepper:

Job name: ee410LOCOSR1
Layer ID: 7
Layer Number: METAL
Image ID: METAL1
Reticle ID: EE410 2008 2

Date _________ Time _________ Operator ______________

Exposure used:______________________________________

Comments____

STEP 6.16 – POST EXPOSE BAKE
Bake using SVG Dev track, bake program 2 (bake only)

System: ❑***svgdev*** ❑***svgdev2***

Date _________ Time _________ Operator ______________

Comments____

STEP 7.16 - RESIST DEVELOP
Bake using SVG Dev track, programs 4 (develop) and 2 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date________ Time _________ Operator ________________

Comments____

STEP 7.18 – VISUAL INSPECTION
Inspect and clean backside for particles and resist residues
Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected ______ ______ ______ ______ ______

Date _________ Time _________ Operator ______________

Comments ____

REWORK DONE? ❑***yes*** ❑***no***

Wafers reworked: _____
If yes, attach REWORK sheet here.

STEP 7.20 - METAL ETCH

p5000etch, Recipe CH A. METAL, ~120-150 sec.
End Point Algorithm: SU_Al_lg.alg

End Point Time: _____ Overetch Time: _____

Date_____ Time _____ Operator _____

Comments_____

STEP 7.22 – POST ETCH METAL PASSIVATION
Must be done immediately following removal from etch system

wbmetal, dump rinse, spin rinse dry

Date_____ Time _____ Operator _____

Comments_____

STEP 7.24 - METAL RESIST STRIP
Make sure the wafers are dry before putting in to PRS-3000 bath.

wbmetal, PRS-3000, @ 60°C, 20'; dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 7.26 - METAL CLEAN
Make sure the wafers are dry before putting in to PRS1000 bath.

wbmetal, PRS1000, @ 40°C, 10', dump rinse, spin dry

Date_____ Time _____ Operator _____

Comments_____

STEP 7.30 - ANNEAL AND ALLOY
45' forming gas (4% H_2 in N_2) @ 400°C

tylanfga Program FGA400

Date_____ Time _____ Operator _____

Comments_____

ELECTRICAL TEST!

STEP 100.00 - REWORK SHEET
REWORK PHOTOMASK LAYER# _____

Reworked wafers: _____

❑ Resist removal for wafers before metal deposition:

wbnonmetal, piranha clean, dump rinse 6X, spin-rinse dry

Date _____ Time _____ Operator _____

❑ Resist removal for wafers after metal deposition

wbmetal, PRS1000, dump rinse, spin-rinse dry

Date _____ Time _____ Operator _____

Comments _____

STEP 100.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments _____

STEP 100.12 - RESIST SPIN COAT
Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG coat programs 7 (coat and softbake)

System used: : ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date _____ Time _____ Operator _____

Comments _____

STEP 100.13 – Spin Rinse Dry- All device wafers plus T1 and T2 - Inspect and clean backside for particles and resist residues

LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

STEP 100.14 - ALIGNED EXPOSE
Expose using ASML Stepper,
❑ 0 – Global Marks: ee410LOCOSR1: 45023981A009
❑ 1 – ISO: ee410LOCOSR1: EE410 2008 1
❑ 2 – P-Well: ee410LOCOSR1: EE410 2008 1
❑ 3 – Gate: ee410LOCOSR1: EE410 2008 1
❑ 4 – N-Dope: ee410LOCOSR1: EE410 2008 1
❑ 6 – Contact: ee410LOCOSR1: EE410 2008 2
❑ 7 – Metal: ee410LOCOSR1: EE410 2008 2

Exposure Used: _____

Date _____ Time _____ Operator _____

Comments _____

STEP 100.16 - RESIST DEVELOP
Develop using SVG Dev track, programs 3 (develop) and 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments _____

STEP 100.18 - VISUAL INSPECTION
Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

Comments _____

STEP 200.00 - REWORK SHEET
REWORK PHOTOMASK LAYER# _____

Reworked wafers: _____

❑ Resist removal for wafers before metal deposition:

wbnonmetal, piranha clean, dump rinse 6X, spin-rinse dry

Date _____ Time _____ Operator _____

❑ Resist removal for wafers after metal deposition

wbmetal, PRS1000, dump rinse, spin-rinse dry

Date _____ Time _____ Operator _____

Comments _____

STEP 200.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments _____

STEP 200.12 - RESIST SPIN COAT
Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG coat programs 7 (coat and softbake)

System used: : ❑***svgcoat2*** ❑***svgcoat (backup option)***

Date _____ Time _____ Operator _____

Comments _____

STEP 200.13 – Spin Rinse Dry- All device wafers plus T1 and T2 - Inspect and clean backside for particles and resist residues

LithoSRD

Date_____ **Time** _____ **Operator** _____

Comments_____

STEP 200.14 - ALIGNED EXPOSE
Expose using ASML Stepper,
❑ 0 – Global Marks: ee410LOCOSR1: 45023981A009
❑ 1 – ISO: ee410LOCOSR1: EE410 2008 1
❑ 2 – P-Well: ee410LOCOSR1: EE410 2008 1
❑ 3 – Gate: ee410LOCOSR1: EE410 2008 1
❑ 4 – N-Dope: ee410LOCOSR1: EE410 2008 1
❑ 6 – Contact: ee410LOCOSR1: EE410 2008 2
❑ 7 – Metal: ee410LOCOSR1: EE410 2008 2

Exposure Used: _____

Date _____ Time _____ Operator _____

Comments _____

STEP 200.16 - RESIST DEVELOP
Develop using SVG Dev track, programs 3 (develop) and 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____ Operator _____

Comments _____

STEP 200.18 - VISUAL INSPECTION
Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____ _____ _____ _____ _____

Date _____ Time _____ Operator _____

Comments _____